Analog Integrated Circuits and Signal Processing
https://doi.org/10.1007/s10470-018-1141-5

A 14-bit 500-MS/s DAC with 211-MHz 70 dB SFDR bandwidth using TRI-DEMRZ

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Received: 4 September 2017 / Revised: 22 December 2017 / Accepted: 23 February 2018

Abstract
Time-relaxed interleaving dynamic element matching return-to-zero (TRI-DEMRZ) is proposed and verified in this paper to improve the spurious-free dynamic range (SFDR) of current-steering digital-to-analog converters (DACs). It incorporates time-relaxed interleaving (TRI), return-to-zero, and the dynamic-element-matching techniques, in a way that fosters the strength of each technique. As analyzed in this paper, merits beyond the combination of these techniques could be achieved. Firstly, TRI-DEMRZ provides a new dimension in the space domain, rather than the time domain, to explore the methods of mitigating nonlinear switching distortions. Secondly, this paper proves that, the image tone caused by typical channel mismatches between interleaved sub-DACs can be randomized into noise with TRI-DEMRZ. Circuit simulations and analysis are provided. An experimental 14-bit 500-MS/s current-steering DAC in 65 nm CMOS has been fabricated and measured, showing 81 dB SFDR at 5.5 MHz and more than 70 dB SFDR up to 211 MHz bandwidth. The SFDR improvement achieved by TRI-DEMRZ is more than 10 dB, which further verifies the effectiveness of TRI-DEMRZ.

Keywords Digital-to-analog converter (DAC) · Dynamic element matching (DEM) · Channel mismatch · Time-relaxed interleaving · Current-steering

1 Introduction

While most high-speed digital-to-analog converters (DACs) are implemented in the current-steering topology because of the high intrinsic switching speed and moderate matching property, recent research has revealed two main bottlenecks towards a high dynamic range [1–4]. One is the current source mismatch that affects the output amplitude. The other one is the nonlinear distortion caused by code-dependent switching glitches, which becomes more severe at a higher frequency with inevitable switching time mismatch and more switching activities.

Among various approaches, dynamic element matching (DEM) and return-to-zero (RZ) techniques are widely used to mitigate the aforementioned two aspects [1, 2, 4, 5]. With sufficient randomization, DEM is effective in averaging out current source mismatches. Meanwhile, RZ techniques are effective in mitigating the inter-symbol-interference (ISI) to reduce the code-dependent switching distortions. In [2], dynamic element matching return-to-zero (DMRZ) combined DEM and half-a-cycle RZ, leading to the first CMOS DAC with 70 dB SFDR up to 800 MHz.

Collectively incorporating the advantages of both the DMRZ technique in [2] and the time-relaxed interleaving technique in [3, 4, 6, 7], we have proposed TRI-DEMRZ, as depicted in Fig. 1. Compared with our previous effort in [4], this paper provides the first experimental measurement verifications and also fundamental analysis of TRI-DEMRZ that shows significant highlights, including:

- The proposed TRI-DEMRZ reveals and confirms a new design dimension by trading space (associated area and power) for better dynamic performance with assisting

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Published online: 14 March 2018

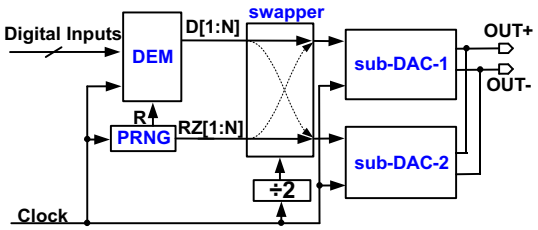


Fig. 1 The concept of TRI-DEMRZ

digital signal processing techniques such as randomization. Note that, in our proposed TRI-DEMRZ, switching distortions in the final output are reduced by means of space domain randomization, which is fundamentally different from the previous DMRZ method that deals with switching distortions in the time domain, which will be analyzed in Sect. 2. Such a new dimension provides more chance of distortion suppression and performance enhancement.

- The combination of interleaving and DEM, not only randomizes the static mismatch of current sources inside each sub-DAC, but also randomizes the channel mismatch between the two sub-DACs. In this paper, we theoretically prove that under certain mismatch distribution, the channel mismatch between interleaved sub-DACs can be randomized, and the related image tone can be smashed into noise with TRI-DEMRZ. In this way, TRI-DEMRZ provides a new method to deal with the channel mismatch in interleaving.

The rest of this paper is organized as follows. Section "Static mismatches and switching distortions" revisits the existing study of current source mismatches and code-dependent switching glitches revealing the new design dimension of TRI-DEMRZ. The derivation and analysis of channel mismatch randomization using TRI-DEMRZ are provided in Section "Channel mismatch randomization". The implementation and measurement of the experimental DAC are provided in Section "Implementation and experiment". Finally, Section "Conclusion" concludes this paper.

2 Static mismatches and switching distortions

This section revisits the inherent features of the current source mismatches and code-dependent switching glitches, so as to get in-depth understanding of the pros and cons of existing solutions. This also shows how DEM and RZ techniques could potentially outperform or collaborate with other techniques. Then the basic concept of TRI-DEMRZ technique is revisited to show how it expands the design space for a higher dynamic range.

2.1 Problems in dealing with inter sub-DACs current source mismatches

Various sources result in systematic and random mismatches between current sources in fabricated current-steering DACs. These mismatches not only limit the static output signal amplitude, but also deteriorate the spectral performance [1, 2, 8–19]. DEM is a method to deal with the mismatches by selecting current sources dynamically from random places in the current source array to make the integrated amplitude errors less code-dependent [1, 2]. Such randomization leads to averaging of the mismatches, and also contributes to harmonic distortion suppression. As the effectiveness of existing DEM on the mismatch noise shaping depends on "averaging over time" [2, 20], signals with amplitude near full scale at a higher frequency have less room for randomization and consequently, less mismatch averaging benefits in wideband Nyquist DACs. Nevertheless, for applications where SFDR is the bottleneck due to the current source mismatches, DEM is intriguing to improve SFDR by turning distortions into flat noise [1].

Meanwhile, there is urgent need of a good method to deal with the channel mismatch between the sub-DACs. Such channel mismatches exist when an interleaving DAC has more than one sub-DACs, as in [3, 4]. Section 2.3 of this paper will introduce the proposed interleaving DEM method for such DACs.

2.2 Problems in dealing with switching glitch distortions

The performance of conventional high-speed current-steering DACs is sensitive to the code-dependent switching glitches that cause harmonic distortions at the output [1–3, 21, 22, 23–28]. Figure 2 illustrates two such dominant distortion sources of (1) coupled switching glitches from the switch control signals directly to the current routes, and (2) charge variation in each current source due to output amplitude modulation or varying current delivered by the differential switches. With more frequent switching activities, these distortions become more severe at a higher frequency. It is noted that these effects relate to the previous and current input digital codes of the DAC, generating inter-symbol-interference (ISI) [28, 29]. To mitigate these effects, circuit and layout optimizations could be applied, such as transistor size and biasing tuning, switch control signal swing and cross-over voltage adjustment, layout parasitics reduction, and tree-like layout usage, etc. [2, 3, 25, 27]. Meanwhile, RZ techniques have

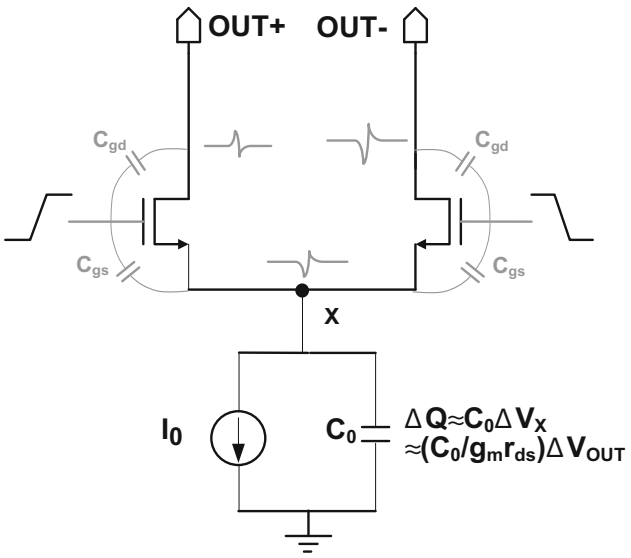


Fig. 2 Nonlinear switching glitches due to code-dependent gate coupling and charge resettling modulated by the output voltage during a switching transition [25]

also been proved useful [30–32]: Analog RZ (ARZ) with additional reset-and-track operations could isolate the output from code-dependent settling glitches and only tracks the settled deglitched signal, with the overhead of additional re-sampling circuitry with parasitics and limit the high-frequency performance [33, 34]; Digital RZ (DRZ) modifies only the digital decoder so that the analog output is reset after every code accordingly, showing effectiveness in removing the ISI effects [3, 30].

Nevertheless, it is important to understand that even if the ISI effects (history effects) are removed, some harmonics induced by the input-code-dependent effects mentioned above could not be fully eliminated. For example, the switching or re-sampling timing skews [35], the re-sampling coupling glitches or switch coupling glitches, as well as the charge resettling at the internal nodes inside each current route due to switching or re-sampling, will cause code-dependent glitches with carry-on harmonics at the DAC output. Therefore, these approaches to a high dynamic range, either by optimizing the existing circuit, layout, segmentation, adding dummy switching activities, or employing RZ operations, are useful, but still have inherent limitations for a DAC with a high SFDR.

2.3 Proposed TRI-DEMRZ in comparison with DEM and interleaving techniques

Dynamic random switching techniques provide another effective way to suppress the harmonic distortions by using code-independent switching [1–3, 30, 36–38]. In the time domain, the random operation could incorporate with RZ so that random and non-random operations are carried out alternately in phases of half clock cycles [2, 3, 30]. The random operation could be either in the phase of RZ, as in digital random return-to-zero (DRRZ) and TRI-DRRZ [3, 30], or in the phase of normal operation, as in DMRZ [2]. Figure 3(a) illustrates the comparison between NRZ, DRRZ, and DMRZ output.

The problems of existing incorporated DEM and RZ methods, as revealed in [3], are high-speed design challenges or drawbacks, including (1) tight timing requirement as the switching activities need to settle within half a clock period, and (2) signal energy loss, and higher image tones in the 2nd Nyquist zone to filter out due to the RZ output pattern. The mitigating method is time-relaxed interleaving (TRI) [3], which uses two parallel interleaving sub-DACs, each operating in a mode of alternate NRZ and RZ that settles within one full clock period instead of half a clock period. Figure 3 shows the TRI-DRRZ waveforms. It is clear that the two DRRZ problems are solved. The SFDR can also be higher because the signal power is higher than DRRZ while the total number of switching activities remains the same.

The technique of TRI in [3] is a new concept to seek for higher performance by trading extra space or area while doing random switching, which is fundamentally different from the previous DRRZ or DMRZ method of doing it in the time domain. The performance improvement would be significant when timing and amplitude mismatches caused by the increased area are not yet the performance bottleneck. Unfortunately, the previously proposed technique of TRI-DRRZ in [3] did not make full use of TRI to deal with current source mismatches in each subDAC, or between subDACs. This is because subDACs in [3] are (1) physically and operationally independent of each other, and (2) thermometer-decoded without DEM as depicted in Fig. 3(b).

To solve such problem in TRI-DRRZ while still keeping the advantages of TRI and incorporated random switching and RZ operations, we propose TRI-DEMRZ in this paper. Figure 4 depicts the TRI-DEMRZ concept. It consists of a DEM decoder, a RZ decoder, and two sub-DACs, i.e. subDAC-1 and subDAC-2. In each odd clock phase, sub-DAC-1 generates an NRZ output under the control of the DEM decoder, and subDAC-2 returns to zero under the control of the RZ decoder. In each even clock phase, subDAC-1 and subDAC-2 interchange actions. It is noted that the RZ decoding needs not to be random, as is the case in DMRZ. Figure 4 also compares the waveforms of DMRZ and TRI-DEMRZ.

Same as the evolvement from DRRZ to TRI-DRRZ, the proposed TRI-DEMRZ has essential advantages over DMRZ, including (1) the relaxation of settling-time requirements, (2) the increase of signal energy and more suppression of image tones, and (3) higher SFDR due to

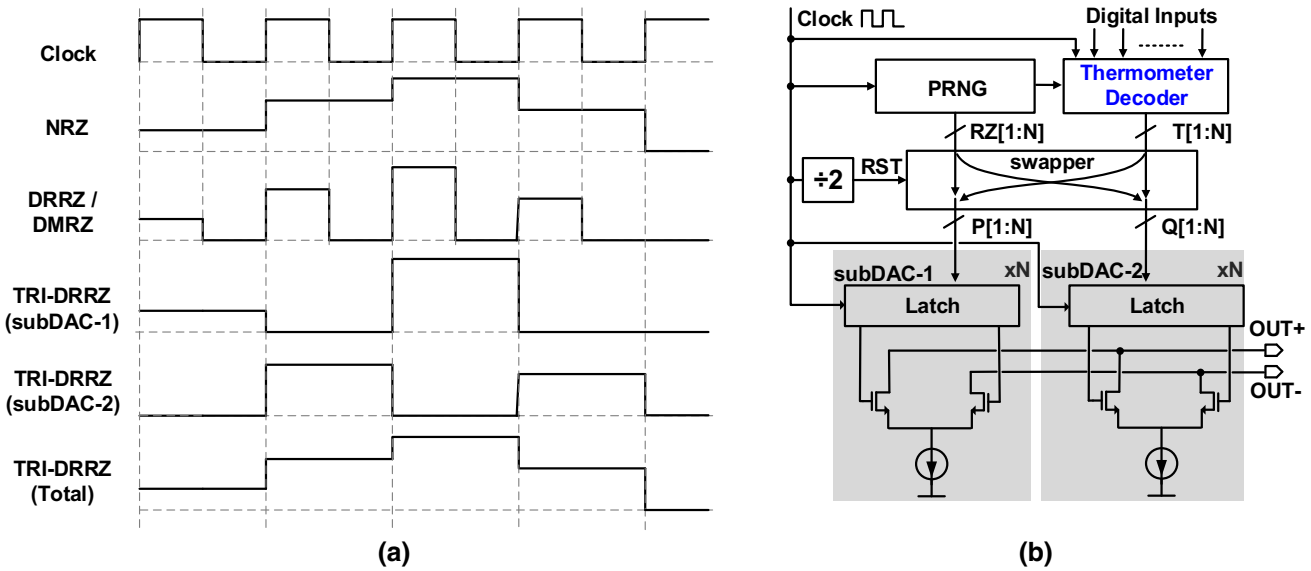


Fig. 3 **a** The output waveform comparison between NRZ, DRRZ, DMRZ and TRI-DRRZ, showing different settling behavior [3]. **b** The basic structure of TRI-DRRZ [3]

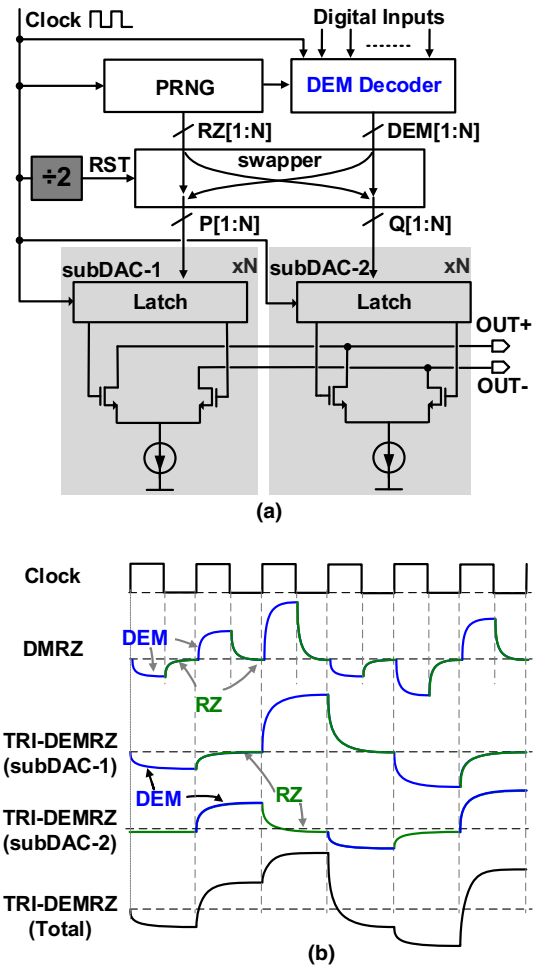


Fig. 4 The function diagram of TRI-DEMRZ. **a** Implementation; **b** Transient waveform examples [4]

higher signal power but the same total number of randomized switching activities and corresponding switching glitches.

It is noted that the total number of switching activities in TRI-DEMRZ is the same as DMRZ, DRRZ, and TRI-DRRZ, all higher than NRZ. Detailed analysis in this aspect has been provided in [3]. Such behavior results in higher noise level than NRZ DACs, which is one side effect of these techniques. Another side effect of TRI-DEMRZ is the doubled number of current sources, which is the main drawback of interleaving techniques. However, compared with the traditional uncalibrated interleaved DACs, e.g. the DAC with TRI-DRRZ in [3], the area of each sub-DACs could be smaller with TRI-DEMRZ. This is because the dynamic element matching in TRI-DEMRZ transforms the mismatch-caused harmonics or tones into noise with lower requirement on the area for current source matching [13].

Summarizing the discussions above, TRI-DEMRZ significantly extends the design space of wideband high-SFDR DACs by trading additional randomized switch activities and chip area for a higher SFDR. Table 1 summarizes the performance comparisons between NRZ, DRRZ, DMRZ, TRI-DRRZ and TRI-DEMRZ.

3 Channel mismatch randomization

This section reveals and studies the channel mismatch randomization property of TRI-DEMRZ. The use of DEM allows each sub-DACs to be smaller size, which on the contrary deteriorates the channel mismatch for interleaving

Table 1 Comparisons between TRI-DEMRZ and others with NRZ as the baseline

Specifications	NRZ	DRRZ	DMRZ	TRI-DRRZ	TRI-DEMRZ
Settling requirement	–	☹	☹	–	–
Output signal power	–	☹	☹	–	–
Image suppression[a]	–	☹	☹	–	–
Switch driving power	–	☹	☹	☹	☹
Static mismatch averaging	–	☹	☺	☹	☺
Chip area	–	–	☺	☹☹	☹
SFDR[b]	–	☺	☺☺	☺☺	☺☺☺

"☺", "☹", and "–" represent better, worse, and no significantly different results, respectively

[a]The image represents the signal image in the 2nd Nyquist spectrum region

[b]Subject to signal power and distortions by mismatch and switching glitches

technique. Fortunately, the use of DEM not only randomizes the static mismatch inside each sub-DAC but also randomizes the channel mismatch between two sub-DACs at the same time. Since DEM introduces redundant combination of current sources, the use of DEM equivalently improves the alternative selection for sub-DACs compared with the interleaving without DEM [39]. This property can help to obscure the channel mismatch between the two sub-DACs. The detailed derivation and analyses of this feature are provided in this section.

3.1 Mathematical model

For simplicity, the input and output of a single channel DAC with DEM are represented by $x(n)$ and $y(n)$, respectively. According to [40], the time-average autocorrelation $\bar{R}_{yy}(k)$ of the output $y(n)$ in the single channel DAC with N current sources is:

$$\bar{R}_{yy}(k) = (1+\alpha)\bar{R}_{xx}(k) + \bar{\beta} + \bar{\sigma}^2\delta(k), \tag{1}$$

with probability 1, where $\bar{R}_{xx}(k)$ is the time-average autocorrelation of input $x(n)$, $\delta(k)$ is the Kronecker delta function which is non-zero only when k is 0. The coefficient in (1): α, $\bar{\beta}$, $\bar{\sigma}^2$ are constant and the expression for them are provided in [40]:

$$\alpha = e_0(2+e_0), \tag{2a}$$

$$\bar{\beta} = 2e_1(1+e_0)\bar{M}_x + e_1^2, \tag{2b}$$

and

$$\bar{\sigma}^2 = \frac{1}{N-1}\left[e_0^2 - \frac{(e_h-e_l)^T(e_h-e_l)}{N\Delta^2}\right] .[x_{min}x_{max} + \bar{R}_{xx}(0) - (x_{min}+x_{max})\bar{M}_x] \tag{2c}$$

where $\bar{M}_x$ is the time-average mean of input x(n), while Δ is the step-size of the DAC, and

$$e_0 = \frac{1}{N\Delta}\left(1^T e_h - 1^T e_l\right), \tag{3a}$$

$$e_1 = \frac{1}{N\Delta}\left(x_{min}1^T e_h - x_{max}1^T e_l\right), \tag{3b}$$

where e_h and e_l represent the conversion errors of each current sources in DAC, and

$$e_h = \begin{bmatrix} e_{h_1} \\ \vdots \\ e_{h_N} \end{bmatrix},\ e_l = \begin{bmatrix} e_{l_1} \\ \vdots \\ e_{l_N} \end{bmatrix},\ 1^T = [1\cdots 1] \tag{4}$$

while e_{h_i} and e_{l_i} are the errors of the ith current sources.

Based on the DEM analysis for one single channel DAC, the rest of this subsection provides the analysis of channel mismatch randomization incorporating DEM and interleaving.

Let $x(n)$ to be the input digital code, $y_1(n)$ and $y_2(n)$ to represent the function of each sub-DACs with DEM, both of which is unary decoded with N current sources and obeys (1), and let $y(n)$ to be the interleaved output of the DAC with TRI-DEMRZ, which can be represented as:

$$y(n) = T(n)y_1(n) + (1-T(n))y_2(n), \tag{5}$$

where $T(n)$ represents the switching function between each sub-DAC and changes between 0 and 1 each clock cycle in turn.

Firstly, the cross-correlation between the output $y(n)$ and the channel mismatch $\varepsilon(n) = y_1(n) - y_2(n)$ is derived:

$$R_{y,\varepsilon}(n,k) = E[y(n)(y_1(n+k) - y_2(n+k))]. \tag{6}$$

Substituting (5) into (6), collecting terms gives

$$\begin{aligned} R_{y,\varepsilon}(n,k) = {} & E[y_2(n)y_1(n+k)] - R_{y_2,y_2}(n,k) \\ & + T(n)\left[R_{y_1,y_1}(n,k) + R_{y_2,y_2}(n,k)\right. \\ & \left. - E[y_1(n)y_2(n+k)] - E[y_2(n)y_1(n+k)]\right] \end{aligned} \tag{7}$$

Assuming that each sub-DAC is independent of one another gives

$$E[y_2(n)y_1(n+k)] = E[y_2(n)]E[y_1(n+k)], \tag{8a}$$

$$E[y_1(n)y_2(n+k)] = E[y_1(n)]E[y_2(n+k)]. \tag{8b}$$

Using the conclusion in [40], we have

$$E[y_2(n)] = x(n)\left(1+\mu_{0,2}\right) + \mu_{1,2}, \tag{9a}$$

$$E[y_2(n+k)] = x(n+k)\left(1+\mu_{0,2}\right) + \mu_{1,2}, \tag{9b}$$

$$E[y_1(n)] = x(n)\left(1+\mu_{0,1}\right) + \mu_{1,1}, \tag{9c}$$

$$E[y_1(n+k)] = x(n+k)\left(1+\mu_{0,1}\right) + \mu_{1,1}, \tag{9d}$$

where the $\mu_{0,i}$ and $\mu_{1,i}$ is the parameter in the ith sub-DACs corresponding to e_0 and e_1 in (3a) and (3b).

Based on the definition in [40], the time-average cross-correlation between output and channel mismatch is:

$$\bar{R}_{y,\varepsilon}(k) = \lim_{P\to\infty}\frac{1}{P}\sum_{n=1}^{P} R_{y,\varepsilon}(n,k). \tag{10}$$

Substituting (7), (8), (9) into (10), collecting the terms gives

$$\bar{R}_{y,\varepsilon}(k) = \frac{1}{2}\left[\bar{R}_{y_1,y_1}(k) - \bar{R}_{y_2,y_2}(k)\right]. \tag{11}$$

Substituting (1) into (11), collecting the terms gives

$$\bar{R}_{y,\varepsilon}(k) = \frac{1}{2}\left[(\alpha_{DAC1}-\alpha_{DAC2})\bar{R}_{xx}(k) + \left(\bar{\beta}_{DAC1}-\bar{\beta}_{DAC2}\right) + \left(\bar{\sigma}^2_{DAC1}-\bar{\sigma}^2_{DAC2}\right)\delta(k)\right]. \tag{12}$$

Using the definition in (2)–(4), letting e_{l_i} be zero and letting $\delta_{k,i}$ represents the ith current mismatch in the kth sub-DAC channel, we can get this conclusion that when the mismatch of each sub-DACs meets the requirement as follows:

$$\sum_{i=1}^{N}\delta_{1,i} = \sum_{i=1}^{N}\delta_{2,i}, \tag{13a}$$

$$\sum_{i=1}^{N}\left(\delta_{1,i}\right)^2 = \sum_{i=1}^{N}\left(\delta_{2,i}\right)^2, \tag{13b}$$

the time-average cross-correlation between output and channel mismatch is zero, which, in the theory of random process, means that the output is independent of channel mismatch and the image tone is randomized into noise. The analysis above reveals that to ensure the effectiveness of channel mismatch randomization, the physical location of two corresponding current sources, $\delta_{1,i}$ and $\delta_{2,i}$ from two sub-DACs, should be as close as possible. In this way, the gradient mismatch will have less impact on (13a).

3.2 Numerical simulation

As analyzed in the previous subsection, when the two unary-decoded sub-DACs in TRI-DEMRZ meet the requirement in (13), i.e. the same mean value and power of the current source mismatch in each sub-DAC, the image tone due to the channel mismatch can be completely eliminated. In practical, considering inevitable variations and also widely used layout techniques like common-centroid layout schemes in [41] for mismatch control, we have analyzed the impact of a certain amount of deviation from the requirement in (13). Numerical simulation results are provided in Fig. 5, in which the normalized power of the image tone due to different amounts of deviation in (13) is compared between TRI-DEMRZ and conventional interleaving DAC without DEM. In Fig. 5, thirteen pairs of current sources are randomly generated using MATLAB normal distribution generation function "*normrnd*" with different mean and standard deviation to simulate the deviation in (13). For each sample, the arithmetic sum deviation is the absolute value of the deviation in (13a) which is normalized to one LSB:

$$\left|\sum_{i=1}^{N}\delta_{1,i} - \sum_{i=1}^{N}\delta_{2,i}\right| / 1LSB, \tag{14a}$$

while the quadratic sum deviation in (13b) is:

$$\left|\sum_{i=1}^{N}\left(\delta_{1,i}\right)^2 - \sum_{i=1}^{N}\left(\delta_{2,i}\right)^2\right| / (1LSB)^2. \tag{14b}$$

For example, the 11th sample in Fig. 5 has normalized arithmetic sum deviation near 2LSB while the quadratic sum deviation is around 10LSB^2 and for the 4th sample, they are near zero LSB and 10LSB^2 separately.

Sample 1 to 4 in Fig. 5 confirm that TRI-DEMRZ is insensitive to the quadratic sum deviation and shows 10–20 dBc image suppression compared with the interleaving without DEM. It means that the value of (14b) has a few influence in the performance of TRI-DEMRZ in channel mismatch randomization as depicted in Fig. 6(a).

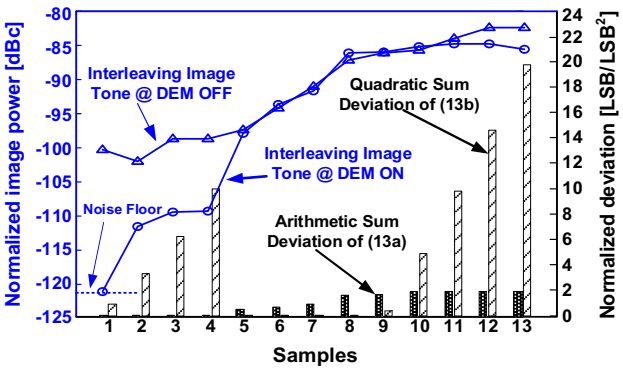


Fig. 5 Image tone power versus channel mismatch deviation in interleaving DAC with DEM ON and OFF. For each samples the image tone is normalized to signal power, which is 0 dBm, while the corresponding deviation is normalized to LSB for arithmetic sum deviation and LSB^2 for quadratic sum deviation

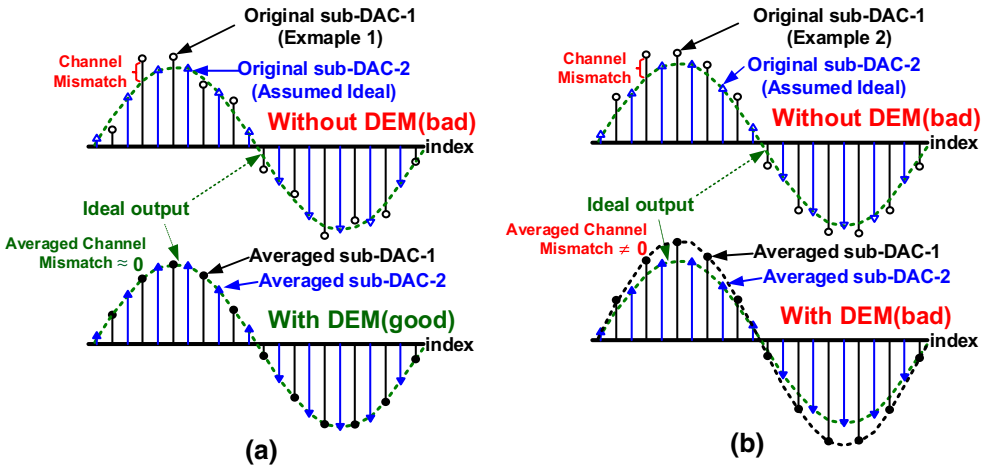


Fig. 6 The conversion difference in interleaving with and without DEM in mismatch distribution example 1 (**a**) and example 2 (**b**)

However, sample 5 to 8 reveal that there is more critical requirement in (14a) to guarantee the performance of TRI-DEMRZ. This is reasonable that when there is obvious mean value deviation in (14a), even under the time average of DEM, the offset between each sub-DACs still exists as depicted in Fig. 6(b). In those cases, if the gradient channel mismatches are all positive or negative, the averaged channel mismatch is larger than that of interleaving without DEM at low amplitude, which may make the image tone worse for TRI-DEMRZ, as shown in sample 8 and sample 10. From sample 9 to sample 13, where the arithmetic sum deviation keeps almost the same and the quadratic sum deviation increases, the image tone of interleaving without DEM deteriorates worse, which again proves the advantages of incorporating DEM with interleaving.

In summary, TRI-DEMRZ incorporating DEM and interleaving not only improves the linearity of each sub-DACs, but also suppresses the image tone caused by channel mismatch in interleaving. Besides, the simulation above emphasizes the importance of (13a) in the design of DAC using TRI-DEMRZ.

4 Implementation and experiment

This section provides the implementation of TRI-DEMRZ and the experimental results of the fabricated experimental DAC.

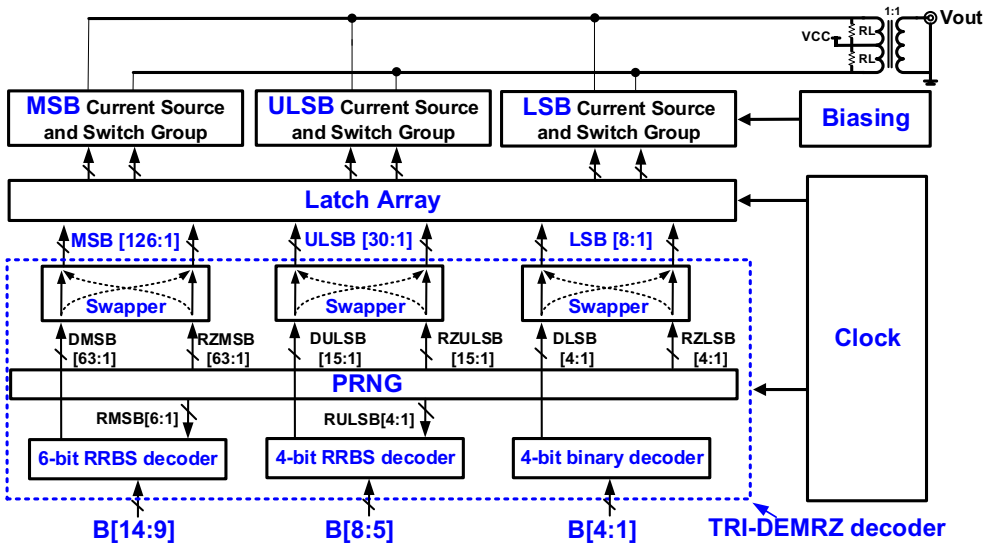
4.1 Chip implementation

To verify the effectiveness of TRI-DEMRZ, a 14-bit 500-MS/s current-steering DAC in 65 nm CMOS was implemented. The DAC structure is shown in Fig. 7(a), including a current source and switch array, a latch array, a TRI-DEMRZ decoder, and a clock generator. The DAC is segmented into 6B + 4B + 4B. This DAC has 1.2 V digital power supply and 2.5 V for the current source and switch arrays. The full-scale current output is 32 mA and the differential AC load is 50 Ω. The chip photograph of the fabricated DAC is shown in Fig. 7(b). The active area is 0.42 mm^2, and the entire chip outline is 1.9 mm × 1.1 mm.

The complementary switched current source (CSCS) depicted in Fig. 8 is employed for the MSB and ULSB segments to reduce the code-dependent load variations caused by the finite output impedance [3, 4]. Considering the output impedance of LSB branches is not the main bottleneck, CSCS is not applied to the LSB segment. For an MSB CSCS unit, the main current I0 is 320 μA and the complementary current I0' is 64 μA, forming a differential output of 256 μA. In ULSB, the main current and the complementary current are 32 μA and 16 μA, respectively, forming a differential output of 16 μA. Both MSB and ULSB are based on the same 16 μA current source unit for matching performance. Another 16 μA current unit is split into 16 unary smaller current sources and 15 of them are used to implement the four LSBs, and the rest one as dummy. As discussed in Section "Static mismatches and switching distortions", with the DEM technique to mitigate the impact of transistor mismatches, a smaller transistor size of 4.8 μm width and 4.5 μm length is adopted for an MSB current source unit. Such sizing provides 90% integral nonlinearity (INL) yield without DEM. The cascade current source transistors, the switches, as well as the top cascoded transistors, are implemented with the shortest gate length to reduce the parasitic capacitance. A smaller transistor size also helps to reduce the timing errors in the switching driving circuitry and the output current tree.

A linear feedback shift register (LFSR) is used as PRNG, and a random rotation-based binary-weighted selection (RRBS) scheme in [42] is employed for the DEM decoder.

For the sub-DAC which returns to zero, the PRNG randomly selects 32 MSB current sources and 15 ULSB



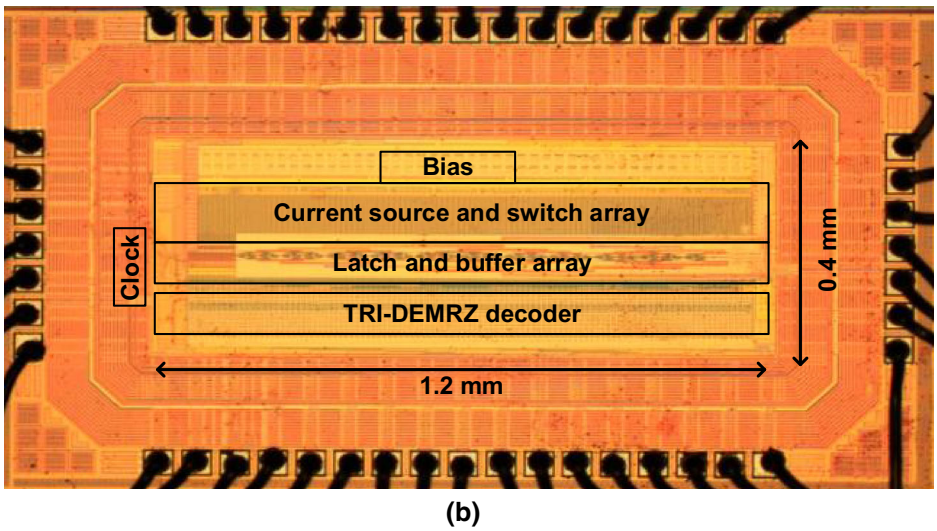


Fig. 7 Chip implementation **a** the structure of this 14-bit DAC with TRI-DEMRZ and **b** micrograph of the fabricated 14-bit DAC using 65 nm process

current sources to the DAC's positive output port and the remaining current sources in MSB and ULSB to the negative output port. Through this way, the differential output of this sub DAC is almost zero with a DC offset of only one LSB which has very little impact on the dynamic performance and is negligible in most applications because this DC offset is isolated by the transformer used for AC differential-to-single conversion [3].

For the sub-DAC which performs the net output according the digital input, the RRBS shown in Fig. 9 is used to implement the DEM decoder. A 3-bit RRBS full decoder implementation example is illustrated in Fig. 9(a) [42]. A 4-bit RRBS full decoder could also be implemented in the same way. The ULSB DEM decoder in this DAC is such a 4-bit RRBS full decoder. To avoid excessively long routing distance and complexity, the construction of the 6-bit MSB RRBS decoder is simplified by reusing the 4-bit RRBS decoder and properly arrange the connection, as illustrated in Fig. 9(b).

4.2 Measurement results

Figure 10 shows the measured INL performance. With TRI-DEMRZ disabled, the DAC operates with only one sub-DAC responding to the input digits in a binary-weighted switching pattern. The measured INL is + 5/− 7 LSB, as shown in Fig. 10(a). The average INL is also measured with TRI-DEMRZ on. Due to the complexity of measurement, in this case, only the MSB segment was measured. As shown in Fig. 10(b), it is reduced

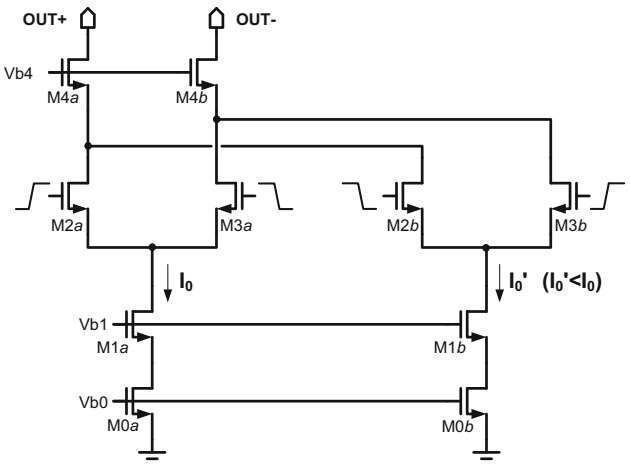


Fig. 8 The CSCS unit [3, 4]

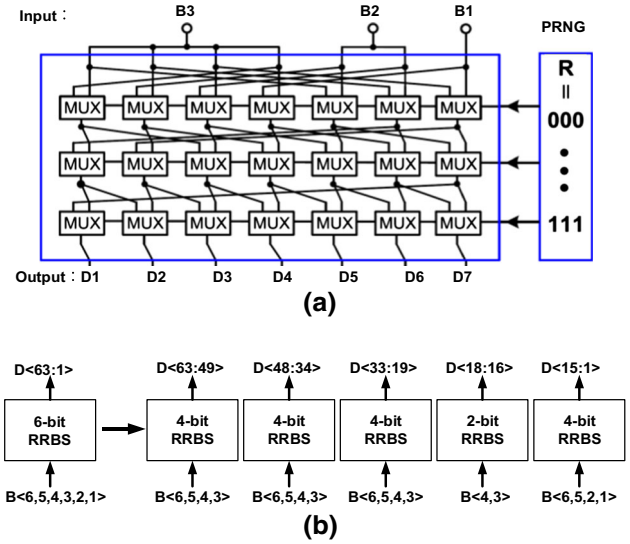


Fig. 9 The structure of a 3-bit RRBS in (**a**) and a simplified 6-bit RRBS in (**b**) implemented with four 4-bit RRBS and one 2-bit RRBS [4]

significantly to only + 1.2/− 1.2 LSB after 500 cycles of DEM randomization, which proves the effectiveness of the DEM decoder.

Figure 11(a), (b) shows the measured output spectra at a 250-MS/s sampling rate with TRI-DEMRZ disabled. The measured SFDR is 70.4 dB at 5.8 MHz and 61.0 dB at 122 MHz, as shown in Fig. 11(a), (b), respectively. When the TRI-DEMRZ is on, the harmonic is suppressed and the SFDR reaches 90.0 dB at 5.8 MHz and 79.2 dB at 122 MHz, as shown in Fig. 11(c), (d), respectively. Such improvement is brought by the TRI-DEMRZ method with signal-independent switching and channel mismatch randomization. At low signal frequencies, the SFDR is mainly determined by the matching property of the current sources and interleaving channels, and TRI-DEMRZ is able to

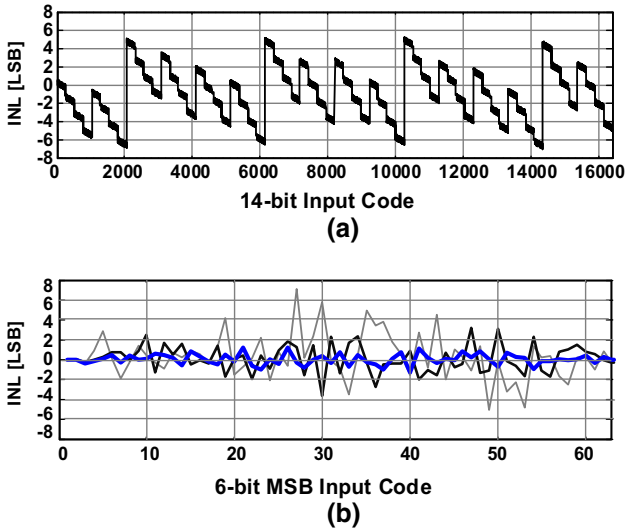


Fig. 10 The measured INL curves in (**a**) with 14-bit full-range input code, and the average INL curves in (**b**) of the 6-bit MSB with TRI-DEMRZ on for 30 (gray), 80 (black), and 500 (blue) clock samples (Color figure online)

effectively average out most current source mismatches, leading to a higher SFDR. At a higher frequency, although the static mismatch averaging improvement is less, TRI-DEMRZ is able to significantly reduce the distortions induced by the code-dependent switching glitches, which dominate the SFDR at a high frequency. Figure 12 plots the measured SFDR versus the signal frequency at 250-MS/s and 500-MS/s. At 250-MS/s, the observed SFDR improvement within the entire Nyquist band varies from 11.5 dB to more than 20.0 dB. At 500-MS/s, this DAC reaches more than 70 dB SFDR within 211 MHz band. It is noted that, at 500-MS/s, the SFDR with TRI-DEMRZ turned on at around 40 MHz is lower than adjacent measurement results in Fig. 12. While similar phenomena and explanations can be found in both literature and products [2, 3, 43], here it may be caused by the signal integrity problem at the DAC input interface. The experimental measurement setup utilizes a single-ended full-swing CMOS parallel interface, and the alignment of the parallel input digital bits is thus very critical for a lower bit error rate. As we experience in the experiments, slightly adjusting the delay of some digital input bits can affect the harmonic tones significantly. While a number of delay settings have been applied in the experiments, the alignment may still be not satisfactory for the measurement around 40 MHz in Fig. 12.

Table 2 provides a summary of the performance of the fabricated DAC. Table 3 compares the performance of the fabricated DAC with the state-of-the-art designs. Although the SFDR of this work is lower than [44], the savings from not using the oversampling rate and off-chip calibration

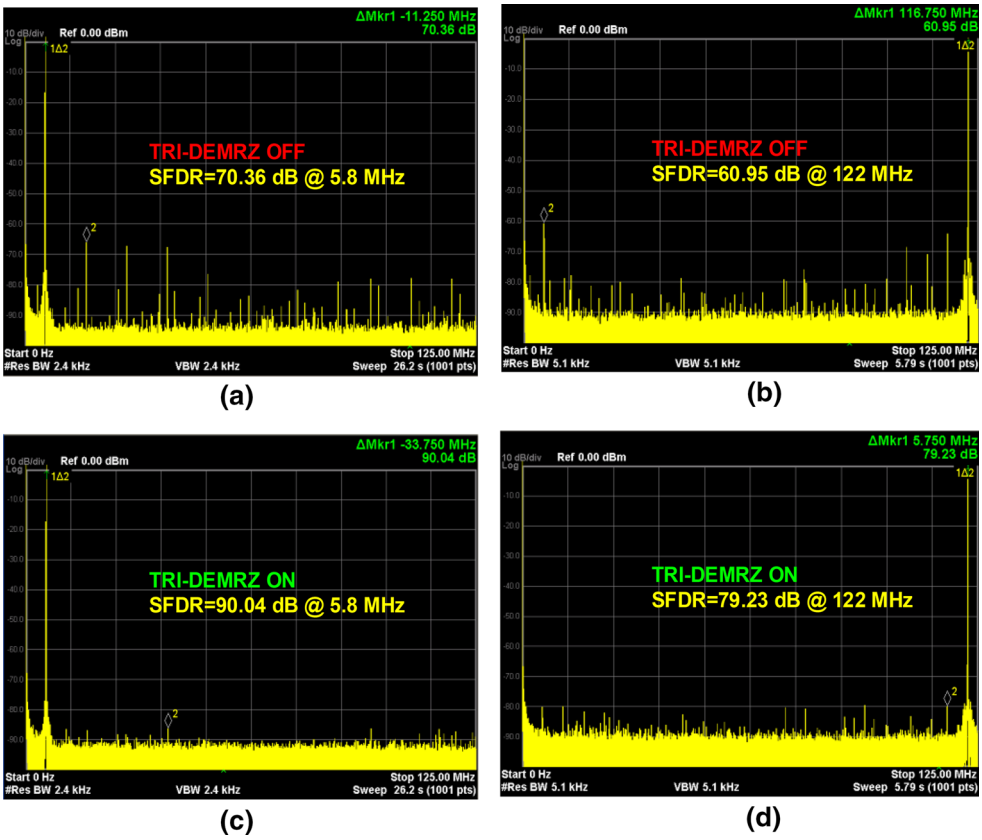


Fig. 11 The measured output spectrum at 250 MS/s with TRI-DEMRZ disabled in (**a**, **b**), and TRI-DEMRZ enabled in (**c**, **d**)

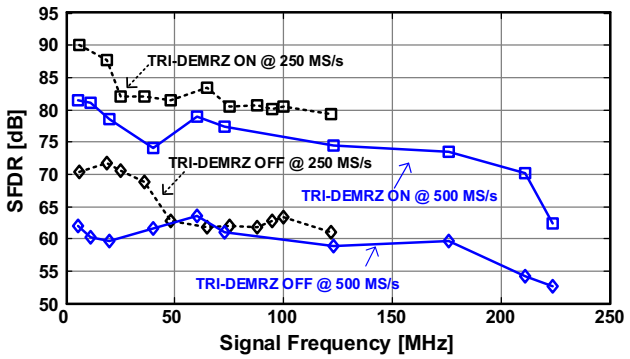


Fig. 12 The measured SFDR versus the signal frequency when TRI-DEMRZ enabled and disabled

Table 2 Measured performance of the proposed TRI-DEMRZ DAC

Technology	CMOS 65 nm
Resolution	14 bits
Clock rate	500MS/s
SFDR	> 70 dB within 211 MHz
INL	+ 5/− 7 LSB
Supply voltage	1.2 V/2.5 V
Power consumption	106 mW
Active area	0.42 mm^2

techniques reduce the complexity and make a wideband DAC design less challenging. Although the sampling frequency of this work is not as high as other works due to the limitations by the CMOS single-ended I/O signal integrity, in the near-Nyquist band of this design, the SFDR of this DAC is higher than [2, 3, 38]. To the best of the authors' knowledge, this work is the only reported design in literature that achieves 90 dB SFDR without calibration or oversampling techniques. Future work of integrating calibration techniques would potentially enable an even higher SFDR. To evaluate the overall power efficiency of this DAC, the widely used figure-of-merit (FOM) [3] is provided in Table 3. Considering the sampling rate, SFDR at a low signal frequency, SFDR near the Nyquist, the signal power, and the DAC power consumption, the FOM of this DAC is higher than the designs [2, 3, 38] with similar technique in Table 3.

5 Conclusion

This paper has revealed that, other than simply incorporating DMRZ and time-relaxed interleaving, TRI-DEMRZ shows more merits. In addition to mitigating the non-linear distortions caused by code-dependent switching activities,

Table 3 Comparisons with state-of-the-art works

Specifications	This work	[38] JSSC2011	[2] ISSCC2013	[3] TCASI2014	[44] JSSC2016
Technique	TRI-DEMRZ	DRRZ	DMRZ	TRI-DRRZ	Hybrid-DAC
Process (nm)	65	90	40	130	65
Core area (mm^2)	0.42	0.825	0.016	1.20	0.57
Supply (V)	1.2/2.5	1.2/2.5	1.2	1.2/2.5	1/2.5
DAC power (mW)	106	128	40	299	681
Sampling rate (GS/s)	0.25/0.5	1.25	1.6	0.50	2
Resolution (bits)	14	12	12	14	12
Calibration	No	Yes	No	No	Yes
Full-scale current (mA)	32	16	16	16	16
$SFDR_{LF}$ (dB)	90.0[b]	75	74	84.8	98
$SFDR_{fs/2}$ (dB)	79.2[b]	66	70.3	73.5	74.4
FOM (10^4Hz/mW)[a]	47[b]	7.4	46	9.2	83.3

[a]$\mathrm{FOM} = 2^{(\mathrm{SFDR_{LF}}-1.76)/6.02} \times 2^{(\mathrm{SFDR}_{f_s/2}-1.76)/6.02} \times f_s/(P_{\mathrm{DAC}} - P_{\mathrm{sig}})$, where P_{DAC} and P_{sig} are the power of the entire DAC and the output signal, respectively

[b]Measured and calculated @ 0.25 GS/s

TRI-DEMRZ provides an effective method to deal with the channel mismatch in interleaving architectures. The exploration of TRI-DEMRZ has significantly extended the design space of wideband high-SFDR DACs by trading additional randomized switch activities and chip area for a higher SFDR. In addition to the theoretical analysis, a 14-bit 500-MS/s current-steering DAC in 65 nm is implemented. The measured SFDR improvement further verifies the effectiveness of TRI-DEMRZ.

Acknowledgements This work was supported in part by the National High Technology Research and Development Program of China (No. 2013AA014103) and in part by the NSFC under Grant #61720106013 and #61532017.

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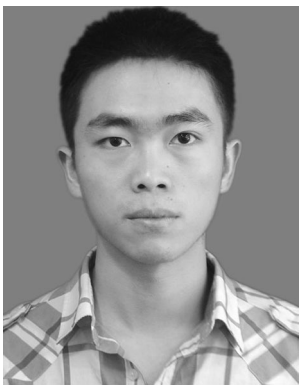

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