Enabling Power-Efficient Designs with III-V Tunnel FETs

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***Abstract* — III-V Tunnel FETs (TFET) possess unique characteristics such as steep slope switching, high g_m/I_{DS}, uni-directional conduction, and low voltage operating capability. These characteristics have the potential to result in energy savings in both digital and analog applications. In this paper, we provide an overview of the power efficient properties of III-V TFETs and designs at the device, circuit and architectural level.**

***Index Terms* — Steep-slope devices, ultra-low power, low-voltage, III-V Tunnel FET (TFET).**

I. Introduction

As technology continues to scale down to the nanometer regime, circuit designers and architects are forced to grapple with problems related to power constraints at various levels of abstraction. The limitation in available power results in a variety of design implications, ranging from reduced battery life in low end mobile processors to increased cooling costs in high performance systems and data centers. Consequently, efforts are being made to realize new power-efficient designs. At the device level, this focuses on new efforts to lower supply voltage by exploring new device architectures and material systems.

Supply voltage scaling in silicon based CMOS transistors has been a significant challenge due to the conflict between the scaling down of threshold voltage for performance and the increased leakage. Enhancements to device architecture such as improved electrostatics using multi-gate devices help to lower supply voltage while retaining the threshold voltage constant. Similarly, III-V materials offer the ability to improve the electron mobility at the same field strength. Recent technology nodes have seen concurrent enhancements in both the device and material systems. However, the switching slope of the CMOS transistors is fundamentally limited to the 60mV/decade swing. This paper focuses on III-V Steep slope Tunnel Field-Effect Transistors (TFETs) that aim at overcoming this limit.

TFET [1, 2] has emerged as a strong candidate for low-energy applications due to its superior energy efficiency arising from the sub-thermal (Sub-kT) switching characteristics at low supply voltages. In addition to the steep switching characteristics, a combination of unique features of TFETs such as asymmetrical source/drain design, and uni-directional conduction provide new opportunities and challenges for analog and digital design.

This paper highlights on how advances in GaSb-InAs (III-V) HTFET design influence circuit and architectural level implementations of digital and analog systems. The rest of the paper is organized as follows: Section II describes the TFET device design and introduces recent progress and modeling efforts. Section III discusses TFET architecture and digital designs for energy efficient systems. Section IV focuses on the TFET advantages for analog systems. Conclusions are followed in Section V.

II. Overview of the Tunnel FET Devices

A. Tunnel FET Device Design

TFETs have become one of the most promising candidates to enable the voltage scaling [1]. Unlike MOSFETs, a TFET is essentially a gated p-i-n tunnel diode with asymmetrical source/drain doping [2]. Benefitting from the band-to-band tunneling (BTBT) induced carrier injection at the source-channel junction, the high energy carriers with an energy slope of kT (where k is the Boltzman constant, T is the absolute temperature) are filtered by a tunneling window, leading to a sub-thermal energy switching slope in TFETs.

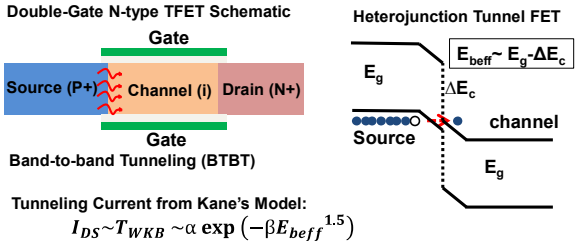

Fig. 1. TFET schematic and band diagram of a hetero-junction TFET for effective tunnel barrier (E_{beff}) reduction.

Recent progress in prototype device and circuit demonstration has shown prominent advantages of TFETs for various energy efficient applications. To outperform CMOS at low supply voltages, the device characteristics such as high on-current at low voltage, high on/off ratio

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and steep sub-threshold swing at room temperature are the key performance aspects of a TFET. Hence, choices of material system and device architecture are critical in TFET design, such as using the hetero-band alignment and low bandgap material to improve the tunneling current, improving the gate electrostatic control from planar to nanowire or ultra-thin body, and reducing defect states to suppress the trap-assisted tunneling [3] (Fig. 1). Knoll et al [4] demonstrated the first strained Si nanowire inverter showing sharp transition at 0.2 V. Considering the low tunneling current of Si TFETs, III-V semiconductor materials offer more freedom of engineering the tunnel junctions and improving the tunneling current [5]. Dewey et al in [6] first explored InGaAs homojunction and heterojunction TFET (HTFET) with improved on-current than Si TFET. Mohata et al [7] demonstrated a MOSFET-like on-current in $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ hetero-junction TFET, by taking advantage of the effective tunneling barrier reduction at the source-channel junction without reducing the band-gap of the channel material, which led to a simultaneous enhancement of the I_{ON} and I_{ON}/I_{OFF} ratio. Later on, a further improvement of on-current of 180 µA/µm has been achieved by Zhou et al [8] in a GaSb-InAs TFET. Recent advancement in complementary TFET process [9, 10] has further highlighted both the performance improvement and process compatibility for TFET technology.

B. Tunnel FET Modeling for Circuit Simulation

To enable the TFET-based circuit designs and system analysis, compact model development is critical for emerging devices. Several works [11, 12] have explored analytical modeling for different designs of TFETs. Zhang et al [11] have developed a compact model of double-gate Si TFET for SPICE simulations, showing good agreement with TCAD simulation. Recently, Lu et al [12] present a continuous semi-empirical model to accurate describe the current-voltage characteristics suitable for both InAs homojunction TFETs and broken-gap AlGaSb/InAs TFETs. Given the variety of TFET designs and lack of mature SPICE models for III-V TFETs, look-up based Verilog-A models derived from atomistic simulation [13] or TCAD [14] have been widely used to explore circuit/architectural designs.

Process variation and electrical noise pose a growing reliability concern for optimal system design for both digital and analog/RF applications at scaled technology nodes, especially due to the preferred low supply voltage operation of TFETs. The process variation for III-V HTFETs has been studied for TFET SRAMs [14] and logics [13]. When variations are considered, the energy savings of III-V HTFET logic gates are slightly reduced,

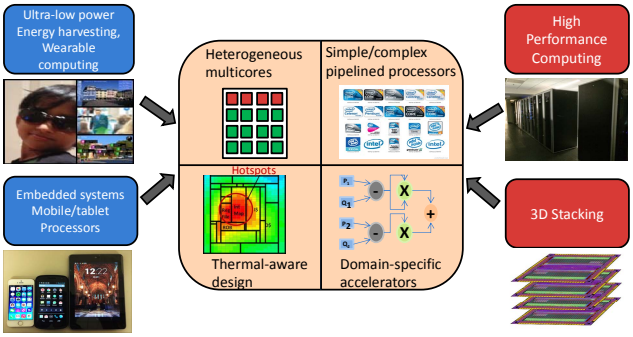

Fig. 2. Design Spaces for Device Heterogeneous Systems.

but still superior compared to CMOS [27]. Moreover, the electrical noise performance has been evaluated in [15] for III-V HTFETs including the flicker, shot and thermal noise. At a nominal operation voltage of 0.3 V, HTFET exhibits a competitive input-referred noise in KHz and MHz frequency range compared to the baseline Si FinFET. When the operating voltage exceeds 0.3 V for a frequency range of 10GHz or higher (RF domain), the input-referred noise of the HTFET increases moderately due to the presence of shot noise.

The progress in TFET modeling for circuit simulation has enabled the circuit-level and architecture-level explorations of the energy efficiency benefits of TFETs, such as TFET digital and analog circuits [16-19], TFET-CMOS heterogonous architecture [20] as well as the TFET standard cell library development [21].

III. Tunnel FET Circuits Exploration

By taking advantage of the unique III-V hetero-junction TFET device characteristics, it is promising to design analog and digital circuits with novel functions and/or superior performance. In the rest of this section, a review of recent reported TFET circuits and applications is provided in comparison with Si FinFET designs.

A. Tunnel FET Digital Logic Design Opportunities

These characteristics of HTFETs can manifest themselves in various system-level design techniques that make this technology attractive across a wide range of application domains. Fig. 2 shows the potential scope of applications domains that would benefit from the adoption of HTFET technology into their design. For instance, heterogeneous CMOS-TFET multicores could be used to optimize a wide range of sequential and parallel workloads. The efficiency of TFET at low voltage makes it highly energy-efficient in executing highly parallel workloads using tens of low-voltage cores operating at low frequencies. Similarly, it is possible to duplicate the performance of a high frequency CMOS processor with

TFET processors of higher micro-architectural complexity by consuming much less power, by simply lowering the operating voltage and frequency. In a similar manner, the lower power density of TFET processors can translate into more effective elimination of temperature hotspots, making them feasible candidates for thermal-aware systems. This aspect would also be useful in state-of-the-art techniques like 3D stacking of processors and memory, where thermal effects are a significant concern. Finally, HTFET designs can also be extremely useful in realizing power-efficient, domain-specific accelerators [20].

Designing the HTFET processors used in the domains stated above require efficiently re-designing constituent digital circuit components present in these processors. Energy-efficient adders, inverters and other combinational logic have been demonstrated in prior efforts [22]. For example, for the energy-delay performance of 32-bit adders, the energy consumed by the HTFET adder is one order less than that of a Si FinFET adder for the requirement of 1 nS delay.

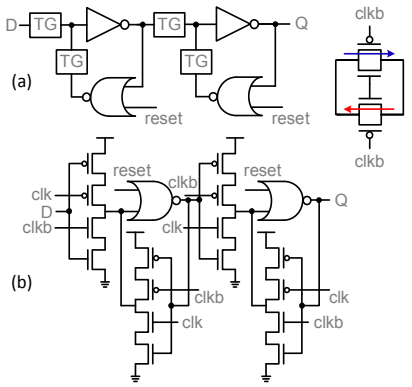

Fig. 3. (a) TG (transmission gates) flip-flop and (b) C^2MOS flip-flop.

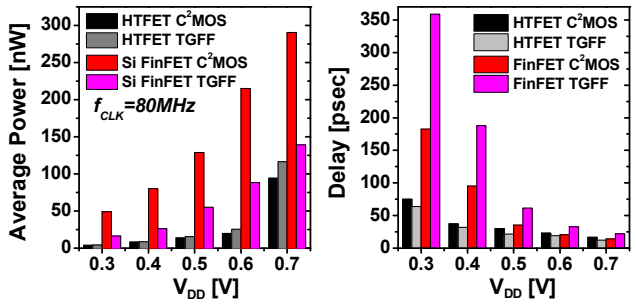

Fig. 4. (a) Average power consumption, and (b) delay of C^2MOS and double TGs flip-flops at 0.3-0.7 V.

Flip-flop is a key component in digital circuits. In [17], the energy efficiency and performance of TFET flip-flop designs are discussed, where HTFET flip-flops reduce 2.5 times power consumption compared with the Si FinFET designs. Fig. 4 shows the average power consumption and delay performance for two types of the popular master/slave flip-flop topologies with an additional port (reset) at various supply voltage ranges. From the simulation results, HTFET flip-flops shows the high power-efficiency and fast transition performance at a power supply lower than 0.5 V due to steep slope switching.

B. Tunnel FET Analog Circuits Design Opportunities

One unique feature of TFET is the uni-directional conduction ability, which turns out to be useful in applications like charge pumps where the TFET are working as switches. Fig. 5 shows a widely-used conventional switch design using one single MOSFET. When the switch is turned on, current could flow from either terminal of the switch to the other, with the current direction depending on the terminal voltage. When the MOSFET in Fig. 5 is replaced by a TFET, this bidirectional current conduction phenomenon is changed to be uni-directional.

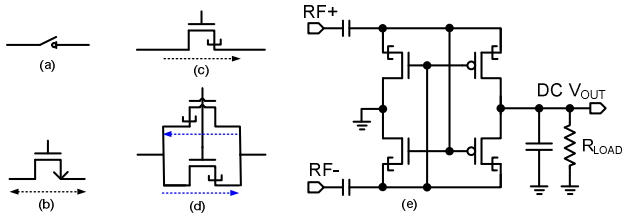

Fig. 5. (a) Ideal On/Off switch; (b) NMOS switch with bidirectional current conduction; (c-d) Uni-directional/bidirectional N-type/2N-type TFET switches; (e) RF rectifier using TFETs.

Fig. 5(e) shows a conventional rectifier topology in which transistors behave as switches [18]. One major power loss that limits the power conversion efficiency (PCE) in CMOS rectifiers is the reverse leakage current. Such leakage current transports the charge at the output towards the input, resulting in significant undesirable output voltage drop and efficiency degradation. In contrast, the reverse leakage could be simply prevented using TFET devices without modifications to the circuit topology. Therefore, the PCE could be improved. Similarly, for conventional DC-DC charge pumps, such bidirectional conduction could also result in reverse leakage current. [23]. In contrast, utilizing TFET in such designs could reduce the reverse leakage current and improve the PCE.

Another feature that contributes to a higher PCE is the steep-slope switching at low input voltage that helps to reduce the turn-on resistance and accordingly, reduce the power loss. As a result, compared with the Si FinFET, the TFET enables both AC-DC conversion and DC-DC conversion under a low input voltage with a higher PCE.

High g_m/I_{DS} helps to achieve high power efficiency in analog designs. In [19], the authors presented a TFET

neural amplifier design employing a telescopic operational trans-conductance amplifier (OTA) for multi-channel bio-signal recording. For such amplifier design, low power to prevent burning the body tissue, high gain and low input-referred noise to sense weak signals are key design specifications. By exploring the high g_m/I_{DS} advantage of TFETs, the neural amplifier exhibited high current efficiency, high voltage gain, and also low input-referred noise. A noise efficiency factor was reduced significantly compared to the theoretical limit of CMOS amplifiers.

With the transistor process scaling and the system application developing, the analog circuits design is becoming challenging [24]. On the one hand, the requirements are more stringent with higher resolution, faster speeds, lower power, and larger dynamic range. On the other hand, the transistors are getting less dependable in terms of matching, voltage range, leakage and reliabilities even if getting faster. Under such circumstances, more and more digital assisted/enhanced techniques are being proposed to compensate these non-idealities, and analog circuits design are becoming more and more "digital". For example, digital calibration is widely used in analog-to-digital converters (ADC) to improve the effective number of bits (ENOB) and signal-to-noise-and-distortion ratio (SNDR) [25]; Pre-distortion could be applied to improve the linearity of power amplifier (PA) and digital-to-analog converters (DAC) [25]; Phase-locked loops (PLL) could even be built nearly digitally [26]. Considering the fact that the advantage of using TFET to build these digital assisting blocks remains, TFETs will be showing more advantages in designing future analog and mixed-signal circuits.

VII. Conclusion

In this paper, new opportunities of using the III-V hetero-junction Tunnel FETs have been reviewed from device, circuits, and system-level perspectives. Progress in III-V Tunnel FET devices can have a significant impact on the landscape of energy-efficient systems.

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