Enabling Power-Efficient Designs With III-V Heterojunction Tunnel FETs

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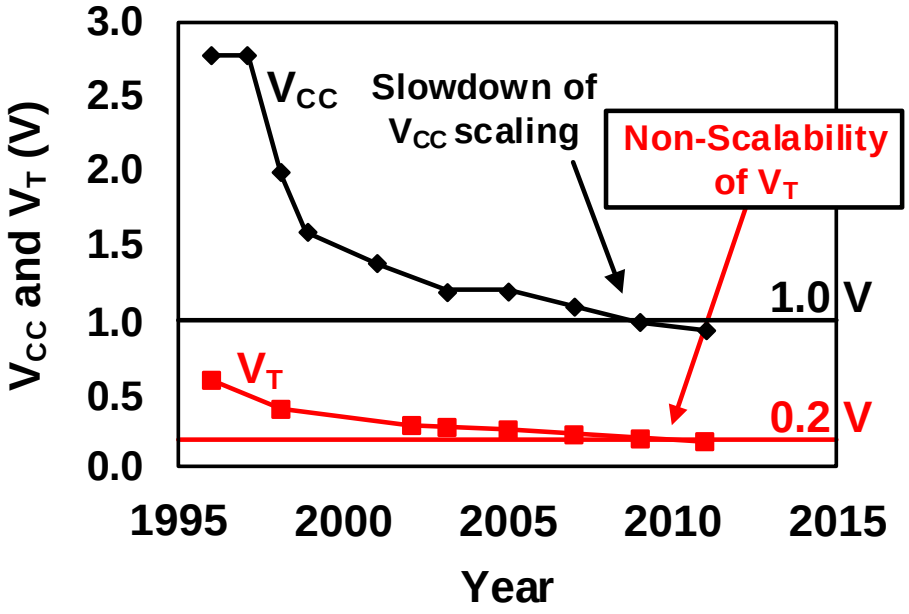
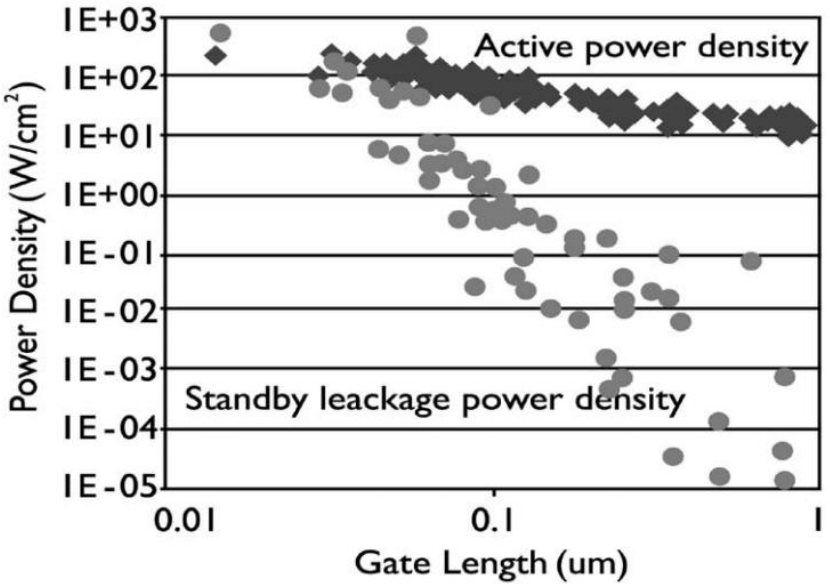
The Pennsylvania State University

Oct 21, 2014

Why TFET? CMOS Scaling Challenge



K. Swaminathan et al, IEEE Micro 2013.



H. Jeon Trans on Instrument and Measurement 2010.

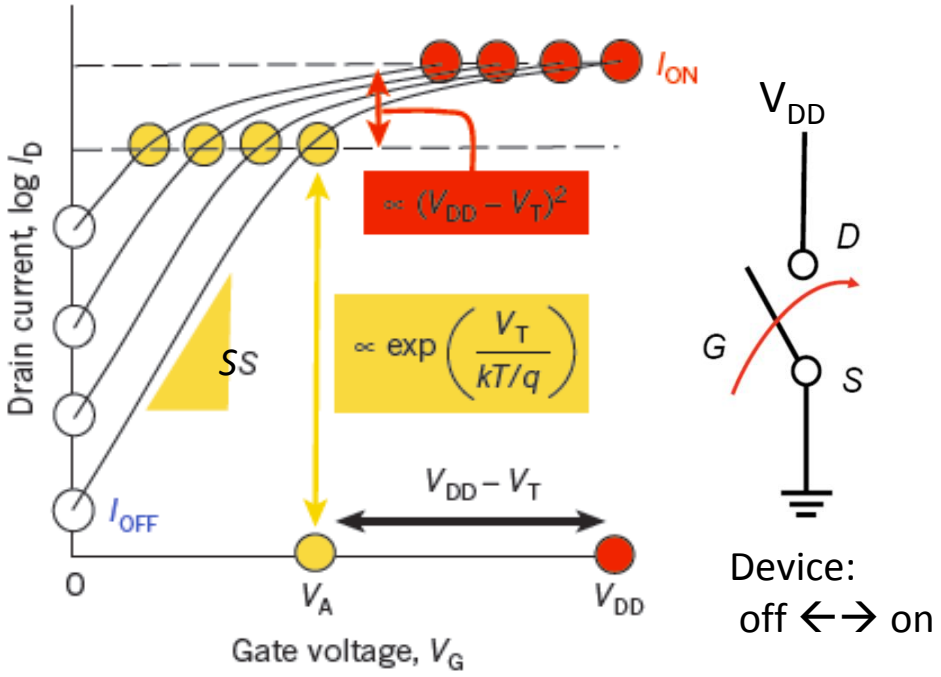
Why TFET? CMOS Scaling Challenge

- **Subthreshold Swing (SS), I_{ON}, and Leakage I_{OFF}**

$$SS = \frac{dV_{GS}}{d(log_{10}I_{DS})} > 60mV/Dec$$

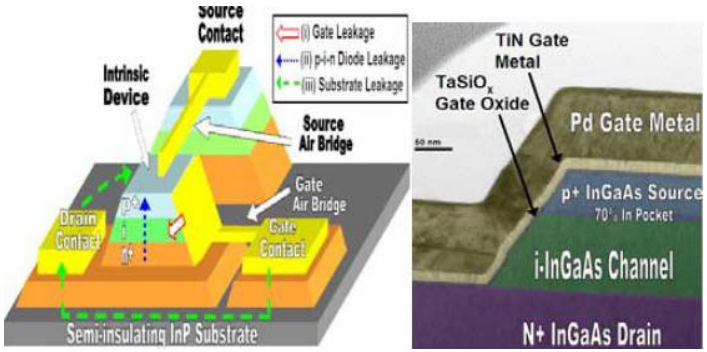
$$E_{tot} = I_{Leak}V_{DD}\tau + C_{eff}{V_{DD}}^2\alpha$$

A. M. Ionescu, H. Riel, Nature 2011.
A. M. Ionescu, IEDM short course 2013.

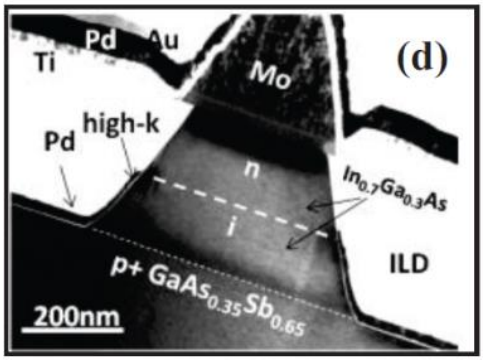


- **Due to 60 mV/dec CMOS SS limit, reducing V_T (so as to reduce VDD for lower power) increases the leakage power significantly;**
- **With a lower SS, Tunnel FETs can operate at a lower VDD and lower power.**

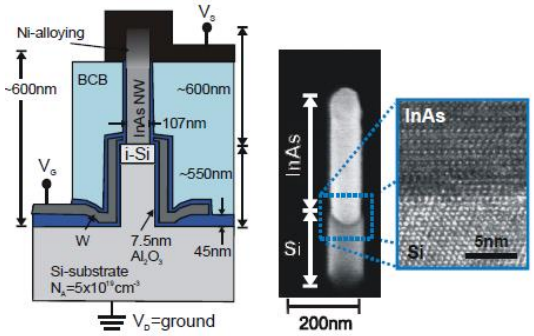
Emerging Tunnel FETs (TFETs)



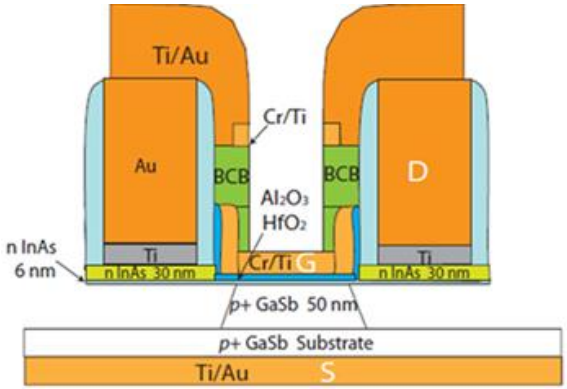
Deway et al., IEDM 11



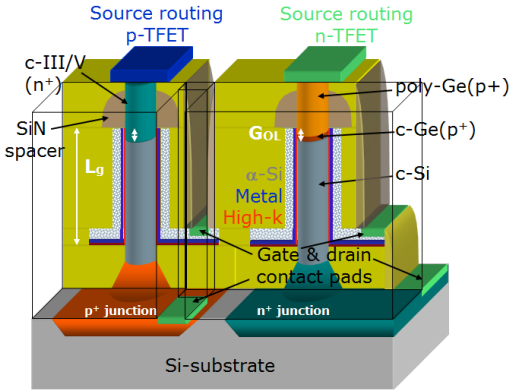
Mohata et al., VLSI 12



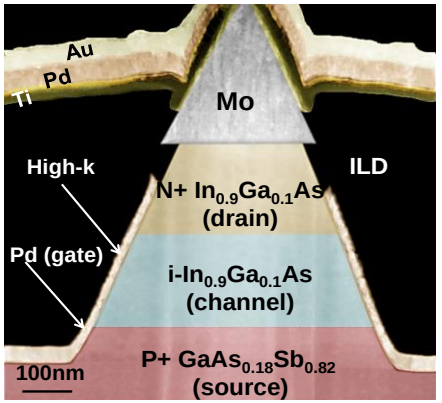
K. Moselund et al., IBM



Xing et al., IEDM 12



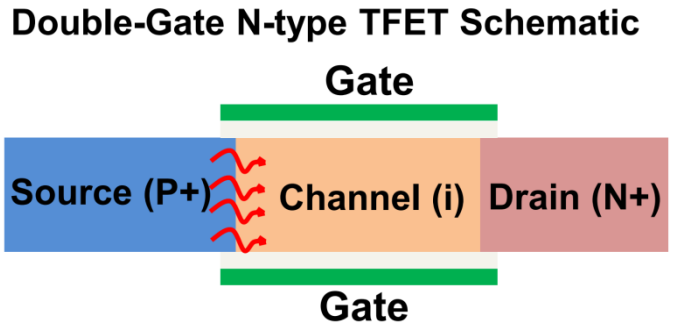
Rooyackers et al., IEDM 13



Bijesh R. et al., *IEDM 13*

A. M. Ionescu, IEDM short course 2013.

III-V GaSb-InAs Heterojunction TFET (HTFET)



- HTFET: High I_{on} and low SS achieved in n- and p- TFET with electrostatic improvement.
- Non-steep subthreshold slope is mainly due to the trap assisted tunneling (TAT) of the source/channel interface states. Further improvement on material interface is required.

V. Narayanan, ISLPED 2013.

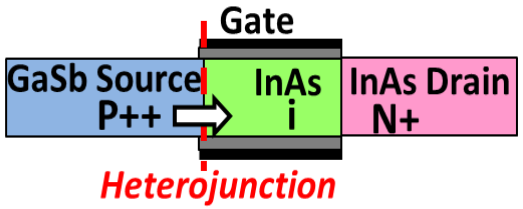
NTFET Ref.	Source-Channel Material	EOT [nm]	I_{ON} [uA/um]	V_{DS} [V]	V_{ON}-V_{OFF} [V]	I_{ON}/I_{OFF}	S_{MIN} [mV/dec]	S_{EFF} [mV/dec]
G. Zhou IEDM 2012	GaSb-InAs	1.3	180	0.5	1.5	6e3	200	400
G. Zhou EDL 2012	InP-InGaAs	1.3	20	0.5	1.75	4.5e5	93	310
Mohata VLSI 2012	GaAsSb-InGaAs	1.75	135	0.5	1.5	1.7e4	230	350
H. Zhao APL 2011	$In_{0.7}Ga_{0.3}As$	1.2	40	0.5	2	2e5	84	380
R. Li EDL 2012	AlGaSb-InAs	1.6	78	0.5	1.5	1.6e3	125	470
G. Dewey IEDM 2011	$In_{0.53}Ga_{0.47}As$	1.1	5	0.3	0.9	7e4	58	190

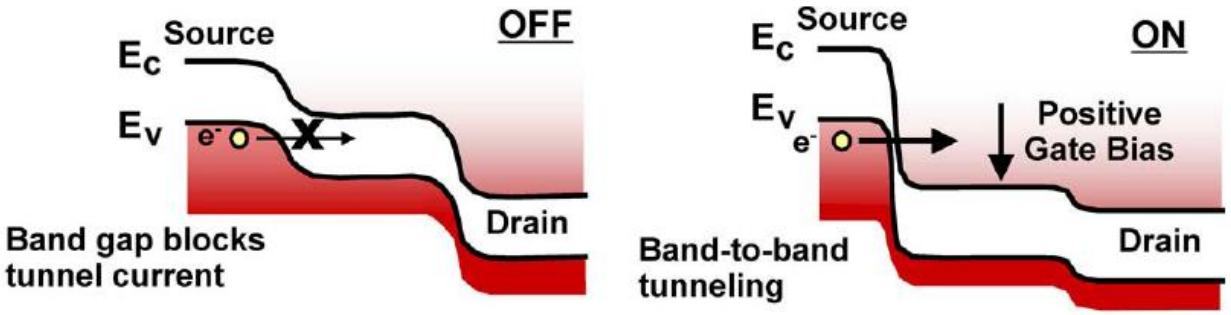
PTFET Ref.	Source-Channel Material	EOT [nm]	I_{ON} [uA/um]	V_{DS} [V]	V_{ON}-V_{OFF} [V]	I_{ON}/I_{OFF}	S_{MIN} [mV/dec]	S_{EFF} [mV/dec]
K. Jeon VLSI 2010	SOI	~0.9	1.2	-1	-1	7e7	32	47
F. Mayer IEDM 2008	GeOI	~2.2	3	-1	-1.5	1.4e2	130	200~300
A. Villalon VLSI 2012	Strained SiGe/SOI	1.25	112	-1	-1.5	3.1e6	33	133
Y. Yang IEDM 2012	$Ge_{0.958}Sn_{0.042}$		4.3	-1	-1	1e2	-	~750
L. Knoll APL 2013	Strained Si Nanowire	2.2	10	-0.5	-1.2	~1e7	90	~120

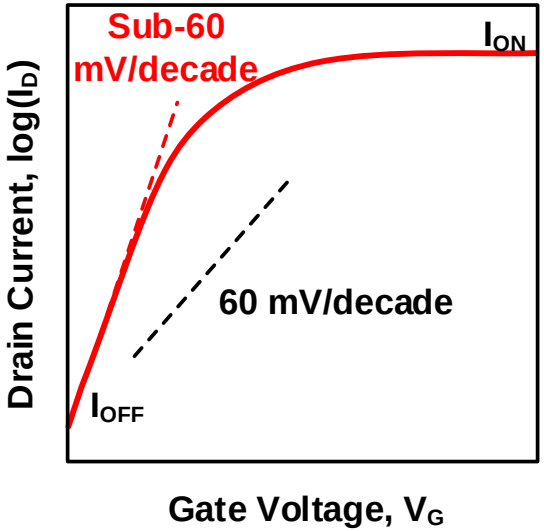
III-V GaSb-InAs Heterojunction TFET (HTFET)

❑ HTFET Structure and Operation

- Essentially a gated reverse-biased p-i-n tunnel diode with asymmetrical source/drain doping;
- Band-to-Band tunneling (BTBT) induced from the sub-thermal switching leads to <60mV/dec SS, more abrupt ON-OFF transition compared to CMOS.



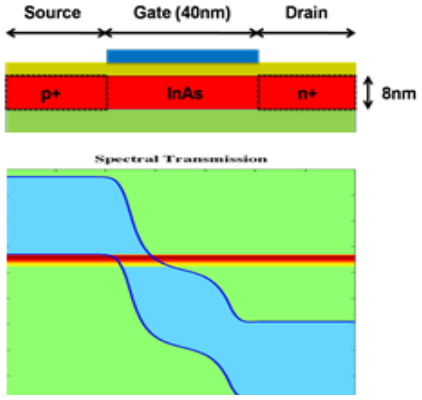




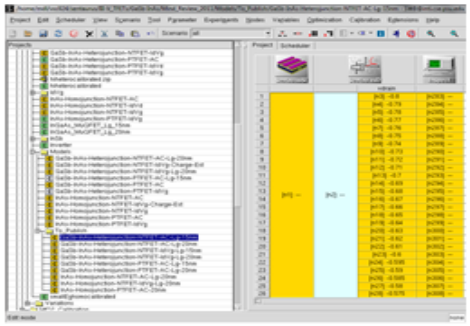
L. Chang IEEE Proceeding 2010; A. Seabaugh et al, IEEE Proc., Nov 2010

Modeling HTFET: Device to Architecture

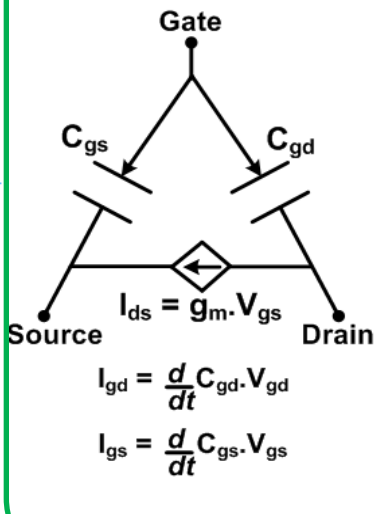
Full band Atomistic simulation (Purdue Nanohub)



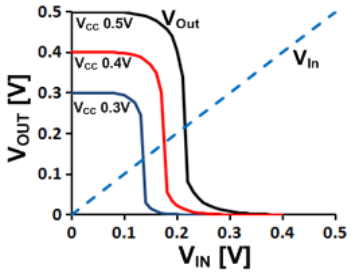
I-V/C-V sweep (experimentally verified)



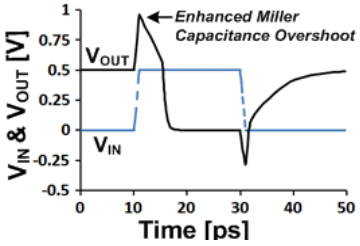
Verilog-A Device Model



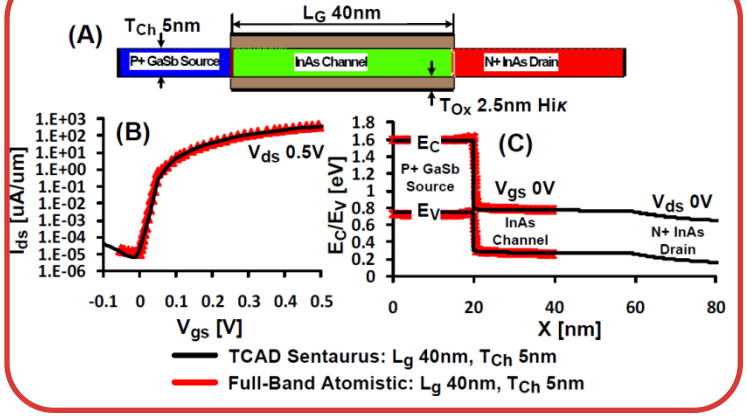
DC Validation



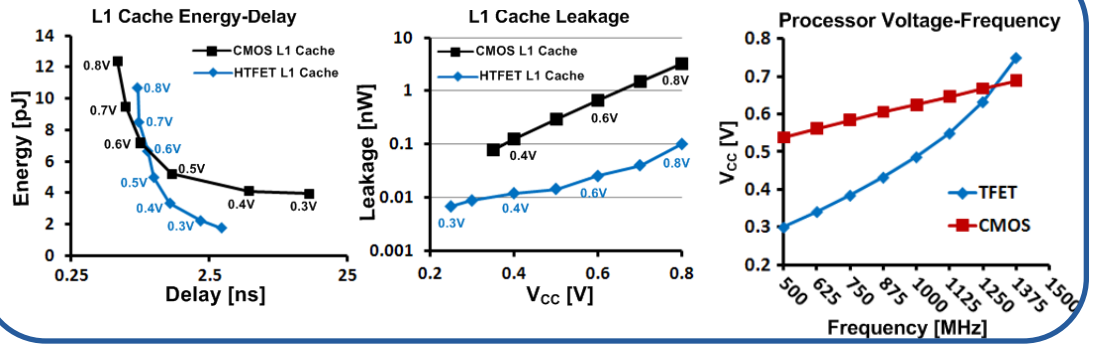
Transient Validation



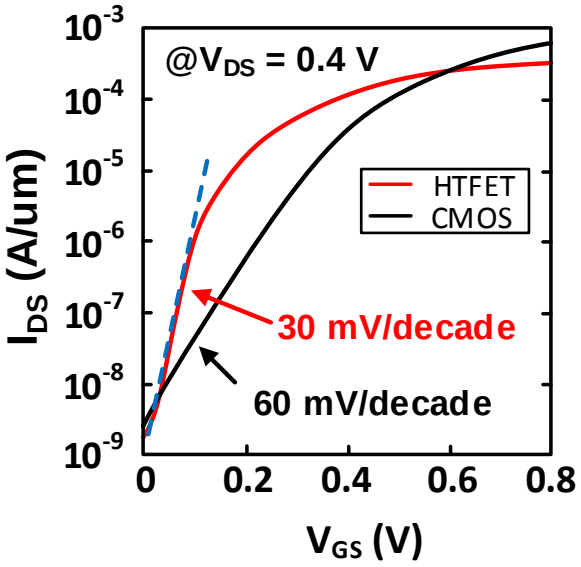
TCAD Model Calibration

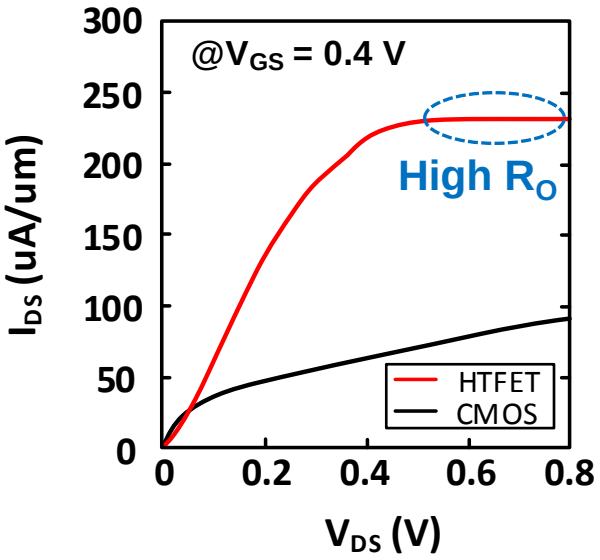


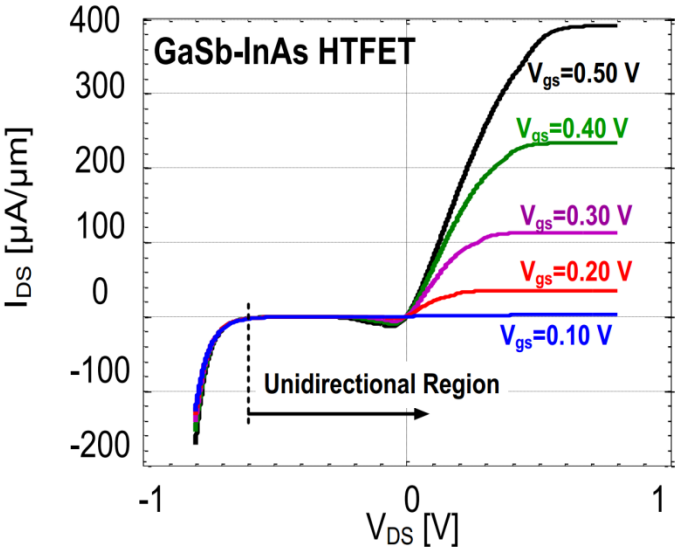
Circuit & Architecture Design



GaSb-InAs TFET Characteristics

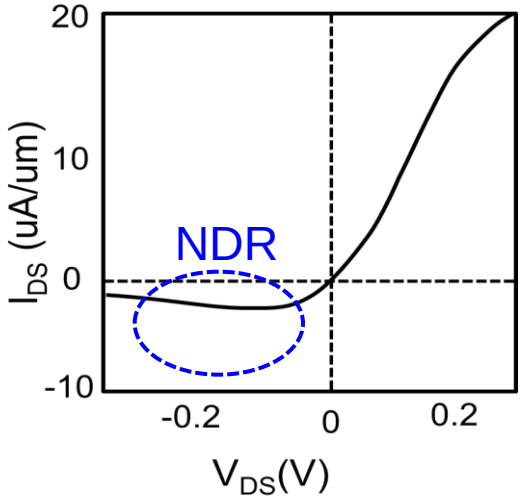






Key Features Observed

- Steep-slope with High I_{on} @ low V_{CC}
- High saturated small-signal R_O
- Uni-directional Tunneling
- Negative differential resistance (NDR)

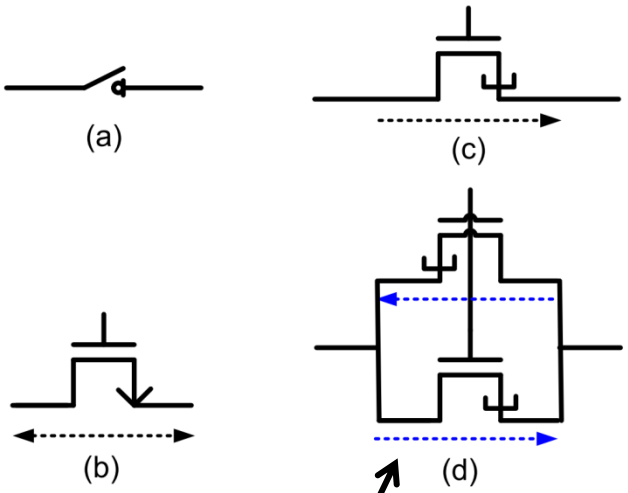


H. Liu et al, ISLPED13

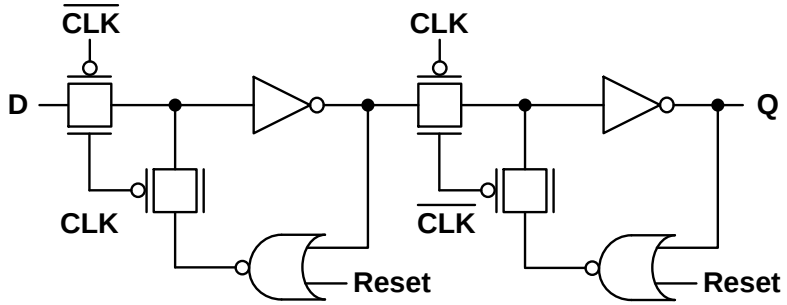
B. Sedighi et al, "A CNN-Inspired Mixed Signal Processor Based on Tunnel Transistors," DATE 2015, submitted

GaSb-InAs TFET Characteristics (cont.)

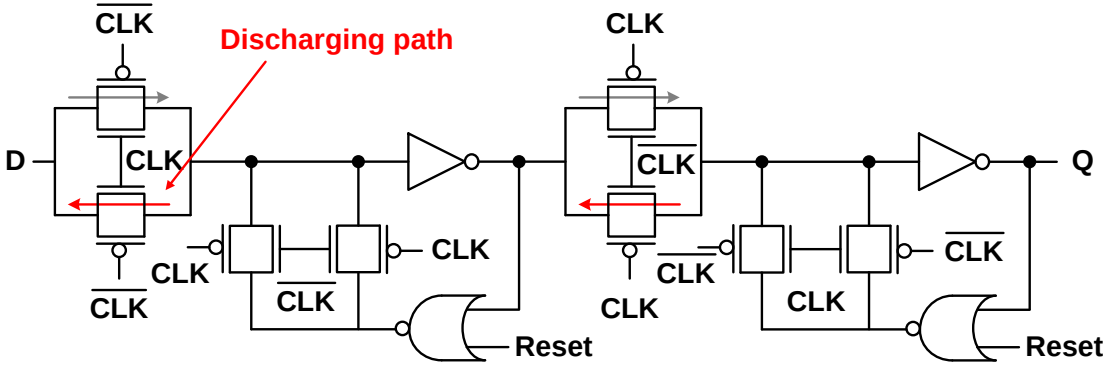
Example of Switch Design Considerations



Additional switch for bidirectional conduction



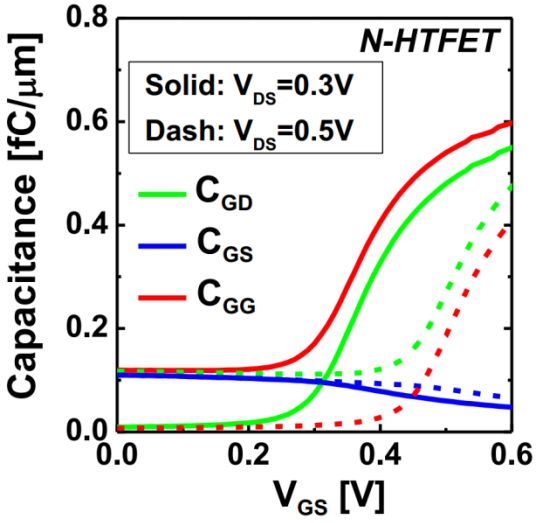
Type 2. Transmission based Si FinFET DFF

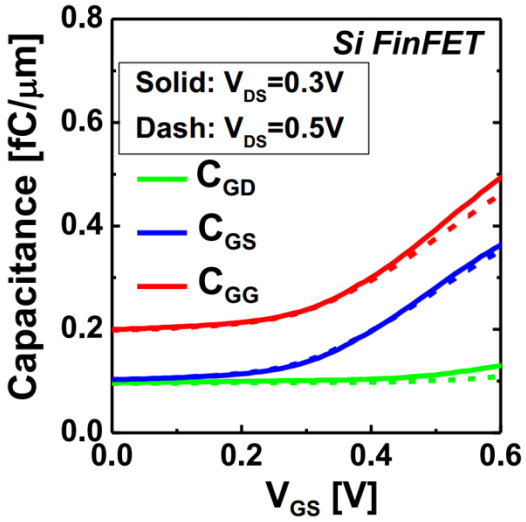


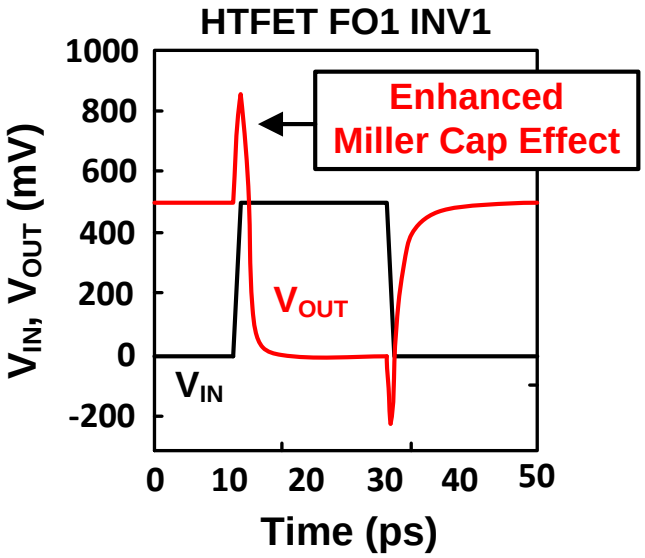
Type 2. Transmission based HTFET DFF

GaSb-InAs TFET Characteristics (cont.)

- Capacitance versus gate voltage
  - Suppressed capacitance (low voltage)
  - Enhanced Miller effect (full voltage)

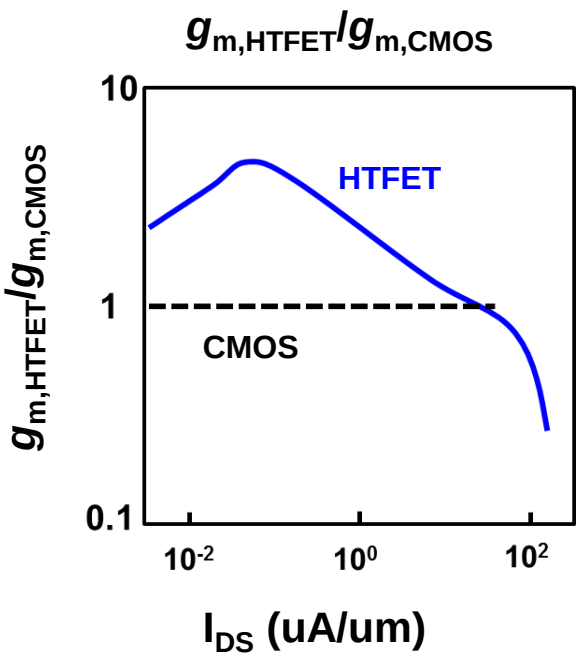


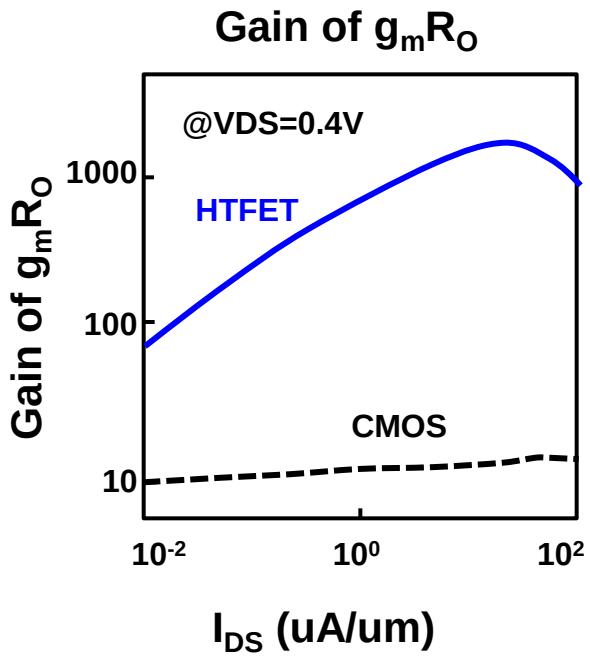


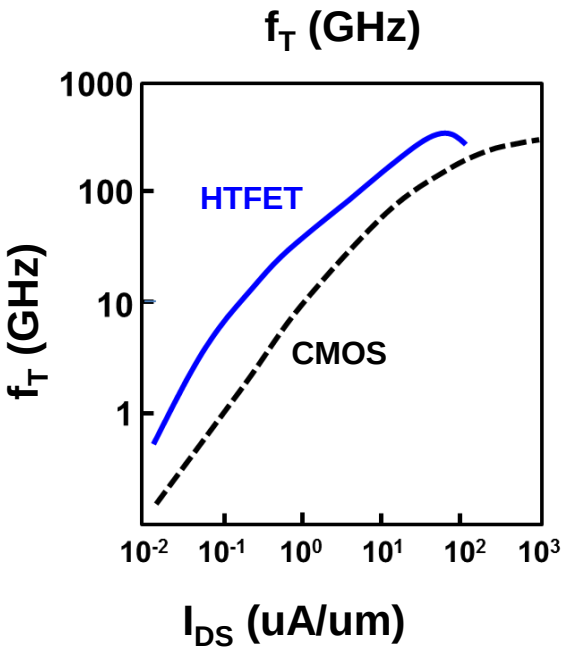


S. Mookerjea et al., EDL 2009.
H. Liu et al., "Tunnel FET RF rectifier design for energy harvesting applications," JETCAS 2014

GaSb-InAs TFET Characteristics (cont.)







- The $g_{m,\ HTFET}$ is significantly larger than $g_{m,CMOS}$ at a low current.
- With larger small-signal Ro, the intrinsic gain is further improved.
- HTFET has >300 GHz while CMOS shows higher f_T at a higher current.
- The peak f_T at a lower current makes HTFET attractive for low-power applications.

B. Sedighi et al., "Analog Circuit Design Using Tunnel-FETs," TCAS-I, to be published

GaSb-InAs TFET Characteristics (cont.)

- Flicker noise is based on carrier number fluctuation

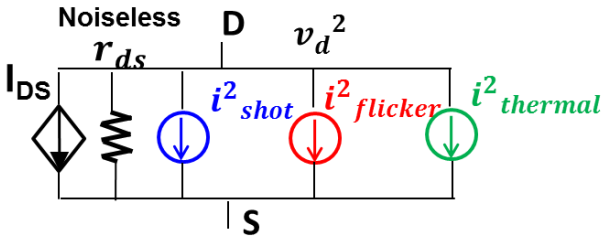
$$\frac{S_{\mathrm{id}}(f)}{I_D^2} = \left(\frac{2}{F} + \frac{B}{F^2}\right)^2 \frac{q^2 N_t(E_{\mathrm{fn}})}{\varepsilon_{\mathrm{ox}}^2 W L' \alpha f}$$

- The shot noise is modeled similar to tunnel diode

$$i_{\mathrm{shot}}^2 = 2q I_D \Gamma$$

- The thermal noise model is similar to the Si-FinFET thermal model

$$\overline{i_{n,thermal}^2} = 4kT\gamma g_m \Delta f$$

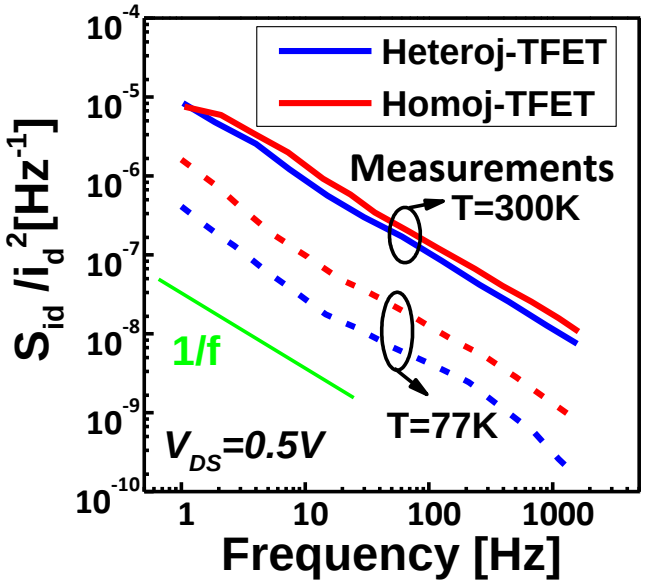


R. Pandey, et al., "Electrical Noise in Heterojunction Interband Tunnel FETs," TED, Feb 2014
K. K. Hung, et al., "A physics-based MOSFET noise model for circuit simulators," TED, May 1990.

GaSb-InAs TFET Characteristics (cont.)

◆ Tunnel FET Flicker Noise (interface traps)

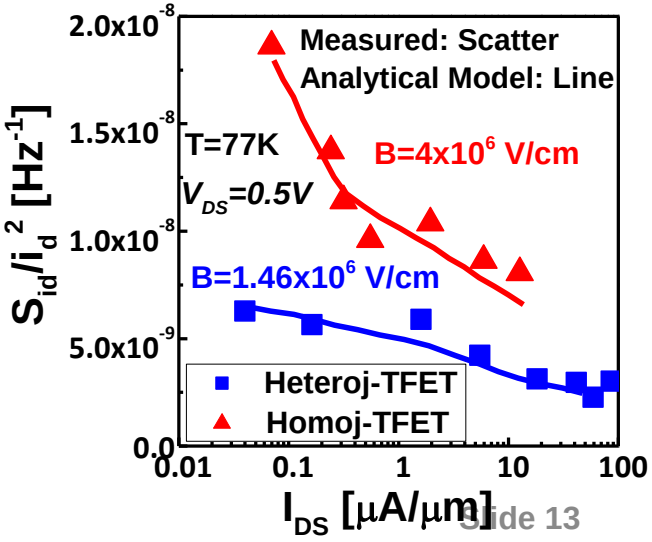
TFET flicker noise highly depends on the spreading of the tunneled carriers in the channel (L'), which is independent of the channel-length (L_g)



TFET Drain Current Flicker Noise Power Analytical Model:

$$\frac{S_{id}(f)}{I_D^2} = \left(\frac{2}{F} + B\frac{B}{F^2}\right)^2 \frac{q^2 N_t(E_{fn})}{\varepsilon_{ox}^2 W L' \alpha f}$$

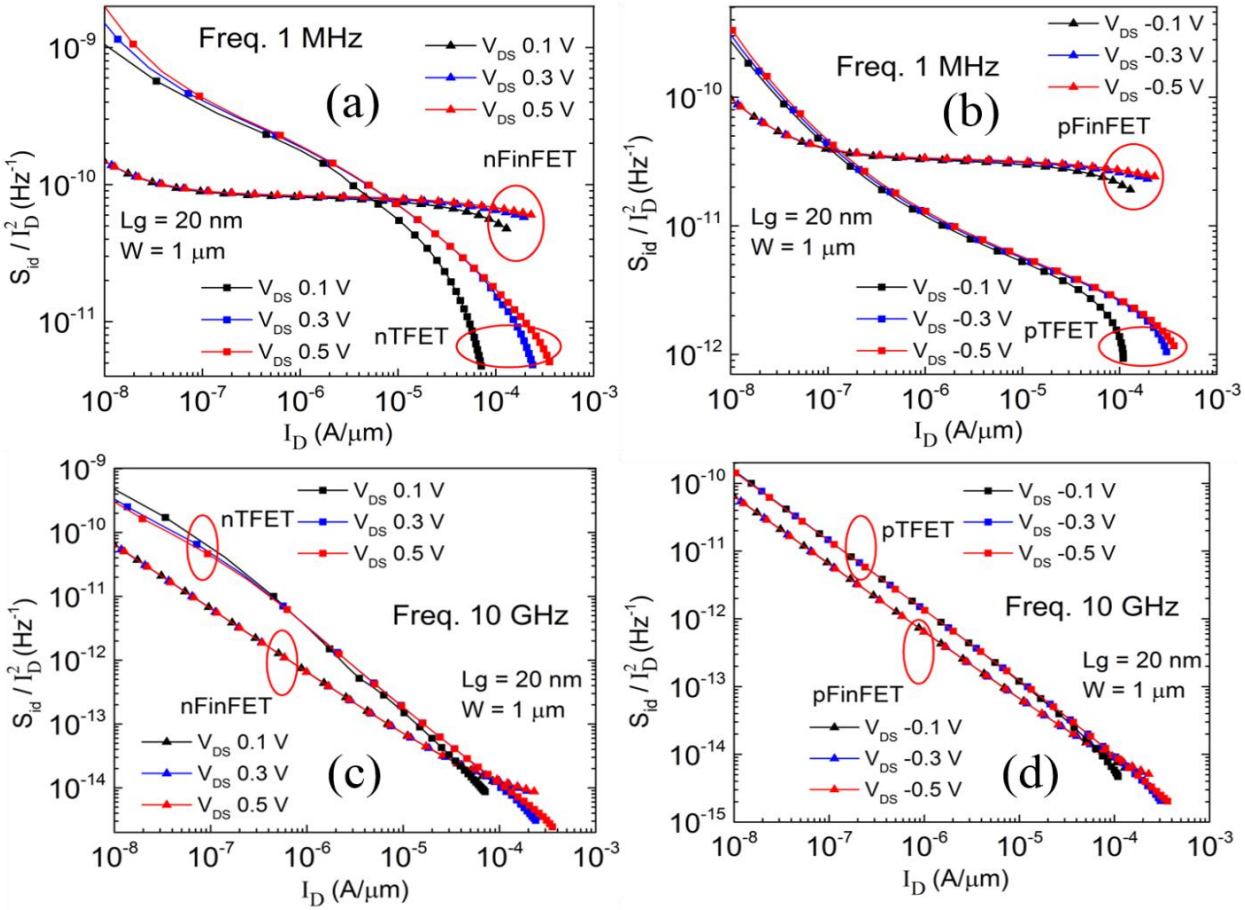
B is Kane's model paraemter, f is frequency, W is the device width, α is the attenuation factor, N_t is the interface trap density, F is the electrical field.



Bijesh, R., et al, DRC 2012.
Rahul, P., et al, TED 2014.

GaSb-InAs TFET Characteristics (cont.)

Overall Electrical Noise: HTFETs vs Si FinFETs

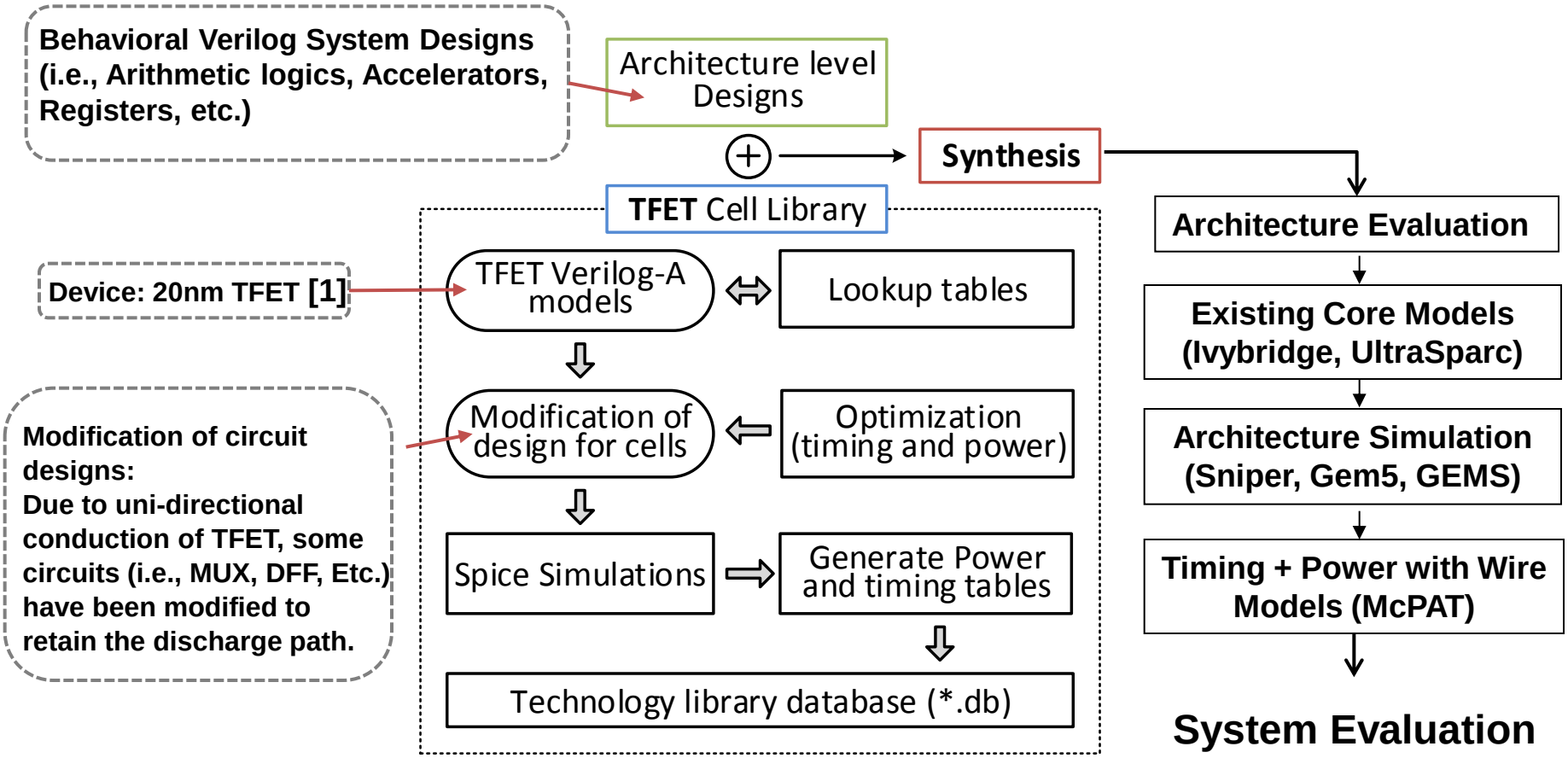


- A larger noise of HTFET at low I_D is due to the smaller tunneling length of carriers.
- HTFET noise reduces faster is due to faster carrier density increase.
- **Competitive device noise**
- **Lower input-referred noise for HTFET with high gains**

Ref: Rahul, P., et al, TED 2014.

HTFET Standard Cell Library

- Standard Cell Library Design Flow Enables quick evaluation of large-scale digital circuits.



K. Swaminathan et al, DAC2014.

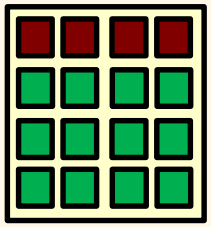
Potential Design Space By TFETs

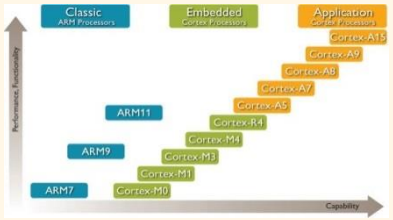
Ultra Low power Energy Harvesting, Wearable Computing

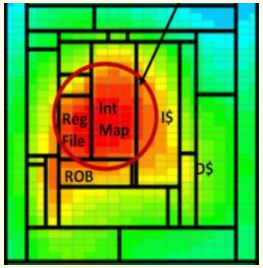
Low power/ Embedded Systems Mobile/Tablet Processors

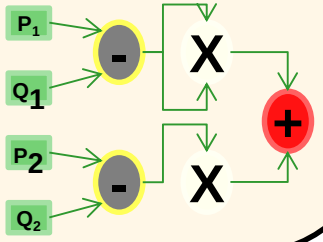
Architectural Innovation

Heterogeneous multicores	Simple/complex pipelined processors
Thermal-aware design Hotspots	Domain-specific accelerators



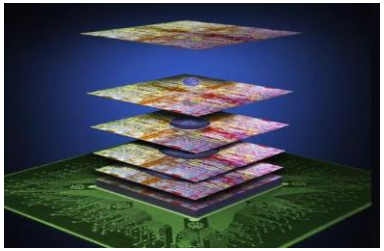




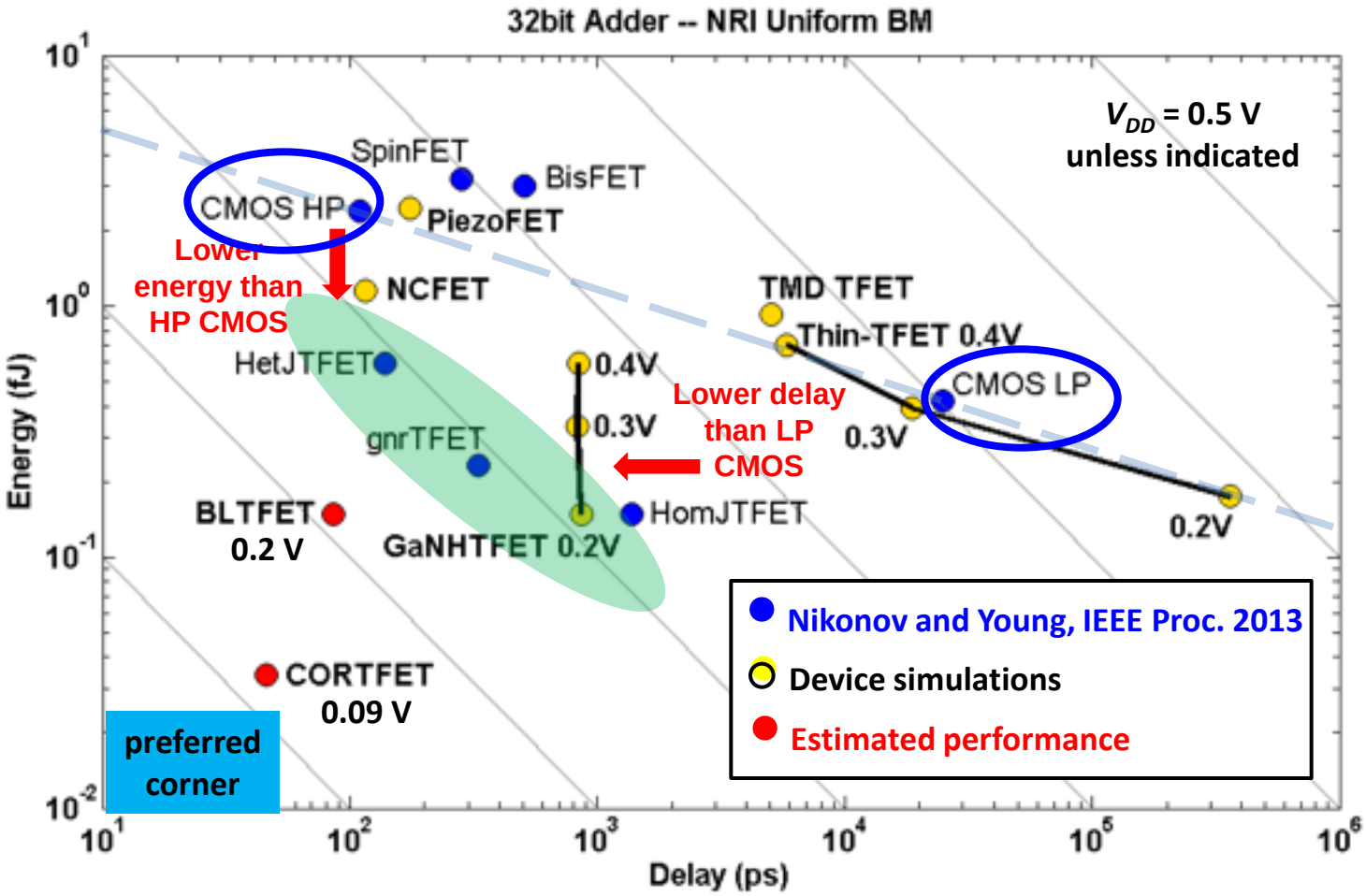


High Performance Computing

3D Stacking

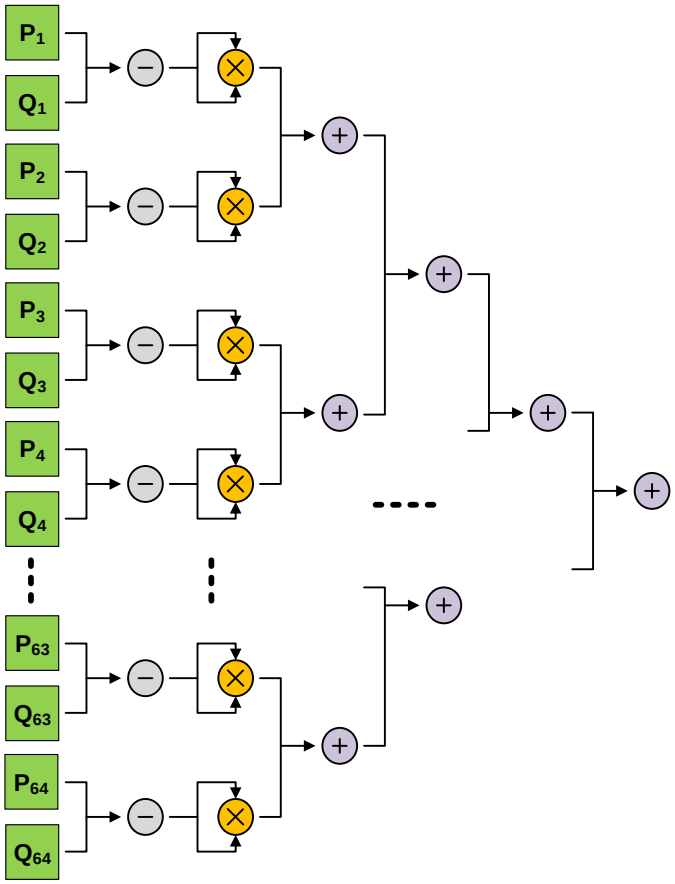


Digital Benchmarking: Tunnel FET vs. CMOS



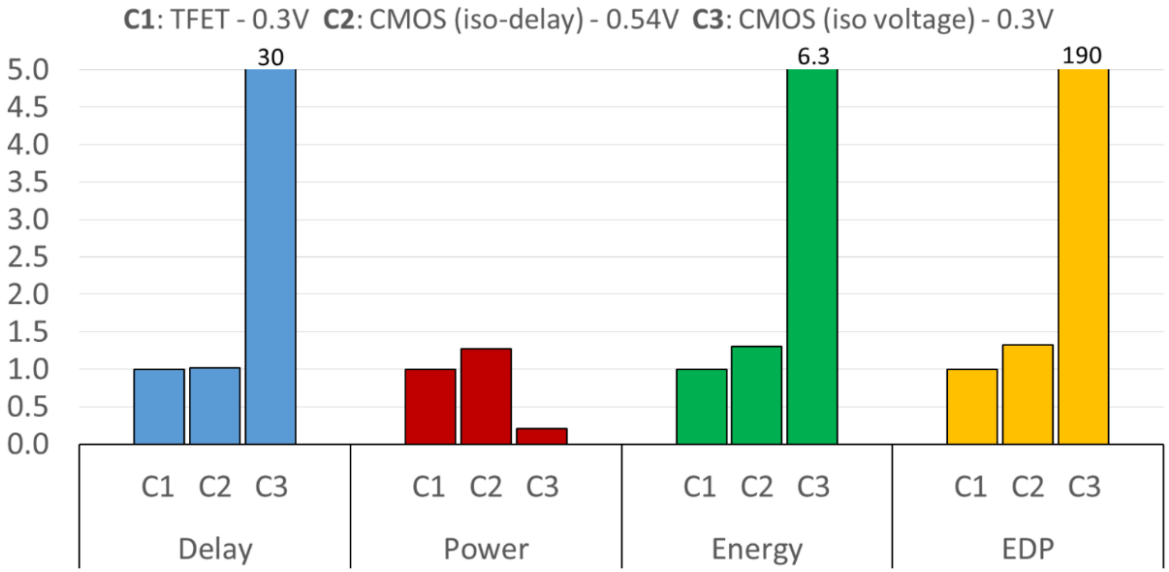
D. Nikonov and I. Young, "Overview of beyond-CMOS devices and a uniform methodology for their benchmarking", Proc. IEEE, 2013

Euclidean Distance Computation



$$\sum_{i=1}^{64} (P_1 - Q_1)^2$$

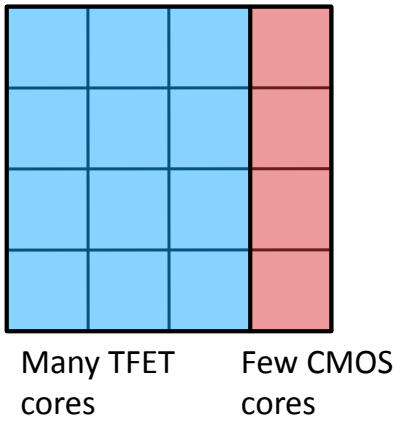
- **HTFET accelerators outperform a range of CMOS designs**
  - **6X energy reduction over iso-voltage CMOS design**
  - **30% less energy than iso-performance CMOS design**

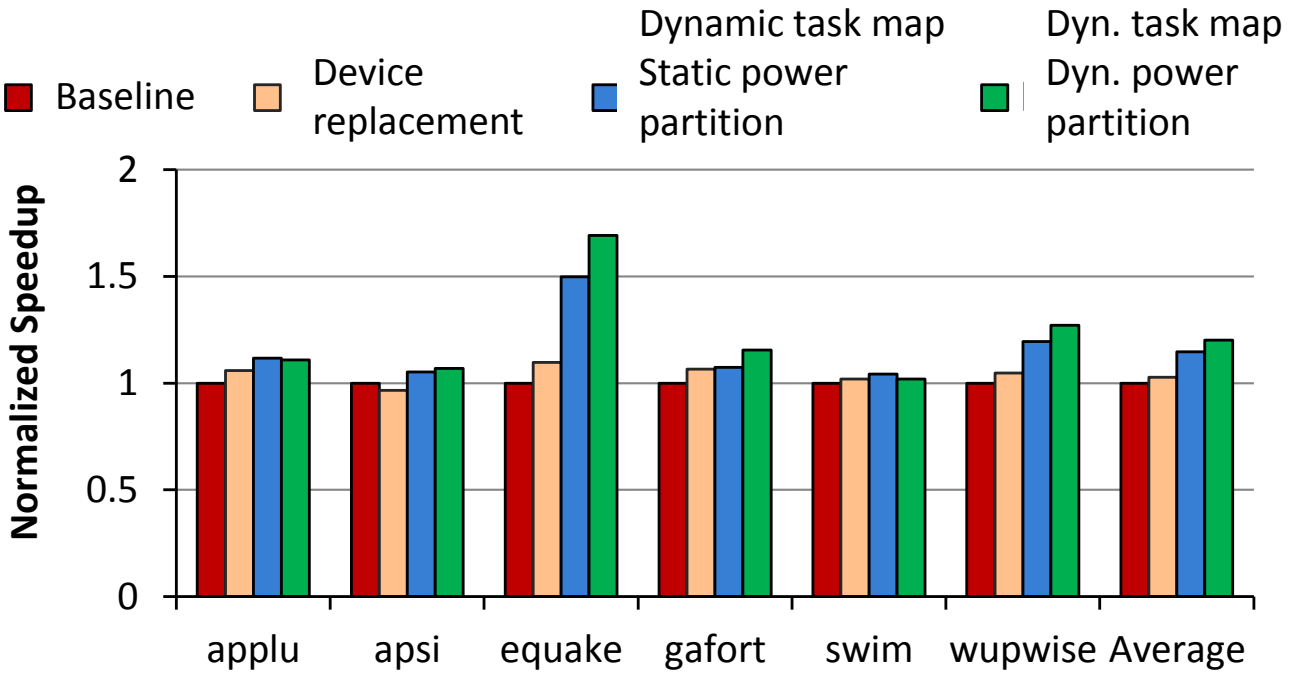


Ref: K. Swaminathan et al, DATE 2014.

CMOS-TFET Heterogeneous Multicores

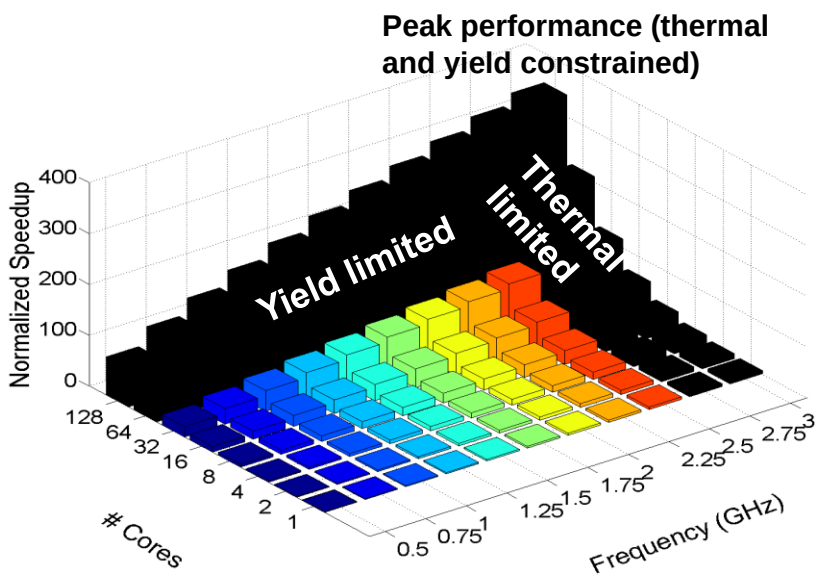
- CMOS has higher peak performance @ high VDD
- TFET Processor is “cooler”
- Maximize performance using CMOS-TFET heterogeneous multicores

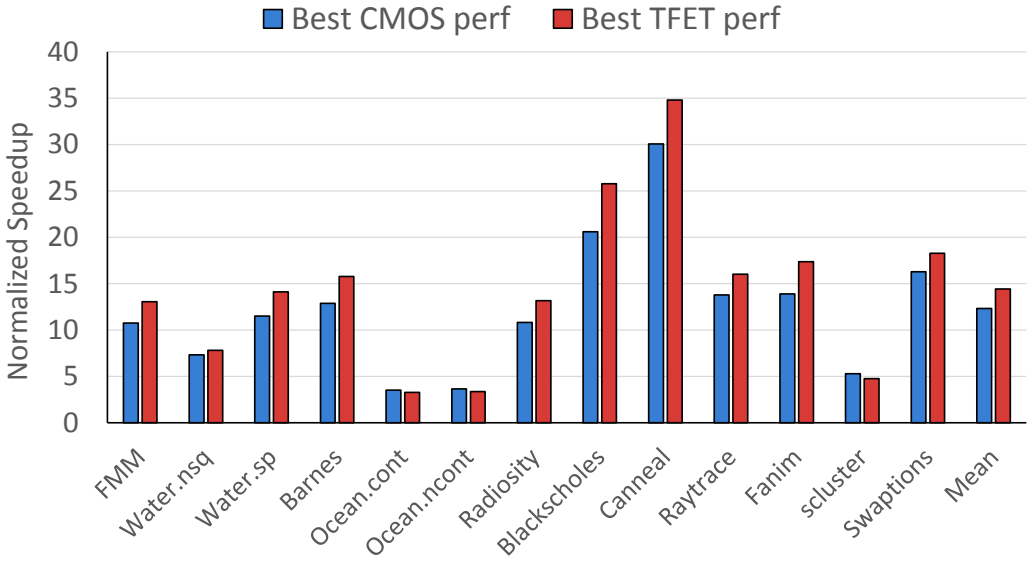




K. Swaminathan et al, ISCA 2014.

TFET in 3D Stacked Multicore Systems

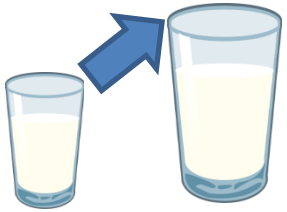




- **Relative performance of a 64-core CMOS and HTFET 3D stacked system, normalized to a single core CMOS performance.**
- **18% speedup obtained by using HTFET cores over CMOS cores.**
- **Heterogeneous 3D stacked CMOS-HTFET multicore system can result in even higher speedups**

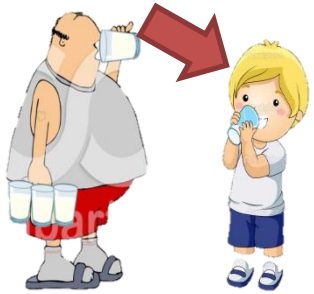
K. Swaminathan et al, ISCA 2014.

Emerging System Design Using HTFET



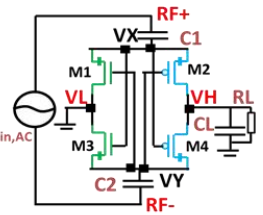
Increase the harvested power

+

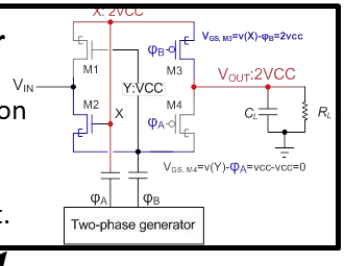


Reduce the power consumption

PSU: TFET AC-DC Rectifier
(H. Liu et al., ISLPED'13, JETCAS14)
- ✓ High sensitivity and power conversion efficiency to weak RF input (> 90% @-42 dBm input).
- ✓ 0.4uW output @-33dBm RF input

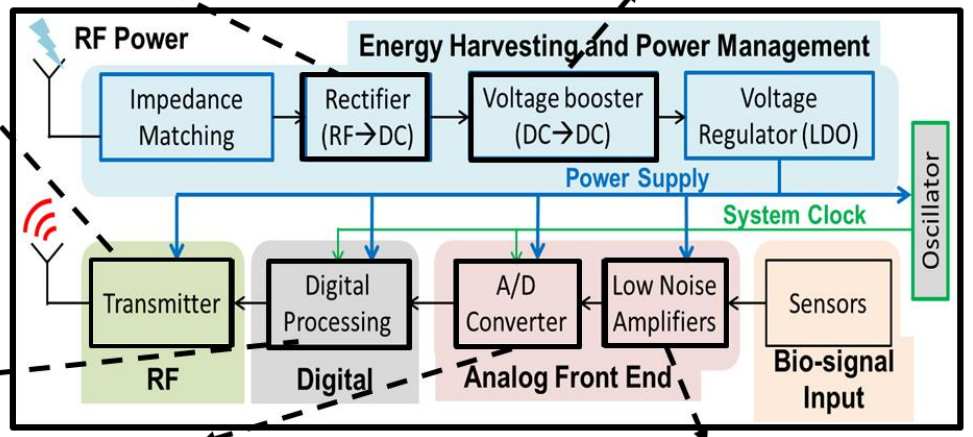


PSU: TFET DC-DC Converter
(U. Heo, et al, VLSI Design 2015)
- ✓ > 90% peak power conversion efficiency at 0.2V without external kick-up.
- ✓ 0.37 V output at 0.2 V input.

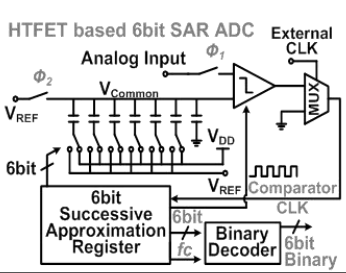


UCSD: TFET RF circuits (VCO/ Mixer/LNA), Parasitic Analysis; PSU: Current-mode transmitter
(W. Y. Tsai, et al, VLSI-SOC'14)

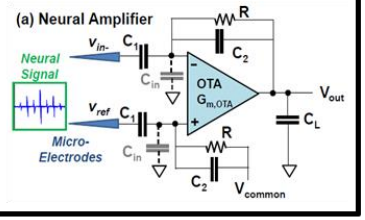
PSU: TFET Standard Cell Library, Processor Architecture
(K. Swaminathan, et al, ISCA'14, DATE'14)
- ✓ Ultra-low power, energy efficient digital processing



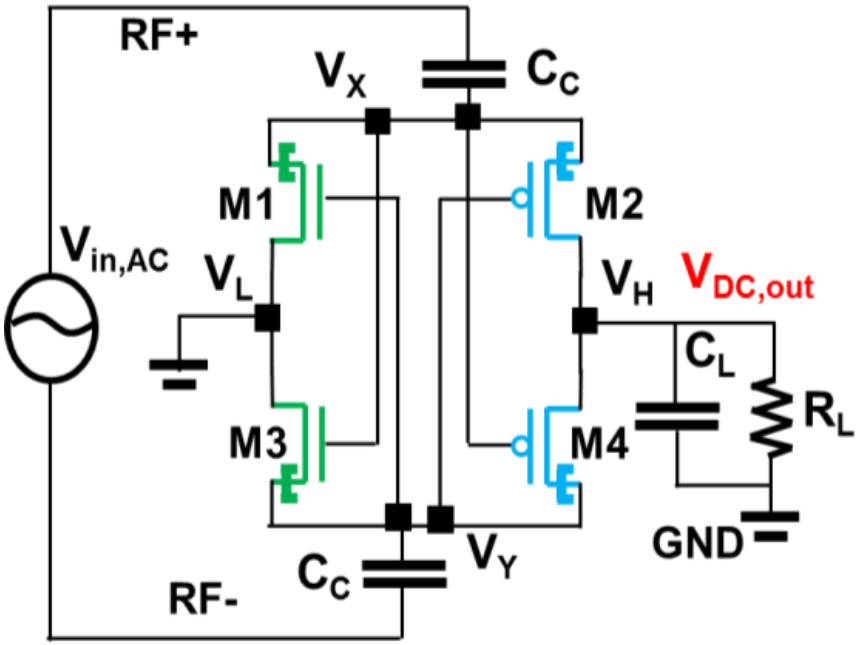
PSU 6-bit 10MS/s SAR ADC
(M. S. Kim, et al, TED to be published)
- ✓ Low-power, low-voltages.
- ✓ At 0.3 V supply voltage, power consumption of 0.25 µW, SNDR of 35dB (ENOB=5.6b), 0.51 fJ/Step.

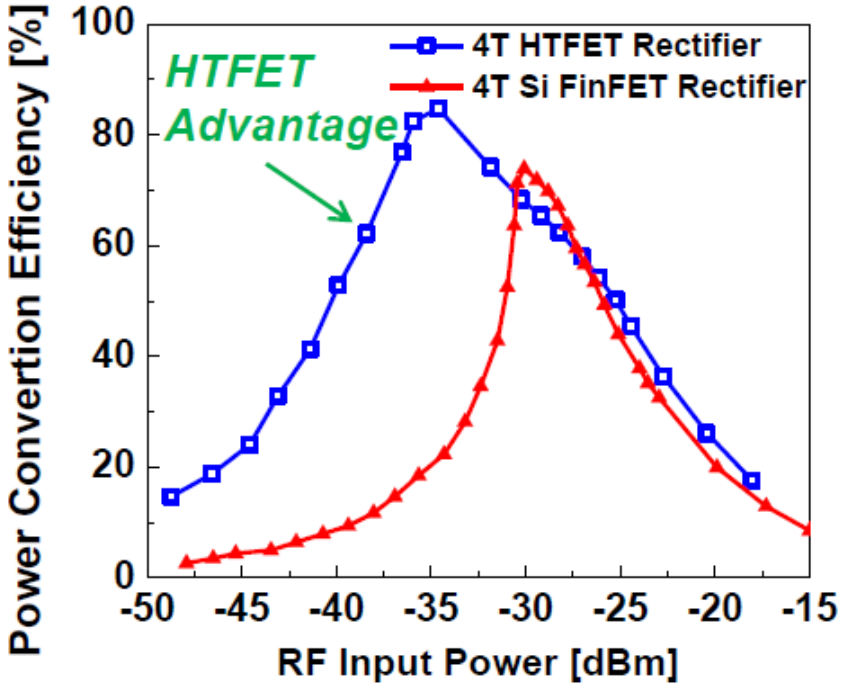


PSU Neural Amplifier (H. Liu, et al, ISLPED'14)
- ✓ 0.5 V, 5nW per channel.
- ✓ 39 dB voltage gain, 2kHzbandwidth
- ✓ noise efficiency factor: 0.64



High-Efficiency HTFET Rectifier

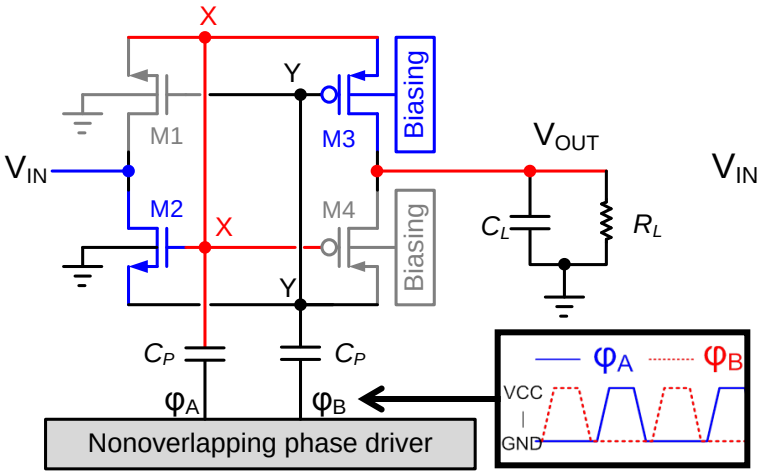




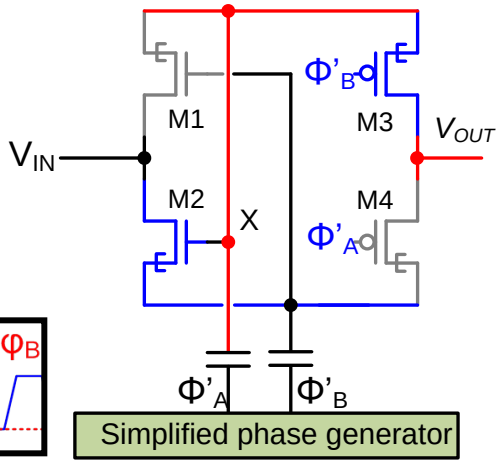
Steep-Slope Features: Lower threshold voltage and resistive loss
Uni-diretional Conduction: Lower leakage current from output to input

H. Liu et al., "Tunnel FET RF rectifier design for energy harvesting applications," JETCAS 2014

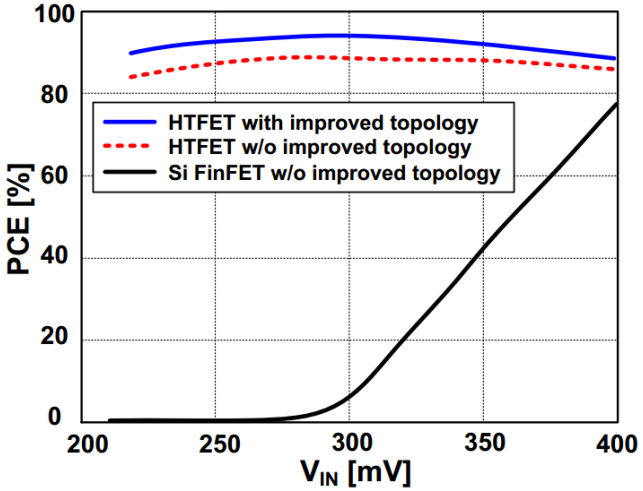
High-Efficiency HTFET Switched-Capacitor DC-DC Converter



(a) Conventional design

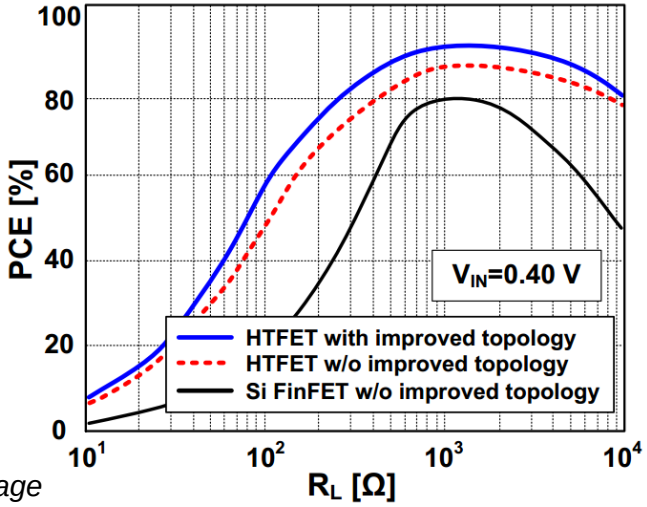


(b) Proposed design



(c) Efficiency

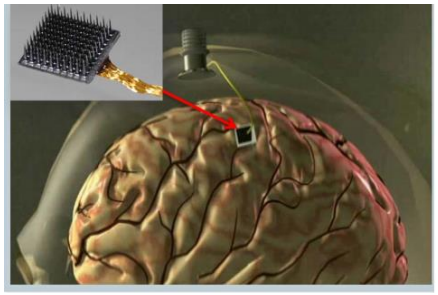
- **Steep-Slope Features**
  - Lower threshold voltage and resistive loss
- **Uni-diretional Current Conduction**
  - Lower leakage current from output to input
  - **Lower power by simplified phase generator**
  - **Novel topology of doubling output gate control for lower resistive loss**



U. Heo et al., "A high-efficiency switched-capacitance HTFET charge pump for low-input-voltage applications," VLSI Design 2015

Low-Noise HTFET Neural Amplifier

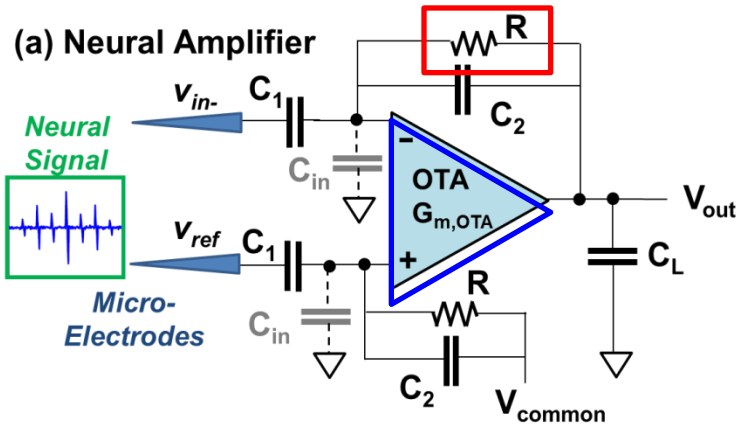
❑ Motivation: Low-Noise Amplifier for Neural Signal Recording

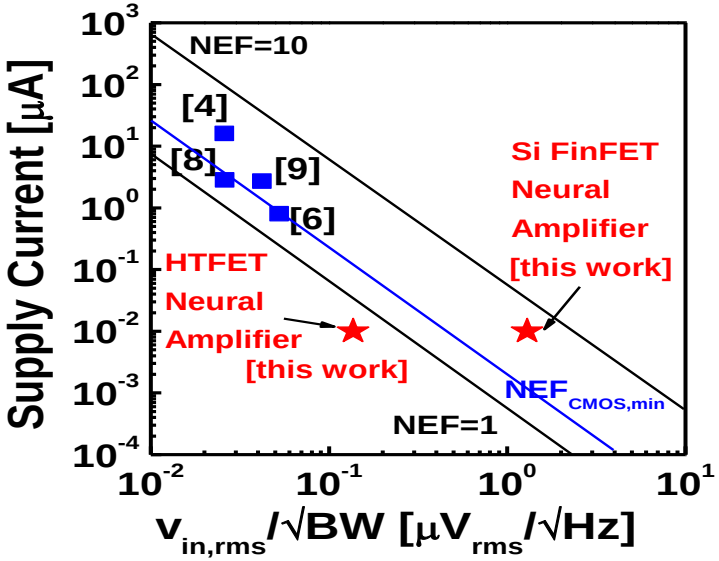


Key Design Points:
- ✓ High gain
- ✓ Low input-referred noise
- ✓ Low power

Nurmikko et al. "Listening to Brain Microcircuits for Interfacing With External World", 2010 IEEE Proceeding.

❑ Steep-Slope Tunnel FET Neural Amplifier



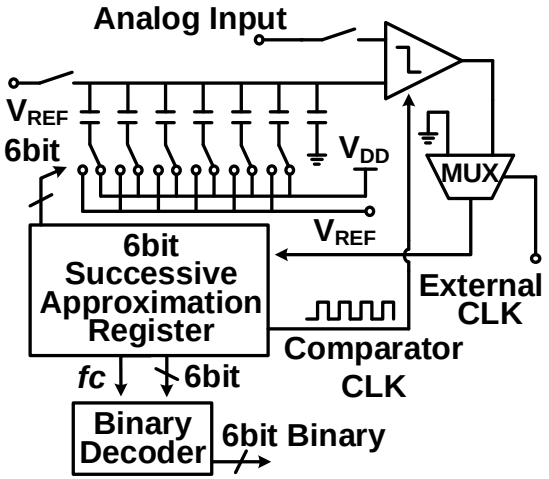


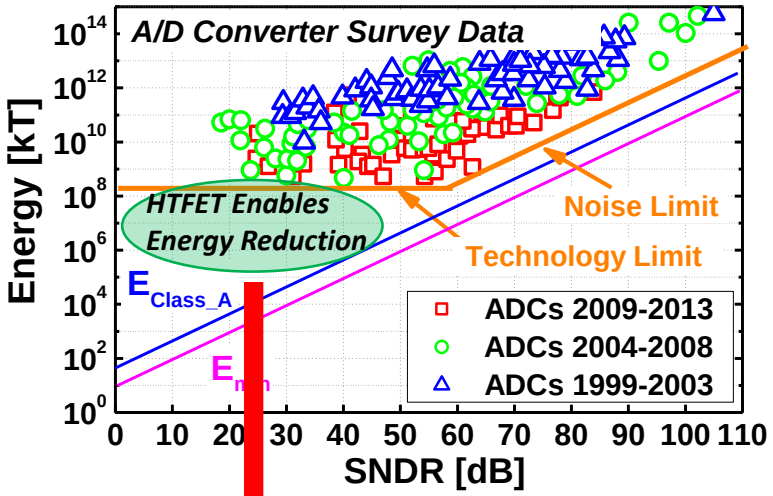
[4] UU@JSSC'03
[6] UW@T.BCAS'12
[8] EPFL@EMBC'12
[9] MIT@T.BCAS'07

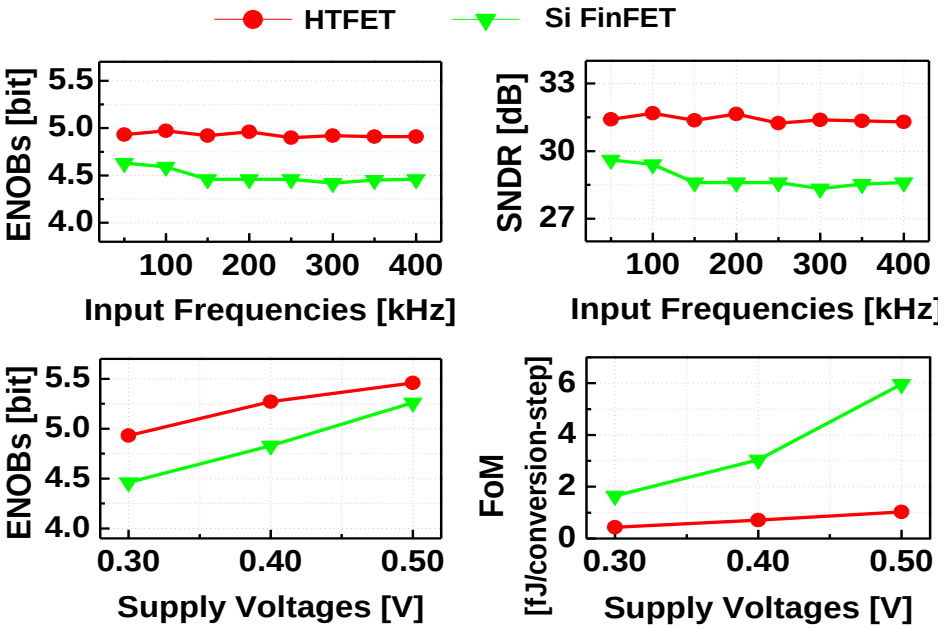
H. Liu., et al, ISLPED'14.

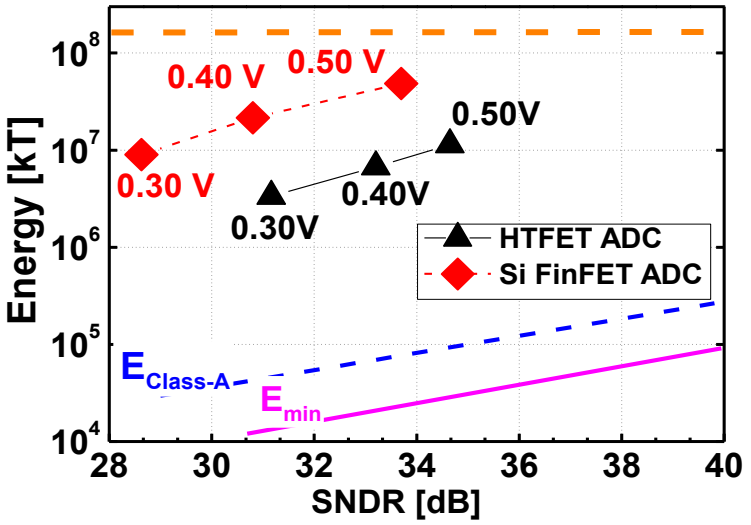
Low-Power HTFET SAR ADC

SAR: most digitized









M. Kim., et al, TED 2014

Summary

- **Promising "Beyond-CMOS" candidate**
  - Technology scaling has forced us to plan for the Post-CMOS era
  - HTFET can complement, or replace CMOS enabling new design spaces
- **Key devices features**
  - Steep-slope switching, Uni-directional current conduction,
  - High small-signal R_O in saturation, high g_m/I_{ds}, high f_T at low current,
  - Negative differential resistance (NDR), Competitive noise performance
- **Parallelism and 3D design further improves performance**
- **Beneficial device features in analog/RF circuits design**
  - Amplifier
  - Current-mode logic
  - RF transceiver
  - Rectifier
  - DC-DC converter
  - A/D converter
  - Energy harvesting
  - Power management
- **Future work**
  - Device fabrication, modeling, circuit & system design and evaluations

Thanks
Q&A

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