Steep Slope Devices: Enabling New Architectural Paradigms

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ABSTRACT

The existence of domains where traditional CMOS processors are inefficient has been well-documented in the current literature. In particular, the inefficiency of general purpose CMOS designs operating at very low supply voltages is well-known, and steep sub-threshold slope technologies, such as Tunneling Field Effect Transistors (TFETs), have been demonstrated as a viable alternative for the low-voltage operation domain. However, restricting the design space of steep slope technology-based processors to near-threshold or sub-threshold general purpose processors does the technology a disservice.

Steep slope (SS) architectures can simultaneously expand the frontiers of viable computers at both ends of the energy scale: On the one hand, SS architectures enable ultra-low power sensor nodes and wearable technology, while on the other, they are applicable to high powered servers and high performance computing engines. We demonstrate the benefits of adapting this technology in such non-conventional domains, while attempting to address the major challenges encountered. We explore the effect of noise and variations at various levels of abstraction, ranging from the device to the architecture, and examine various techniques to overcome them.

1. INTRODUCTION

Limitations in the performance and energy efficiency of traditional CMOS transistors at sub-threshold voltages have led to explorations of a wide gamut of device and architectural techniques. Several techniques, such as vertical FinFETs at the device-level and near- or sub-threshold computing at the architectural level, have so far enabled energy efficiency enhancements. However, the inherent physical limitations of the charge transport mechanism in MOS transistors have forced a rethink of several aspects of processor design, ranging from the device to the system level. We examine adopting a special class of devices, with steep sub-threshold slope, to achieve these designs.

In this paper, we attempt to stretch the boundaries of computing further into domains that are currently unreachable or difficult to achieve, ranging from ultra-low power sensor nodes with RF energy harvesting capabilities to high performance server architectures that are designed with high yield and thermal resilience.

The subsequent sections of the paper are as follows. Section 2 describes the device-to-architecture abstraction model that we employ. Section 3 illustrates some of the challenges faced during the adoption of these new computing paradigms, while Section 4 proposes means to overcome these challenges and demonstrates the benefits of using these steep-slope transistor-based designs. Finally, we conclude with Section 5.

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2. FROM DEVICE TO PROCESSOR: BOTTOM-UP MODELING OF STEEP SLOPE ARCHITECTURES

In order to implement circuit and architecture designs using emerging device-based technologies, we employ a device-circuit-architecture modeling framework to bridge the different design layers, as shown in Fig. 1. A lookup-table based TFET Verilog-A model has been widely used to accurately model the device performance in TFET prototype circuit demonstration and performance benchmarking. Here the device characteristics across a wide range of operation voltages can be directly obtained from full-band atomistic simulations [1] or from calibrated TCAD Sentaurus simulations [12, 19]. The lookup-table based Verilog-A modeling also provides an efficient model development platform for alternative device designs based on different materials system, device architecture, scalability and operation range, but it also imposes limitations on circuit scale and complexity due to the increased CPU time in circuit simulation. Driven by the demands of practical circuit design and system analysis, compact SPICE models development for different TFETs have recently attracted lots of interest [28], aiming to achieve an accurate prediction of TFET operation.

Based on the device models, various circuit designs using steep slope TFETs have been explored for ultra-low power digital and analog/RF applications [14, 16, 19, 26] by taking advantage of the steep sub-threshold slope-induced energy efficiency benefits that these devices provide. Studies of TFET electrical noise modeling [17] and variation impacts [1, 19] provide more insights for design tradeoffs between energy efficiency and reliability.

An architecture-level abstraction from the aforementioned circuit design can be obtained in different ways, depending on the nature of the processor configuration. The critical

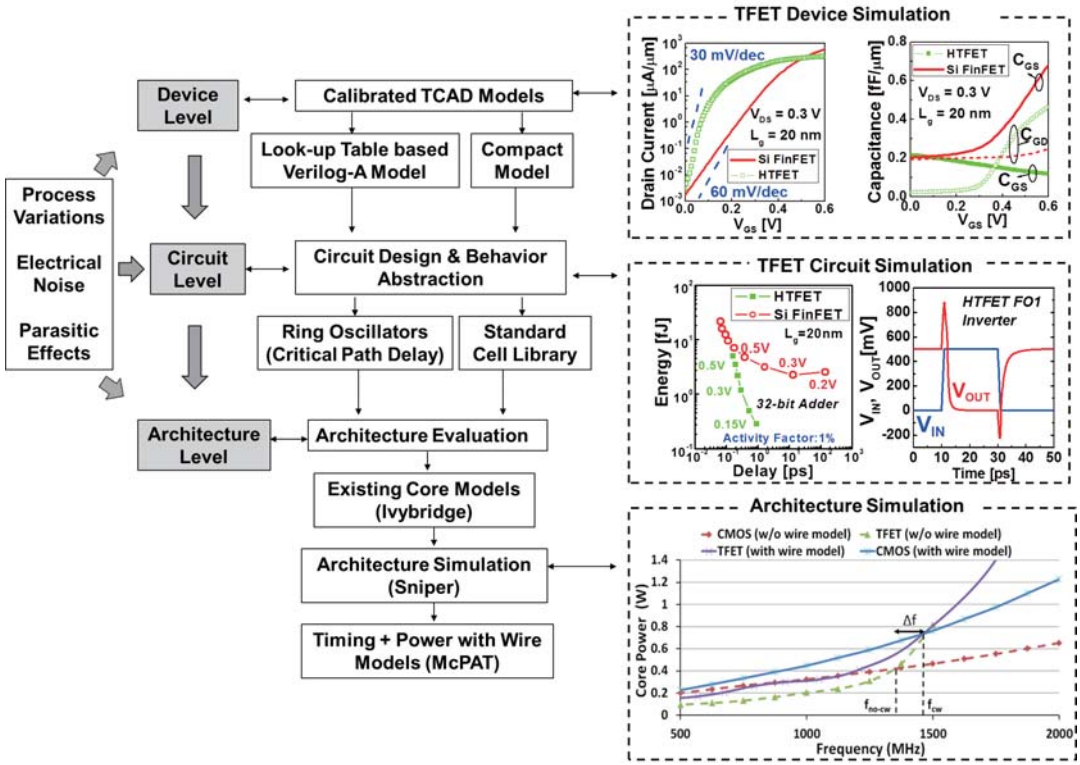

Figure 1: Device-to-architecture abstraction model for Steep Slope Processors

path delay of a CMOS-based in-order core is obtained by calibrating the delay of a series of cascaded FO4 inverters to form a ring oscillator with the frequency of an existing Intel Atom processor configuration. The total core power is obtained by multiplying the individual transistor power by the total number of transistors in the processor. The TFET processor critical path delay and power at different supply voltages are obtained by scaling the corresponding FinFET core parameters at that particular voltage. Further details regarding this modeling technique are described in [11].

On the other hand, due to the diversity in critical paths in out-of-order cores, a simple ring-oscillator model may not be sufficiently accurate. Hence, we carry out power and timing evaluations of existing processor designs such as Intel Ivy-Bridge using an architectural simulator, namely Sniper [2] which is integrated with McPAT [13], a power and timing estimation tool. We instrument McPAT to output the critical path delay and power for a 22nm FinFET processor design and obtain the corresponding TFET core numbers by scaling the device parameters as in the previous case. In addition, wire delay and power form an important constituent of the overall processor delay and power. We instrument McPAT to obtain the power and delay of the most significant microarchitectural components and add a model for wire power and delay for both FinFET and TFET technologies. When added to the existing processor model, we observe a slight increase in the crossover frequency (f_{cw}) in comparison to the crossover frequency in the absence of wire effects (f_{cno-w}). This is on account of the fact that the wire delay remains roughly constant, irrespective of the transistor technology. This complete methodology is illustrated in Figure 1.

3. CHALLENGES TO OVERCOME

While modeling the device-to-architecture abstraction for steep slope processors, the contribution of noise and variations can play a significant role at various levels. Electrical noise has a significant impact on systems which have limited signal amplitude due to a low-voltage power supply. On the other hand, device-level variations, when coupled with variations in the manufacturing process, can manifest themselves at the circuit and architectural levels for a whole range of applications. Our studies show that CMOS and TFET-based processors are affected to different degrees by these variations over different supply voltage ranges. In this section, we examine the impact of noise and device-level variations on CMOS and TFET devices in the different application domains discussed in the paper.

With the scaling of technology nodes, electrical noise imposes a growing reliability issue due to the increased sensitivity of circuit performance and reduced signal range at low V_{DD} [8]. For embedded wireless transceiver systems, the analog and RF front-end blocks are crucial in that they usually consume a considerable fraction of the overall power budget. The presence of noise in these blocks thus limits the overall system power efficiency and performance specifications including the signal bandwidth, signal-to-noise ratio (SNR), dynamic-range (DR), etc. When the embedded system is powered by weak or intermittent energy sources like ambient RF signals, thermo-electricity, or solar cells, the maximum signal amplitude, as well as the harvested power and the supply voltage, are lowered. Some signals are intrinsically weak, e.g. bio-signals. In such scenarios, the performance in the presence of noise suffers, especially when the supply voltage is low.

The analog and RF frontend blocks thus face the challenge of realizing a noise-affected, low-supply, low-power design, and the tradeoff between power and noise is a key consideration. Consequently, it is of great importance to evaluate the electrical noise characteristics for steep-slope devices while pursuing power reduction in embedded systems. We shall subsequently examine the impact of noise on the performance of TFET-based systems, with the noise-related design challenges in TFET amplifiers as an example.

Low frequency noise characterization for different types of TFETs has been reported in [6, 18], showing strongly process dependent noise characteristics. The analytical models on flicker, shot and thermal noise were developed in [17] for III-V HTFET. The simulation results reveal that at a nominal operation voltage of 0.3 V, HTFET exhibits competitive input referred noise as compared to Si-FinFET in KHz and MHz frequency range. Due to the presence of increased shot noise due to the tunnel junction, however, the input referred noise of HTFET increases moderately at operating voltage exceeding 0.3 V and frequency range of 10 GHz or higher. The resultant noise figure of III-V HTFET fulfills the bandwidth requirement of ultra-low voltage sensor node applications.

3.1 Effect of noise in amplifier design

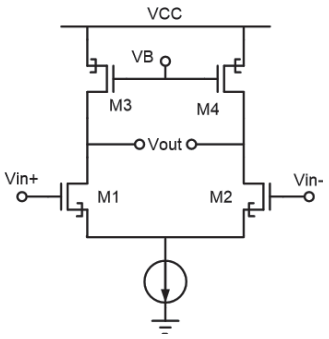

Figure 2: A typical fully differential amplifier

Figure 2 shows a typical fully differential amplifier. It is well known that the input referred noise of the CMOS amplifier is given by the equation:

$$\overline{d\nu_{n,in}^2} = 2\Big(\frac{4kT\gamma}{g_{m1}} + \frac{K_{fn}/2K_n}{(WL)_1 C_{ox} f} + \frac{g_{m3}^2}{g_{m1}^2}\Big(\frac{4kT\gamma}{g_{m3}} + \frac{K_{fp}/2K_p}{(WL)_1 C_{ox} f}\Big)\Big) df \quad (1)$$

where g_m is the transconductance, WL is the transistor area, f is frequency, and K_{fn}, K_n, and C_{ox} are device-related constant parameters. Further, the dynamic range of the amplifier can be derived as:

$$DR = \frac{\frac{1}{2}v_{sig}^2}{\nu_{n,in}^2} = \frac{V_{out}^2}{2A\overline{\nu_{n,in}^2}} \quad (2)$$

where A is the amplifier gain. In order to reduce the input noise and increase the dynamic range, larger input g_m is required. However, for a power-sensitive design, a large current might not be efficient to boost the transconductance. Therefore, a trade-off occurs between low power and low noise. In this case, the steep-slope TFET offers a higher current efficiency in terms of g_m/I_{ds} while providing the same transconductance [17].

3.2 Variation in steep-slope multicores

In addition to the noise challenge discussed above, steep-slope devices are also prone to process variations due to their operation at reduced supply voltage and the steep transition of their current characteristics. For III-V HTFET, variation sources that can alter the tunneling barrier width can cause a significant I_{on} fluctuation given the exponential current dependence on the tunneling barrier width [1, 19]. Variation sources such as fluctuations in source doping, oxide thickness, gate-contact work function, left/right gate edge overlap, body thickness have been investigated from the device to circuit level [19], among which the work function variation dominates, considering the reported process data [1]. Fig. 3 shows the transistor delay fluctuation corresponding to the threshold voltage shift caused by the gate work function variation, based on the Verilog-A models of L_g=20 nm HTFET and Si FinFET. HTFET exhibits an overall lower delay variation compared to Si FinFET for $V_{dd} < 0.5V$ while Si FinFET operates in the near- or sub- threshold region.

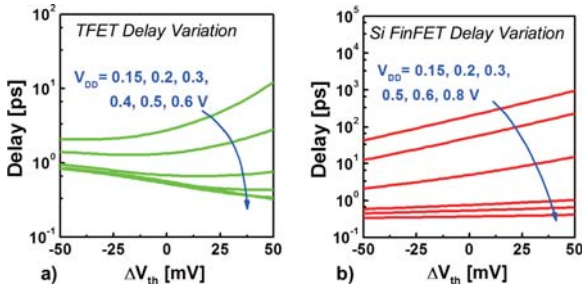

Figure 3: Impact of effective V_{th} shift on transistor switching delay for a) TFETs and b) Si FinFETs. The effective V_{th} shift in TFET is a reflection of the gate-contact work function variation.

3.3 Observing device variations at the architecture level

Based on the different sources of variations at the device level, we classify the variations as global (constant) and random variations. As observed, the variation in work function, an inherent atomistic property of transistors, dominates the overall variation for TFETs [1]. In a similar manner, the corresponding variation in FinFETs can be modeled as a zero mean Gaussian with a work function variation of around 50 mV, as demonstrated in [22]. The remaining sources of variation, allied with variation components localized to a section of the wafer, can be assumed to encompass 3-5% of the total variation [10].

In order to model the critical path of a processor, we assume a number of such variation-affected transistors cascaded together. In order to determine the exact length of this critical path, we carry out a critical path analysis using *Fabscalar* [4]. This tool generates synthesizable HDL code for different micro-architectural configurations, by varying parameters such as the issue width, pipeline depth and number of execution units. Further details regarding the standard cell libraries used for synthesizing TFET processor model are given in [23].

Figures 4 and 5 show the dependence on the worst case (3σ) variation in delay on supply voltage and frequency respectively, for both FinFET and TFET-based processors.

The processor model used was a 4-issue Ivybridge configuration with logic and wire models obtaine using techniques similar to those in [24]. These figures lead us to draw the following conclusions. Firstly, TFET processors are less susceptible to variations at low V_{dd} than their FinFET counterparts. Also, the variation behavior in the region of optimal operation of both core types are roughly similar (within ± 10% of each other).

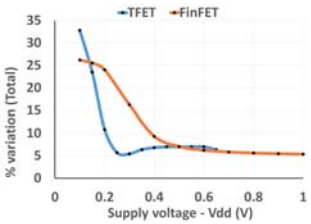

Figure 4: Dependence of variation on supply voltage

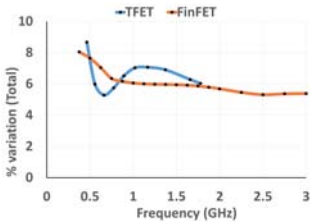

Figure 5: Dependence of variation on frequency

3.4 Variation mitigation using voltage scaling

In order for a system to meet its specified performance criterion in the presence of variation, it is possible to boost the supply voltage to compensate for the additional worst-case variation-induced delay. Doing so, however, comes at the cost of additional dynamic and leakage power. As shown in Figure 4, both the distribution of variation and its worst case ($\mu \pm 3\sigma$), depend on the target supply voltage. Further, in case of TFET processors, this can also shift the effective crossover point, i.e f_c, below which TFET cores are more power efficient than CMOS cores. Since the variation of TFETs becomes higher than CMOS for supply voltages above V_t, the crossover point, which falls in this super-threshold region is shifted to the left due to the additional voltage boost required by TFETs to compensate for the increase in worst-case delay. Figure 6 shows the effect of these overall variations on the TFET-CMOS crossover plot.

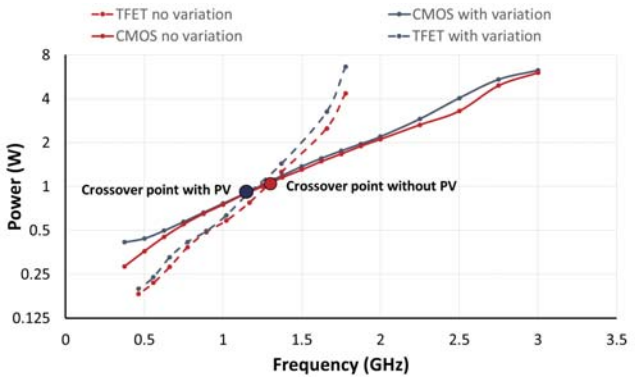

Figure 6: Power-frequency curves for CMOS and TFET processors with and without the effects of variation.

4. REALIZING NEW DESIGN SPACES

In this section we examine in detail the impact of employing steep slope technology in different domains ranging from the ultra-low power domain with energy harvesting to the server/high peformance domain with 3D stacked multicore architectures.

4.1 RF Energy Harvesting using Steep Slope Devices

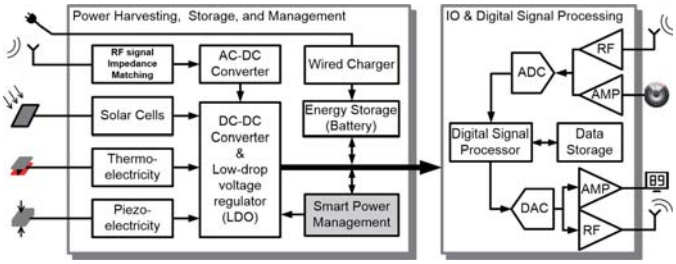

Figure 7: Embedded systems powered by energy harvesting sources

Improvements in the energy density of batteries have lagged behind the power scaling of integrated circuits and systems. However, batteries are are still prevalent power sources nowadays, and the necessity of replacing and charging of these batteries limits the design space of wireless circuits and systems. At the same time, energy sources like solar cells, thermo-electrics, piezo-electrics, and RF signals have been studied further to power low-power systems. In recent years, emerging battery-less designs, such as RFID, RF-powered insect monitoring and sensing, and vibration-powered transceivers have extended the traditional design space.

Table 1 summarizes the characteristics of typical non-battery power sources along with the traditional lithium ion battery. It can be concluded from Table 1 that, under certain conditions, the non-battery sources are able to generate power up to several mW. It is also important to notice that the applications using such non-battery power sources are limited in that they have strong dependence on the environment, e.g. the light intensity, vibration strength, temperature gradient, and RF power density. Hence, due to limited and unstable power that could be harvested from the ambient environment, existing battery-less systems have a limited operation range or computational capability. For example, with a wireless several-watt RF signal transmitter, existing RFID tags typically have an operation range of meters and support only primitive sensing, identification, or transmission [25].Therefore, aside from the exploration of more power-efficient energy harvesters, the synergy of hybrid power sources and the more power-efficient signal processing modules based on TFETs is of great significance.

Fig 7 shows an embedded system powered by hybrid energy sources. Using a smart power management module to obtain co-operation of two or more power sources, the system operation is less likely to be interrupted. Furthermore, it has been already shown that steep-slope TFET has higher power efficiency in both digital and analog signal processing domains. Finally, energy harvesters like the AC-DC rectifiers based on TFET also have high power-conversion-efficiencies [14]. The design space of TFET-based system is thus significantly extended through the high power-conversion-efficiency energy harvester, high efficiency signal processing, and the synergy of hybrid power sources.

4.2 Extending the boundaries of high performance computing with steep-slope devices

Energy Source	Output power and voltage	Cost, Volume Area etc.
Solar cells	Efficiency 8-28% ∼700mv for 0.1W/cm^2 power density by crystal-Si solar cell	\$0.6/Watt Silicon thickness: 30-100 μm
Lithium Ion Battery	1.8 W/g, 4V	0.3-0.8/Wh size down to a coin
Thermo-Electrics	$20\mu W/cm^2$ extracted from body	1300 thermocouples per cm^2
RF	Typical values: a) 25(100)μW ∼20(10)km from 1MW TV station b) 5 μW ∼100 m from 40W cellular station c) 45(4500)μW ∼10(1.0)m from 4W RFID reader with R_x antenna.	
Piezo-electrics	2.1 mW/cm^2 at 4 km/hr	

Table 1: Typical energy sources for embedded systems

Emerging devices expand the regions of system design space considered both plausible for mass deployment, in terms of manufacturability as well as operating conditions, and preferable in terms of performance, power and cost. The technique of 3D integration is rapidly maturing [7] and we seek to optimize the benefits offered by processor designs comprising steep-slope devices, like HTFETs [15, 20, 21].

Although steep slope device-based processors, are noted for their low voltage and power efficient operation, they have an important role to play in the high performance computing domain as well. Both 3D integration and TFET designs offer the potential to extend the maximum number of aggressive cores possible within a viable yield and thermal budget. By adopting 3D designs, it is possible to ameliorate problems with yield and thermal limitations that affect current manycore designs.

It is known that yield decreases super-linearly with increase in area [3], and communication costs among cores scale poorly in planar designs [27]. As a result, transitioning to 3D integration offers a very direct means to achieve meaningfully higher core counts in tightly integrated systems. However, this aggravates thermal limitations due to the huge increase in power density, since there are additional heat sources and insulators between the cooling system and lower layers in the chip stack. Hence it becomes necessary to operate the cores at extremely low frequencies to ensure that the power dissipated and, consequently, the power and thermal density, remain within acceptable limits. Due to the ability of steep-slope devices to offer fundamental reductions in leakage currents and switching energy at lower operating frequencies, adopting steep-slope processor designs in place of CMOS will allow more layers within the same thermal budget. This allows 3D TFET based designs to scale to sufficient parallelism to overcome limitations in the serial performance of TFET based processors.

In such a scenario, there are several considerations, such as determining the optimal multiprocessor microarchitecture and operating conditions, and obtaining the 'sweet spot' between the yield and thermal constraints in terms of manufacturing cost, performance and power efficiency.

4.3 Yield and thermal aware processor design

On account of the super-linear decrease in yield with increase in die area, it is not viable to increase the number of cores on a single layer of a chip beyond a certain point. 3D stacking [9] of multiple layers on chip has been demonstrated to be beneficial in increasing overall performance due to increased bandwidth and shorter wire lengths. In addition, it is also possible to obtain a much higher yield in comparison to an iso-area 2D design by reducing the area footprint per layer. However, there are losses occurring as a result of joining 2 layers together, quantified by the bonding yield. As a result there is a trade-off between increasing the die size and increasing the number of layers [3].

The extra die area that 3D stacking provides makes it possible to improve the overall chip yield by introducing redundant cores. This is known as core sparing and is commonly used as a technique to improve the overall yield of several processors in industry [5]. The improvement in yield significantly shortens the time to market for these processors, which makes up for the additional hardware resources required for the core redundancy. This is a far more viable alternative than aiming to improve the fabrication process both from a time and cost perspective. Both the area footprint and the number of layers cause the proportion of redundant cores to increase. For smaller chip areas the losses due to bonding multiple layers together dominates. However, as the area per layer increases, the yield decreases at a faster rate and folding the cores to stack them in multiple layers can arrest this decline.

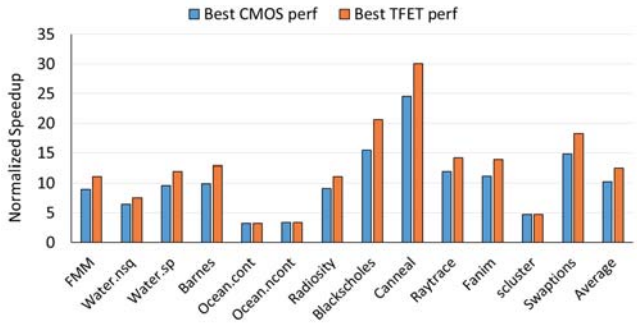

Figure 8: CMOS and TFET multicore speedup (normalized to single core CMOS configuration) for a server system comprising of a maximum of 64 cores.

Figure 8 shows the overall speedup for CMOS and TFET multicore systems comprising stacked cores, under yield and thermal limitations. For the purpose of this study we consider a thermal limit of around 85-90°C (358-363K), which is an acceptable thermal range for server-based systems. Although all cores have similar microarchitecture configurations (4-issue Ivybridge-like architecture), we observe that the superior thermal efficiency of TFET cores enables a larger number of cores to function within the thermal limit, resulting in a 22% speedup over an equivalent CMOS configuration. Also the idea of core-sparing enables us to employ a configuration which requires only 64 functioning cores from a maximum of 128 cores.

5. CONCLUSION

We have demonstrated how steep-slope devices can overcome their inherent device and domain challenges, such as noise and variation sensitivities, to extend the range of computing beyond that of traditional CMOS based processors. In the ultra-low power digital domain, we can decrease power demand by expanding the range of lifetimes, or complexity

of processors used in harvested energy devices. At the same time, we improve the potential compute density of HPC applications by 22% by exploiting the increased slack in the thermal envelope that steep-slope devices can provide. In addition to the digital applications, we have demonstrated the benefits of utilizing the unique characteristics of the steep-slope devices to achieve high sensitivity and high energy conversion efficiency in energy harvesting systems.

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