Pairwise Coupled Hybrid Vanadium Dioxide-MOSFET (HVFET) Oscillators for Non-Boolean Associative Computing

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Abstract

Information processing applications related to associative computing like image / pattern recognition consume excessive computational resources in the Boolean processing framework. This motivates the exploration of a non-Boolean computing approach for such applications. In this work, we demonstrate, (i) novel hybrid set of pair-wise coupled oscillators comprising of vanadium dioxide (VO_2) metal-insulator-transition (MIT) system integrated with MOSFET; (ii) degree of synchronization between oscillators based on input analog voltage difference; (iii) implementation of hardware platform for fast and efficient evaluation of L_k fractional distance norm ($k<1$); (iv) improved quality of image processing and ~20X lower power consumption of the coupled oscillators over a CMOS accelerator.

Introduction

Complementary metal-oxide-semiconductor (CMOS) based Boolean logic is the cornerstone of the information technology industry. A class of problems, related to associative processing, requires massive computational resources in the Boolean framework [1]. While this has motivated the development of faster and more efficient algorithms, they are mapped back to the Boolean hardware which ultimately limits their performance. Fundamentally, this "Boolean bottleneck" arises from the requirement of a large number of power-intensive multiply–accumulate (MAC) operations, common to many associative-processing algorithms. This encourages the development of a non-Boolean approach utilizing coupled oscillatory systems (Fig. 1) [2-8]. Here, we experimentally demonstrate for the first time, various degrees of synchronization among hybrid VO_2-MOSEFT (HVFET) oscillators in response to an input analog signal difference. The synchronization dynamics enables fast and efficient calculation of a 'fractional distance norm' in the analog domain which is suitable for pattern matching in high dimensional space [9].

Single VO_2 Relaxation Oscillator

VO_2 is a correlated electron system that exhibits a metal-insulator transition (MIT) with up to 4 orders of abrupt resistivity change in 15nm thick epitaxial films (Fig.2b) (bulk films show up to 5 orders). The MIT can be triggered using various external stimuli including electrical triggering [10] (Fig. 2c). This abrupt resistivity change can be engineered into a current controlled negative differential resistance (NDR) regime using an optimum negative feedback to generate sustained charge oscillations [11]. Fig. 3a shows the single VO_2 oscillator circuit consisting of a two-terminal VO_2 device (Fig. 2a) with a MOSFET in series (HVFET-Oscillator). The details of the VO_2 film growth on the (001) TiO_2 substrate and the fabrication process are reported elsewhere [12]. All measurements are carried out at 273K. When the insulator-to-metal transition ($E>E_2$) is electrically induced, there is an abrupt change in the conductivity of VO_2 (Fig. 2c). The MOSFET (acting like a current source) provides a negative feedback to the VO_2 inducing an NDR such that the electric field across VO_2 drops below E_1 (Fig. 3b). This makes the metallic phase unstable causing VO_2 to return to insulating state resulting in a high field drop across VO_2 again. The process repeats inducing a stable oscillatory state [11] (Fig. 3c). The operating load line of the oscillator superimposed on the switching characteristics of the VO_2 device is illustrated in Fig. 3b. The oscillation amplitude superimposed on the output characteristics of the MOSFET (Fig. 3d) shows its operating region. Further, an input gate voltage modulates the MOSFET's operating point and enables the HVFET oscillator frequency to be programmed over a decade (Fig. 3e).

Pairwise Coupled Oscillators

To make such oscillators relevant to computing applications, we explore their synchronization dynamics. Fig. 4a shows the false-colored SEM of the fabricated VO_2 devices and illustrates the capacitively coupled oscillator configuration. The high-pass

filtering configuration formed by the coupling capacitor C_C blocks DC interaction while allowing reactive power to couple. The synchronized time domain waveforms are shown in Fig. 4b along with the corresponding power spectrum (Fig. 4c). It is clear from Fig. 4d that the resonant frequency of the coupled oscillators can be tuned with an input gate voltage difference, ΔV_{GS} (= $V_{GS,2}$ - $V_{GS,1}$).

Computing with Coupled HVFET Oscillators

The nonlinear dynamics of the coupled oscillators are analyzed using the equivalent circuit in Fig. 5. Fig. 6 shows that the relative phase of the two oscillators can be tuned with the gate voltage inputs. The oscillators lock out of phase (~180^o) when ΔV_{GS} =0 V and the phase difference deviates from this value as ΔV_{GS} increases. The corresponding synchronized oscillator trajectories in phase space can be used to capture the difference between the inputs $V_{GS,1}$ and $V_{GS,2}$. An averaged exclusive-or (XOR) measure is used to analyze the oscillator output. The averaged XOR measure is defined as (i) thresholding the analog output to a binary stream, (ii) applying XOR operation on these binary values at every time instance (iii) averaging this XOR output for a finite time duration. The averaged XOR output is equivalent to the fraction of time the dynamical system spends in the grey region (Fig. 7a) where XOR = 1. The XOR output for various input V_{GS} values is shown in Fig. 7b. This output of the synchronized oscillators calculates a fractional distance norm, (L_k norm; k = 0.5), as seen by its close resemblance to the $(x_i^{0.5} - y_i^{0.5})^2$ distance map (Fig. 7c). The experimental and the simulated XOR outputs as a function of input ΔV_{GS} are shown in Fig. 7d, e, respectively.

Associative Processing Application

We investigate the application of these oscillators for visual saliency approximations (detecting parts of the image that visually standout) [13] (Fig. 8a). Oscillator-based edge detection is performed using an array of pairwise oscillators to approximate the degree of dissimilarity between a given image pixel and its immediate neighbors. Different edges, vertical, horizontal, diagonal, are detected based on the selection of neighboring pixels for comparison. As this concept is expanded to include the comparison of pixels within a larger neighborhood (pixels surrounding reference pixel; a 3x3 neighborhood is used here), the output approximates the visual saliency (Fig. 8b). It is evident that the oscillators show higher sensitivity to image contrast in comparison to a CMOS ASIC accelerator (Fig. 8a) that uses a linear $\sum|x_i - y_i|$ norm (Fig. 8b).

Power Consumption

The projected scaling of the input DC voltage and frequency with the VO_2 channel length is shown in Fig. 9a,b respectively. Fig. 10a,b shows the pareto chart of the power consumption for each component of the HVFET oscillator processor and the CMOS ASIC accelerator for visual saliency, respectively. All digital circuits were implemented with 11nm node transistor models projected from the 22nm node PTM model [14]. The coupled oscillators provide a power reduction of ~20X over CMOS reflecting the advantage of 'let physics do the computing' approach [1] and removing the "Boolean bottleneck".

Conclusions

In this work, we provide (i) first experimental demonstration of coupled HVFET oscillators with input programmable synchronization; (ii) hardware platform capable of efficiently computing a fractional distance norm and its application in visual saliency; (iii) ~20X reduction in power dissipation over CMOS.

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References

[1] Shibata *et al.* CNNA, 2012.

[2] Levitan *et al.* CNNA, 2012.

[3] Narayanan *et al.* DATE, 2014.

[4] Hoppenstedt *et al.* PRL, 82,14, 1999.

[4] Datta *et al.* DAC 2014.

[5] Csaba *et al.* CNNA, 2012.

[6] Nikonov *et al.* arXiv: 1304.6125.

[6] Vassilieva *et al.*, IEEE Trans. Neural Netw. 22,84–95 (2011).

[7] Wang *et al.* IEEE Trans. Neural Netw. 6, 283–6 (1995).

[8] Izhikevich, IEEE Trans. Neural Netw.10, 508–26 (1999).

[9] C. Aggarwal *et al.* ICDT 200, 2001.

[10] Freeman *et al.*, APL, 103, 26, 2013.

[11] Shukla *et al.* Sci. Rep, 4, 4964, 2014.

[12] Tashman *et al*. APL, 104,063104 (2014).

[13] N Bruce PhD thesis, York University, Toronto, 2008.

[14] http://ptm.asu.edu/latest.html.

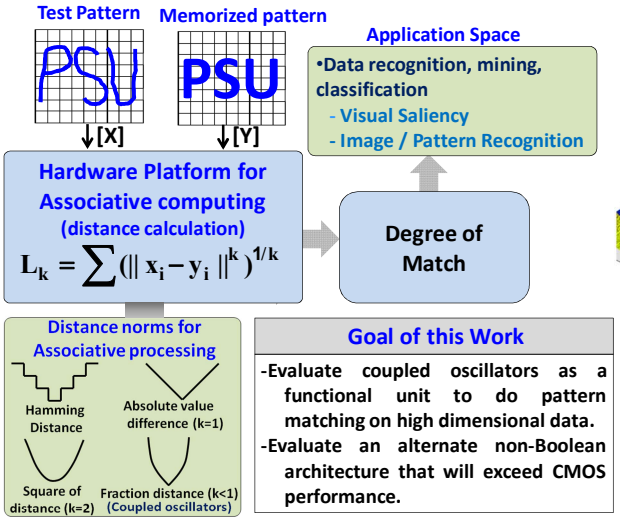


Figure 1| Motivation. We evaluate coupled oscillators as fundamental hardware block for non-Boolean associative computing. The power projection comparison of coupled oscillators with CMOS is also compared.

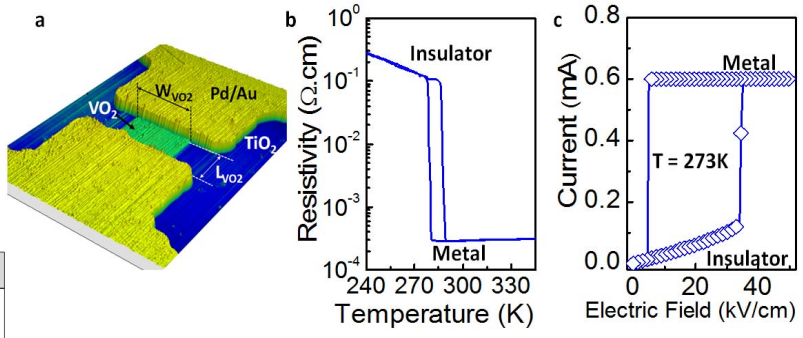


Figure 2| Metal-Insulator transition (MIT) in VO_2. (a) False colored AFM image of the two-terminal device with a strained VO_2 channel (thickness=15nm) on (001) TiO_2. (b) Typical resistivity of a compressively strained VO_2 film as a function of temperature. An abrupt change in resistivity (MIT) occurs near room temperature (c) Typical Current-Electric field characteristics of a two terminal VO_2 device showing the electrically induced MIT.

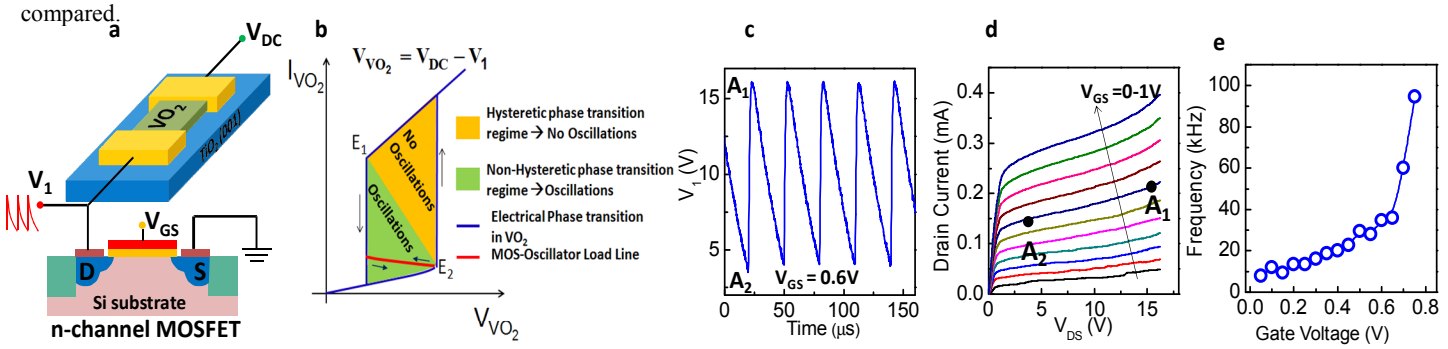
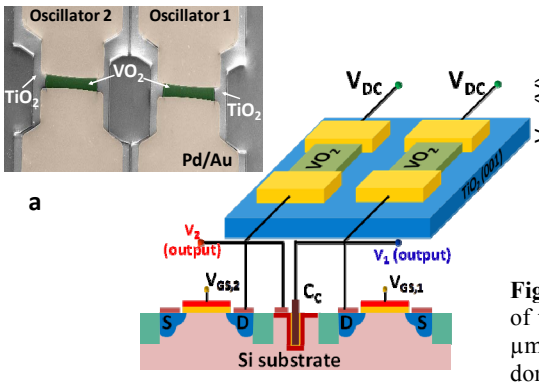


Figure 3| Hybrid VO_2-MOSFET oscillator (HVFET oscillator) with gate programmable oscillation frequency. (a) Schematic of a VO_2 relaxation oscillator consisting of a two terminal VO_2 device in series with the source-drain of a MOSFET. (L_{VO2}= 4 μm; W_{VO2}= 6μm) (b) Schematic of the operating load line (red) of a HVFET oscillator superimposed on the two terminal I-V characteristics of the VO_2 device (blue). The MOSFET induces a non-hysteretic oscillatory regime in VO_2 through negative feedback. (c) Time-Domain waveform of the HVFET oscillator. These oscillations have been shown to be stable over $2.5x10^9$ cycles. (d) Oscillation amplitude (A_1-A_2) superimposed on the output characteristics of the MSOFET.(e) Oscillation frequency as a function of gate voltage (V_{GS}) enabling VCO operation.



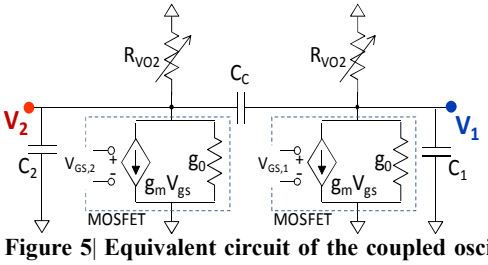


Figure 5| Equivalent circuit of the coupled oscillators. Equivalent circuit of the capacitively coupled oscillators. C_1 and C_2 are the equivalent capacitance of the VO_2 device and the output circuit of the MOSFET.

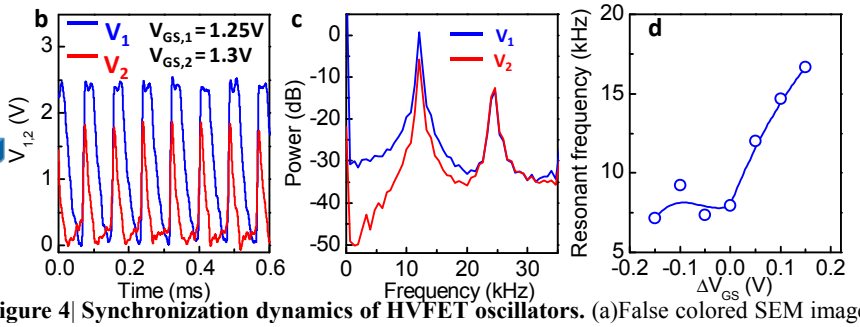


Figure 4| Synchronization dynamics of HVFET oscillators. (a)False colored SEM image of the VO_2 devices used to study their synchronization dynamics (L_{VO2}= 4 μm; W_{VO2}= 40 μm). Schematic of the capacitively coupled HVFET oscillators (C_C=2.2nF). (b) Time domain waveform of the synchronized VO_2 coupled HVFET oscillator after eliminating DC offsets ($V_{GS,1}$= 1.25V, $V_{GS,2}$= 1.3V) (c) Power spectrum of the coupled waveform in (b). (d) Variation of coupled frequency as a function of ΔV_{GS} (= $V_{GS,2}$ - $V_{GS,1}$)

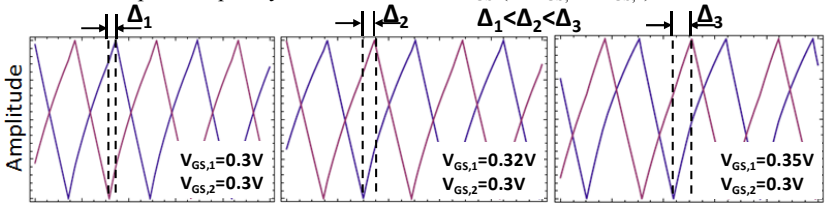


Figure 6| Input gate voltage controlled synchronization characteristics of oscillators. The relative difference (indicated by black lines) between the synchronized waveforms can be tuned and increases with ΔV_{GS}.

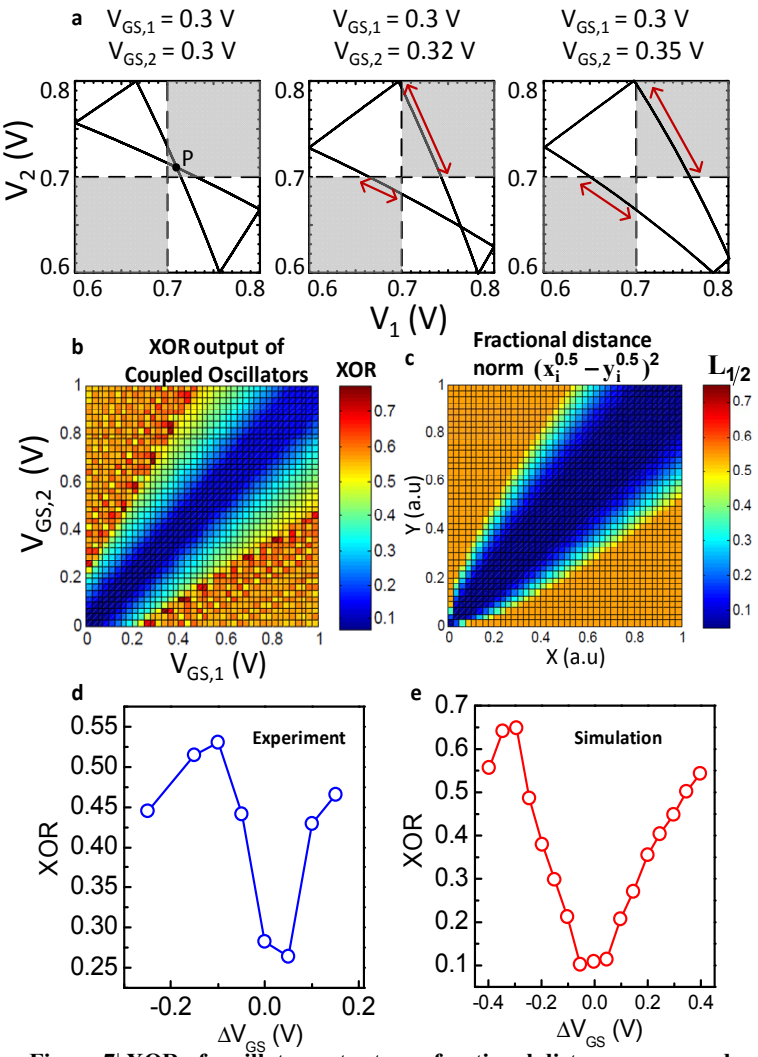


Figure 7| XOR of oscillator output as a fractional distance norm and a computing metric for pair-wise coupled oscillators. (a) Plots showing the relation between averaged XOR output of the oscillators and the steady state periodic orbit of the coupled oscillator system. The averaged XOR output is the fraction of time spent in the gray region, which also captures the phase difference between $V_{GS,1}$ and $V_{GS,2}$. (b) Simulated XOR output as a function of $V_{GS,1}$ and $V_{GS,2}$. The XOR value is minimum when $V_{GS,1}$=$V_{GS,2}$. (c) Fractional distance norm $(x_i^{0.5} - y_i^{0.5})^2$. The XOR metric computes the Euclidean distance as seen by the similarity between the (b) and (c). (d) Experimental (e) Simulated XOR as a function of ΔV_{GS}.

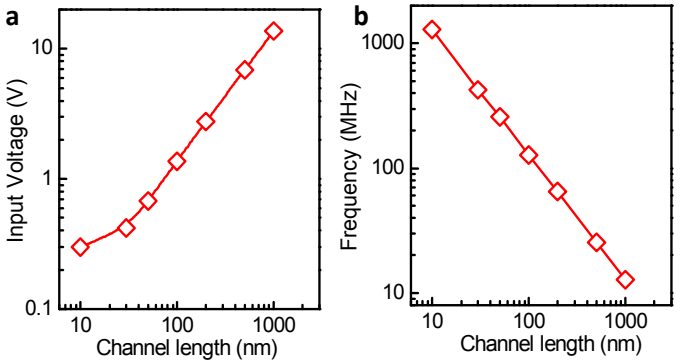


Figure 9| Projected VO_2 oscillator scaling. (a) Scaling of input DC voltage of the oscillator (b) Projected scaling of oscillator frequency with the VO_2 channel length.

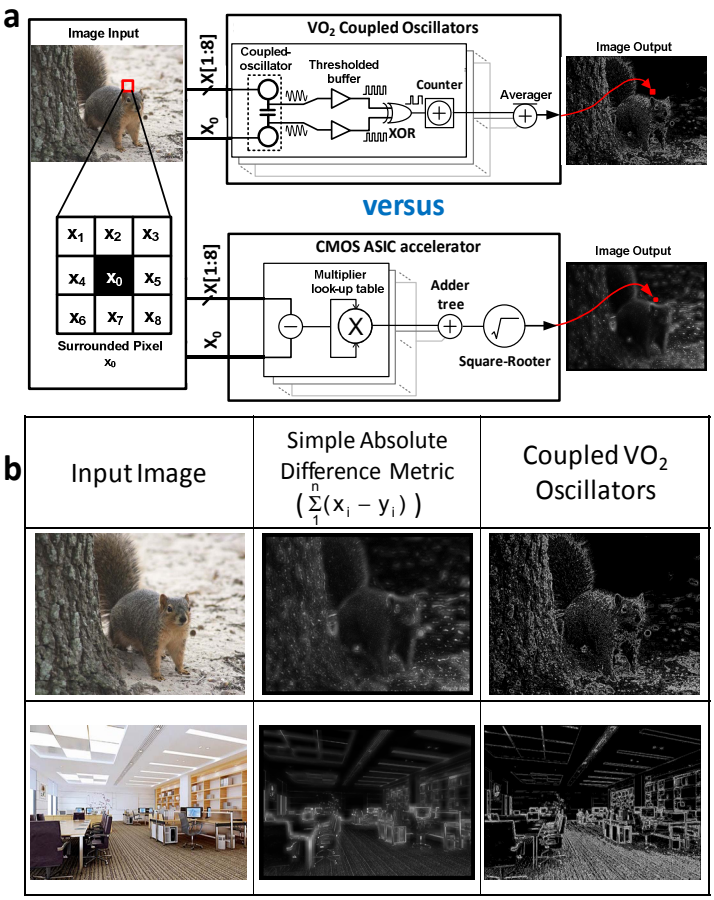


Figure 8| Visual Saliency processing using coupled HVFET oscillators and comparison with CMOS ASIC accelerator. (a) Schematic of the processing scheme for saliency detection with VO_2 coupled oscillators and CMOS ASIC accelerator. (b) Saliency detection outputs obtained with VO_2 coupled oscillators and using the simple $\sum_1^n (x_i - y_i)$ metric.

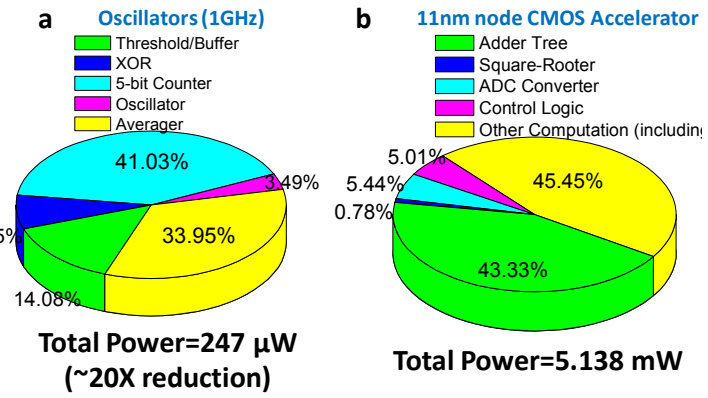


Figure 10| Power comparison. (a) Power dissipation break-down of individual components in the oscillatory processing scheme. (b) Power dissipation breakdown of individual components in a conventional synthesized CMOS ASIC processing accelerator. The Adder tree and the MAC instructions contribute to the bottle-neck in this Boolean processing scheme. All the digital circuits were implemented with 11nm node transistor models projected from the 22nm PMT model.