Tunnel FET-Based Ultra-Low Power, Low-Noise Amplifier Design for Bio-signal Acquisition

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ABSTRACT

Ultra-low power circuit design techniques have enabled rapid progress in biosignal acquisition. The design of a multi-channel biosignal recording system is a challenging task, considering the low amplitude of neural signals and limited power budget for an implantable system. The front-end low-noise amplifier is a critical component with respect to overall power consumption and noise of such system. In this paper, we present a new design of III-V Heterojunction TFET (HTFET)-based neural amplifier employing a telescopic operational transconductance amplifier (OTA) for multi-channel neural spike recording. Exploiting the unique device characteristics of HTFETs, our simulation shows that the proposed amplifier exhibits a midband gain of 39 dB, a gain bandwidth of 12 Hz-2.1 kHz, and an input-referred noise of 6.27 μVrms, consuming 5 nW of power at a 0.5 V supply voltage. Using the proposed HTFET amplifier, a noise efficiency factor (*NEF*) of 0.64 is achieved, which is significantly lower than the CMOS-based theoretical limit. Design tradeoffs related to gain, power and noise requirements are investigated, based on a comprehensive electrical noise model of HTFET and compared with the baseline Si FinFET design.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Type and Design Styles – *advanced technologies*. B.8.0 [**Performance and Reliability**]: General.

Keywords

Biomedical signal processing, Low-noise amplifier, Neural signal recording, Steep subthreshold slope, Tunnel FETs, Ultra-low power analog design.

1. INTRODUCTION

Technology advancements in micro electromechanical (MEMS) and ultra-low power, low-noise circuit designs have led to rapid progress in biosignal acquisition platforms [1-3]. With the ongoing efforts towards lightweight, miniaturized and power efficient neural recording interfaces, the potential application fields extend to various clinical domains such as diagnosis and treatment of neurological disorders including stroke, Parkinson's disease and epilepsy [4-9]. Fig. 1 illustrates a block diagram of a neural signal recording system [5]. It is composed of an electrode array for multichannel signal acquisition, an analog front-end for signal conditioning, a data processing unit for reducing the data rate of the following transmitter unit. Biosignals associated with neural activities are classified into different categories, based on their characteristics such as amplitude, bandwidth (*BW*), spatial resolution and invasiveness of the electrodes [3, 6]: electroencephalographic (EEG) (amplitude: 10~20 μV, BW < 100 Hz), electrocorticographic (ECoG) (amplitude < 100 μV, BW: 0.5~200 Hz), local field potential (LFP) (amplitude < 5 mV, BW < 1 Hz), extracellular action potential or neural spikes (amplitude < 500 μV, BW: 100 Hz~7 kHz), etc. Thus, the design objectives of biosignal acquisition systems strongly depend on the application. In general, due to the microvolt range of the neural signals and the stringent heat dissipation limit of implantable devices (< 1 ºC temperature increase to avoid tissue damage) [1, 3], the system power consumption should be sufficiently low while minimizing the device area for implantation purpose.

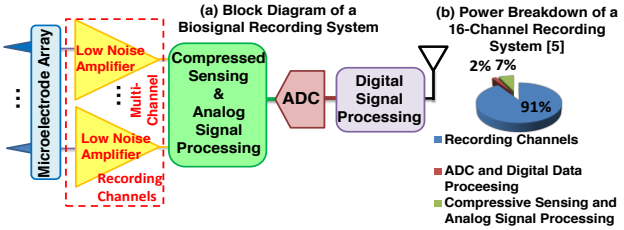

Figure 1. (a) A block diagram of a multi-channel biosignal acquisition system and (b) its power breakdown. [5]

A critical building block in a biosignal acquisition microsystem is the front-end low-noise amplifier. For spike acquisition, an input-referred noise of < 10 μVrms (lower than the background noise) and a power dissipation of < 10 μW/channel are generally required [1-9]. The large dc offsets at the issue-electrode interface should be rejected and the pass band should cover a range from hundreds of hertz to several kilohertz, while providing a high input impedance (~MΩ) to prevent the signal attenuation at the sensor [1, 3, 6]. A gain of 40 dB with sufficient common-mode rejection ratio (*CMRR*) and power-supply rejection ratio (*PSRR*) should also be ensured. The noise efficiency factor (*NEF*) is a widely accepted metric that reveals the design challenge due to the tradeoff between the input-referred thermal noise and the power reduction. Many works have explored the design techniques to reduce the *NEF* [1, 4-10] using CMOS. The subthreshold operation has been introduced for this purpose, to ensure a high transconductance (g_m) at a low bias current (I_{DS}) to reduce the input-referred thermal noise of the amplifier. However, due to the g_m/I_{DS} limit set by the *60 mV/dec* switching in CMOS,

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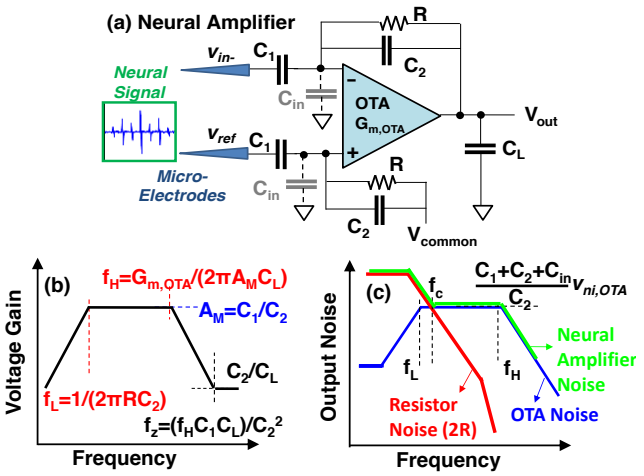


Figure 2. Neural amplifier (a) schematic and (b) gain, (b) output thermal noise characteristics [1, 4].

further reduction of NEF and power consumption of the amplifier is inherently difficult in CMOS-based neural recording systems.

The steep subthreshold slope (*SS*) Tunnel Field Effect Transistor (TFET) has emerged as a prominent candidate for low-voltage applications, taking benefit of the sub-thermal energy switching [11]. Significant progress has been made for the TFET technology such as prototype device demonstration, high-frequency switching and noise characterization, heterogeneous integration and process development [12-15]. Recent work on TFET modeling, circuit designs including variation analysis further explore its energy efficient advantages over CMOS at reduced voltages [16-18]. Authors in [16] first explored the steep SS induced high g_m/I_{DS} to scale the bias current in a SiGe TFET neural amplifier with a degraded gain of 27.7 dB. However, due to the lack of noise models, the power-noise tradeoff was not fully studied. Therefore, it is of great interest to investigate the power-noise tradeoff and explore the design optimizations using TFETs to overcome the technology barriers in neural recording systems.

In this paper, we propose a new design of a III-V Heterojunction TFET (HTFET) neural amplifier for multi-channel neural spike recording based on a shared telescopic OTA through circuit simulations to achieve gain improvement and simultaneous power and noise reduction beyond the CMOS limit. To analyze the design tradeoffs related to power-noise-performance, we apply a comprehensive noise model in [17], and explore the unique device characteristics of HTFETs for neural amplifier design compared to Si FinFETs. The reminder of the paper is as follows. In Section 2, we discuss the fundamental challenges in CMOS-based neural recording system. Section 3 shows the advantages of HTFET and the simulation setup with noise modeling details. Section 4 describes the HTFET telescopic OTA design for performance improvement of the neural amplifier including gain, power and noise. The performance evaluation of the HTFET neural amplifier is shown in Section 5, followed by conclusions.

2. POWER-NOISE CHALLENGES IN CMOS-BASED NEURAL AMPLIFIER

CMOS-based neural amplifiers have been well studied in literature. The work in [4] proposed a neural amplifier topology based on a capacitive feedback network, which has been widely adopted due to its superior area and power efficiency at a given input-referred noise [10]. Later, the authors in [9] explored the theoretical limit of NEF and achieved a significant power reduction with a modified folded-cascode OTA. Furthermore, the authors in [7] present a hardware sharing architecture suitable for multi-channel recording. To further reduce the NEF, the design in [8] utilizes a low-noise telescopic cascode topology with source-degeneration resistors. The recent work in [6] explores neural amplifier designs at a low V_{DD} of 1 V, showing good operation compatibility with digital building blocks.

Fig. 2a shows the neural amplifier topology proposed in [4]. It employs the capacitive feedback network (C_1, C_2), pseudo-resistor elements (R) and an OTA with a voltage gain of $G_{m,OTA}$. The voltage gain, A_M, of the neural amplifier is $A_M = C_1/C_2$ (Fig. 2b). The capacitive coupling rejects the dc offset from the electrode-tissue interface. The pseudo-resistor is diode-connected MOSFETs with resistance over 10^{12} Ω. The low cutoff frequency $f_L = 1/(2\pi RC_2)$. The high cutoff frequency $f_H = G_{m,OTA}/(2\pi A_M C_L)$, where C_L is the load capacitance. $C_2 \ll \sqrt{C_1 C_L}$ must be satisfied to ensure the half-plane-zero f_z higher than the operation bandwidth.

Due to the frequency range of neural signals, the minimization of low frequency flicker and thermal noise is critical. The most effective technique for flicker noise reduction consists of increasing the transistor gate area [4-10]. The thermal noise reduction, however, is constrained by the power requirement, known as power-noise tradeoff. Fig. 2c shows the output thermal noise spectrum of the neural amplifier in [4] and the noise contributions from the OTA and pseudo-resistor (in blue and red, respectively). By ensuring the corner frequency $f_c \ll f_H$, the contribution of the pseudo-resistor thermal noise is minimized. The input-referred thermal noise spectral density $\overline{v_{ni,amp}^2}$ is [1]:

$$\overline{v_{ni,amp}^2} = [(C_1 + C_2 + C_{in})/C_1]^2 \cdot \overline{v_{ni,OTA}^2} \quad (1)$$

where C_{in} is the OTA input capacitance and related to the gate area of the input pair. $\overline{v_{ni,OTA}^2}$ is the OTA input-referred noise. A general expression for $\overline{v_{ni,OTA}^2}$ over a -3dB bandwith of BW is approximated as [1, 7, 9]

$$\overline{v_{ni,OTA}^2} = [\frac{4k_BT}{g_{m,input}}(\frac{1}{\kappa} + \beta\frac{g_{m,load}}{g_{m,input}})] \cdot \frac{\pi}{2} \cdot BW \quad (2)$$

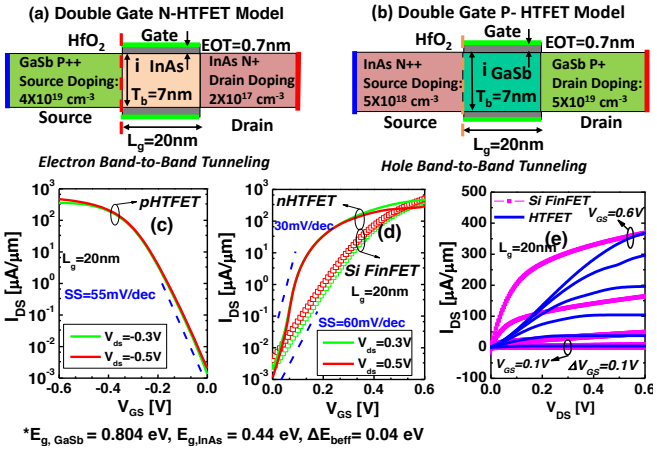
where $g_{m,input}$ and $g_{m,load}$ are the transconductances of the input pair and load transistors in the neural amplifier, respectively. β relates to different OTA topologies and has a value larger than 1. κ is the subthreshold gate coupling factor: $SS = V_t/\kappa \cdot ln10$, where V_t is the thermal voltage (k_BT/q) and k_B is Boltzmann constant. According to Eq. (1) and (2), to minimize $\overline{v_{ni,amp}^2}$, we must size the transistors to maximize $g_{m,input}$ and $g_{m,input}/g_{m,load}$. Hence, at a fixed bias current, the input and load transistors are sized to operate in weak inversion (high g_m/I_{DS}) and strong inversion (low g_m/I_{DS}), respectively. However, to reduce the power dissipation, a severely downscaled I_{DS} is required, which in turn reduces $g_{m,input}$ due to the 40 V^{-1} g_m/I_{DS} limit of CMOS. Furthermore, the reduced voltage headroom at low-V_{DD} also degrades the $g_{m,input}/g_{m,load}$. The essence of the power-noise tradeoff is indicated by the NEF [1, 4],

$$NEF \equiv v_{ni,rms}\sqrt{I_{OTA}/(\pi/2 \cdot V_t \cdot 4k_BT \cdot BW)} \quad (3)$$

where I_{OTA} is the total bias current of the OTA, $v_{ni,rms}$ is the rms value of the input-referred noise. Assuming $(C_1+C_2+C_{in})/C_1 \approx 1$, $\beta \cdot g_{m,load}/g_{m,input} \ll 1$, and substituting Eq.(1) and (2) into (3):

$$NEF \approx \sqrt{I_{OTA}/(\kappa \cdot V_t \cdot g_{m,input})} \quad (4)$$

NEF=1 is the theoretical limit in an ideal single-stage bipolar amplifier with only thermal noise considered, while NEF>1 is



*$E_{g,\ GaSb}$ = 0.804 eV, $E_{g,InAs}$ = 0.44 eV, ΔE_{beff}= 0.04 eV

Figure 3. Schematics and model parameters for (a) N-HTFETs (b) P-HTFETs, and device characteristics of (c-d) I_{ds}-V_{gs} and (e) I_{ds}-V_{ds} , comparing with the baseline Si FinFET [17].

applied to all CMOS-based circuits. The minimum *NEF* is calculated as 2.02 (assuming $I_{OTA}=2I_{DS}$ and $\kappa=0.7$ for the input pair) for any CMOS neural amplifier using a differential input pair [9], which can be moderately reduced through reference branch-sharing in multi-channel designs [7]. Thus, the power-noise tradeoff in CMOS neural amplifiers inherently limits the design of large-scale multi-channel biosignal acquisition systems.

3. TFETS FOR NEURAL RECORDING APPLICATIONS

3.1 TFET Technology: Advantages of Power-Noise Tradeoff in Neural Amplifier Designs

The fundamental limit of g_m/I_{DS} in CMOS originates from the thermal energy slope of k_BT, which results in an over *60 mV/dec SS*. In TFETs, the interband tunneling induced carrier injection mechanism overcomes the thermal energy limit, leading to a *sub-60 mV/dec SS*. Thus, an improvement of g_m/I_{DS} can be achieved in TFETs with SS reduction (Eq. (5)).

$$\frac{g_m}{I_{DS}}=\frac{\partial I_{DS}}{\partial V_{GS}}\frac{1}{I_{DS}}=\frac{\partial lnI_{DS}}{\partial V_{GS}}=\frac{ln10\,\partial\log I_{DS}}{\partial V_{GS}}=\frac{ln10}{SS}=\frac{\kappa}{V_t} \quad (5)$$

In this work, we apply the calibrated GaSb-InAs heterojunction TFET (HTFET) models (Fig. 3a-e) reported in [17], which are based on a double-gate device structure with L_g = *20 nm*. The device characteristics of g_m/I_{DS} vs. I_{DS} and g_m/I_{DS} vs. V_{GS} are shown in Fig. 4, comparing HTFETs and Si FinFETs. The improved g_m/I_{DS} at low voltage and low I_{DS} provides following advantages in HTFET-based neural amplifier design:

1) Avoiding $G_{m,OTA}$ degradation at low bias current (I_{DS}). A high $G_{m,OTA}$ can ensure a low-noise stable operation of an amplifier. At severely scaled I_{DS}, the high g_m/I_{DS} of HTFETs can significantly improve $g_{m,input}$ compared to Si FinFETs. Hence, a desired $G_{m,OTA}$ can be maintained without increasing the circuit complexity using HTFETs.

2) Reducing $\overline{v_{ni,OTA}^2}$ with high $g_{m,input}$ and $g_{m,input}/g_{m,load}$ ratio at low I_{DS}. The steep SS leads to a reduced bias voltage difference to obtain a high $g_{m,input}/g_{m,load}$ ratio. For example, one order change of g_m/I_{DS} is achieved within a 0.2 V window (Fig. 4a), which reduces the overdrive voltage and hence is suitable for low V_{DD} operation.

3) Enabling V_{DD} scaling to reduce the power consumption (V_{DD}·I_{OTA}) benefitted from the low-V_{DD} operation of HTFETs.

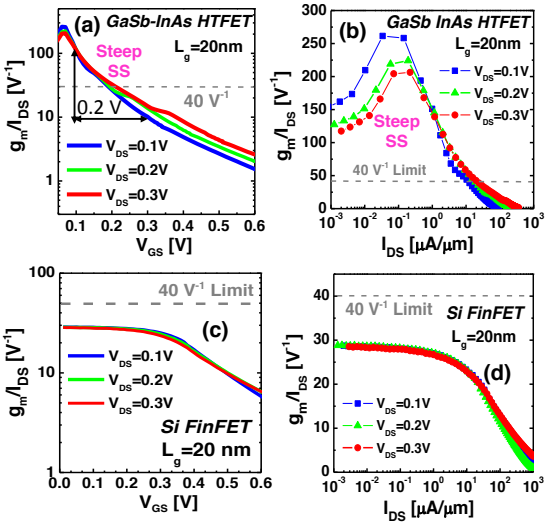


Figure 4. g_m/I_{DS} characteristics comparison of HTFETs (a, b) and Si FinFETs (c, d). The device models are from [17].

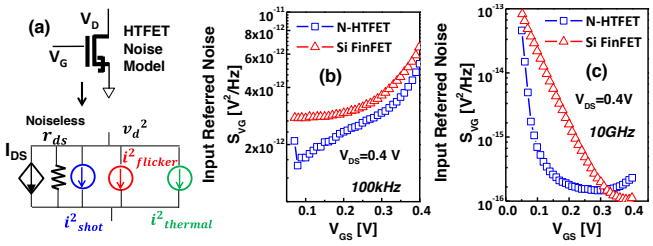


Figure 5. Electrical noise Verilog-A modeling and input-referred noise comparison [17].

4) Reducing the *NEF* by suppressing the thermal energy slope. A steep *SS* in TFET results in $\kappa>1$. Substituting (5) to (4), the minimum NEF of a TFET neural amplifier ($NEF_{TFET,min}$) is lower than the CMOS limit ($NEF_{CMOS,min}$):

$$NEF\approx\sqrt{\frac{I_{OTA}}{I_{DS}}\Big/\left(\frac{\kappa\cdot V_t\cdot g_{m,input}}{I_{DS}}\right)}=\frac{1}{\kappa}\sqrt{\frac{I_{OTA}}{I_{DS}}}=\frac{SS}{V_t ln10}\sqrt{\frac{I_{OTA}}{I_{DS}}} \quad (6)$$

$$NEF_{TFET,min}=NEF_{CMOS,min}\cdot\frac{SS_{TFET,input\ pair}}{SS_{CMOS,input\ pair}} \quad (7)$$

where $SS_{TFET,input\ pair}$ and $SS_{CMOS,input\ pair}$ stand for the *SS* of the input pair of the TFET OTA and Si FinFET OTA, respectively.

3.2 HTFET Noise Modeling and Circuit Simulation Setup

To design the HTFET neural amplifier, we apply the calibrated Verilog-A device models incorporated with the electrical noise model [17] for HTFETs, and compare the results with the baseline Si FinFET design. The electrical noise model is derived from experimentally validated analytical models, which includes thermal, shot noise and low frequency flicker noise. (The random telegraph noise (RTN) is omitted due to the large transistor gate area in our design.) The modeled noise characteristics comparing HTFETs and Si FinFETs are shown in Fig. 5, where HTFETs exhibit a competitive input-referred noise in the kHz and MHz range compared to Si FinFETs at an operation voltage of 0.3 V. The circuit simulation is performed using Cadence Spectre [19].

4. HTFET BASED ULTRA-LOW-POWER, LOW-NOISE OTA

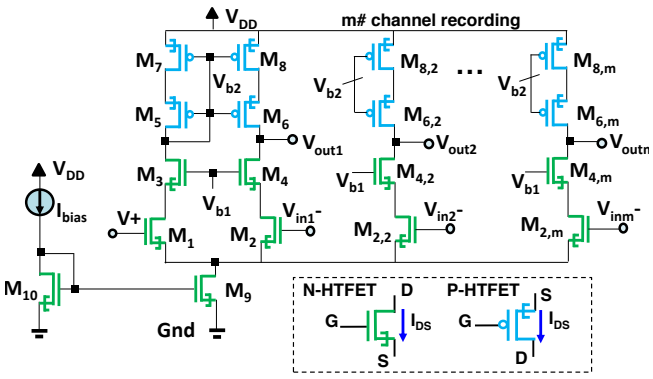


Figure 6. HTFET based telescopic OTA design with sharing architecture for multi-channel recording.

Table 1. Transistor Sizing of the HTFET Telescopic OTA

	W/L [$\mu m/\mu m$]	g_m/I_{ds} [V^{-1}]	V_{ds} [mV]	V_{gs} [mV]
$M_{1,2}$	50/1	**253**	67	50
$M_{3,4}$	1/50	202	150	73
$M_{5,6}$	1/10	40	-92	-92
$M_{7,8}$	0.2/40	**35**	-81	-179
$M_{9,10}$	0.2/10	169	109	82

Table 2. Transistor Sizing of the Si FinFET Telescopic OTA

	W/L [$\mu m/\mu m$]	g_m/I_{ds} [V^{-1}]	V_{ds} [mV]	V_{gs} [mV]
$M_{1,2}$	100/2	**28.7**	220	40
$M_{3,4}$	30/0.2	28.6	79	21
$M_{5,6}$	8/0.2	28.55	-68.4	-68.4
$M_{7,8}$	0.1/80	**9.8**	-423	-492
$M_{9,10}$	2/2	27	209	205

4.1 HTFET-Based Telescopic OTA

A modified telescopic OTA topology, inspired from [7] is employed by the HTFET-based OTA (Fig. 6), which utilizes a partial OTA sharing architecture for multi-channel recording. A N-HTFET input pair is used due to its steeper *SS* (Fig. 3c-d) induced larger g_m/I_{DS}. Cascoded M_3-M_6 are used as gain booster without increasing the input-referred noise-level. Table 1 shows the bias conditions of each transistor in the HTFET OTA. The bias current is 10 nA at V_{DD}=*0.5 V*, providing a 5 nA bias current for M_1-M_8. As discussed in Section 2, to maximize the $g_{m1,2}$ of the input differential pair $M_{1,2}$, a large *W/L* ratio is used to achieve high g_m/I_{DS}. Similar to the reported CMOS designs [4-9], a large gate-area (WxL) is used to reduce the flicker noise contribution. For $M_{7,8}$, on the other hand, a minimized W/L is applied to bias the device into strong inversion with small g_m/I_{DS}, which increases the ratio of $g_{m1,2}/g_{m7,8}$ and reduces the thermal noise contribution of $M_{7,8}$. Since the cascoded M_3-M_6 have a negligible contribution to the total input-referred noise, the choice of the sizing for these transistors is based on gain requirement. The balance of the output resistance and intrinsic gain is carefully considered for M_3-M_6. As a result, a high g_m/I_{DS} of 253 V^{-1} is obtained for $M_{1,2}$, while a g_m/I_{DS} of 35 V^{-1} is used for $M_{7,8}$, resulting $g_{m1,2}/g_{m7,8} \approx 7.2$.

For performance comparison, we design a Si FinFET OTA as a baseline with a similar topology and bias current (10 nA). A supply voltage of 1 V is required in Si FinFET OTA due to the overdrive voltage requirement of the stacked devices. Similarly, $M_{1,2}$ operate in subthreshold regime while $M_{7,8}$ are biased in strong inversion regime, using the sizes presented in Table 2. However, due to the limited g_m/I_{DS} and diminished overdrive voltage, $g_{m1,2}$ and the ratio of $g_{m1,2}/g_{m7,8}$ *(≈3)* are significantly decreased at such low-power level, which is detrimental to noise performance.

4.2 Performance Analysis

Fig. 7a shows the HTFET OTA gain vs frequency for a single channel compared to the baseline Si FinFET OTA. Benefiting from its high g_m/I_{DS} and the cascoding technique, an open-loop gain of 50 dB is achieved in the HTFET OTA at V_{DD}=*0.5 V*,

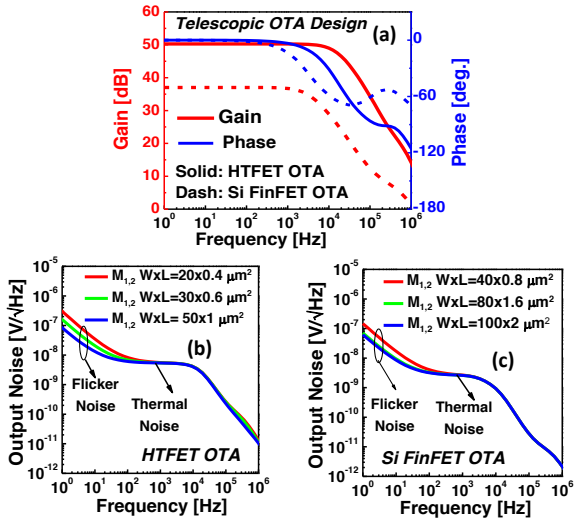


Figure 7. Voltage gain (a) and output noise vs. frequency (b-c) of HTFET and Si FinFET OTAs.

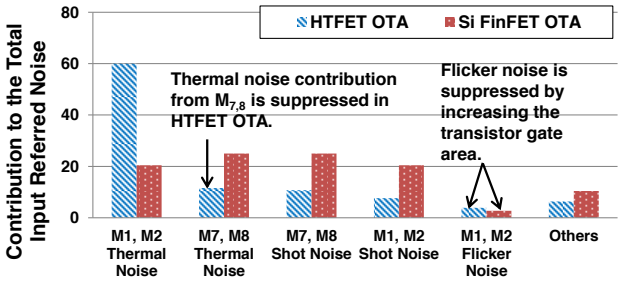


Figure 8. Noise contribution of each transistor to the overall input-referred noise from 10Hz to 1 kHz.

whereas the Si FinFET OTA shows a degraded gain of 37 dB at V_{DD}=*1 V* due to extremely limited bias current. The output noise spectrum vs frequency is shown in Fig.7b-c, where the thermal noise dominates the flicker noise which is suppressed owing to the large gate-area of the input pair.

The dominant noise contributor of each transistor and its contribution to the overall input-referred noise is shown in Fig. 8. In the Si FinFET OTA, $M_{7,8}$ contribute to a significant portion of the overall input-referred noise due to the degradation of $g_{m1,2}$ and $g_{m1,2}/g_{m7,8}$. In contrast, an effective suppression of the thermal noise contribution from $M_{7,8}$ is achieved in the HTFET OTA, given its high g_m/I_{DS}. The desired open-loop gain, ultra-low power and competitive noise performance achieved by the HTFET telescopic OTA confirm its advantage for neural amplifier design.

5. THE HTFET NEURAL AMPLIFIER FOR MULTI-CHANNEL BIOSIGNAL RECORDING

5.1 Closed-loop HTFET Neural Amplifier

Using the capacitive feedback topology, we implement the closed-loop HTFET neural amplifier based on the proposed telescopic OTA (Fig. 9). To further eliminate the redundant dc bias circuitry, we use the dc output voltage of the OTA ($V_{out,dc}$) to bias the common voltage (V_{common}) of the input signal through the resistive divider network (R_b) *at* $V_{common}=V_{out}$. In the OTA simulation, the common dc voltage of the input signal, $V_{in,dc}$, is set to $1/2V_{out,dc}$. Hence, by setting $R_b=R$, the input signal can be biased at

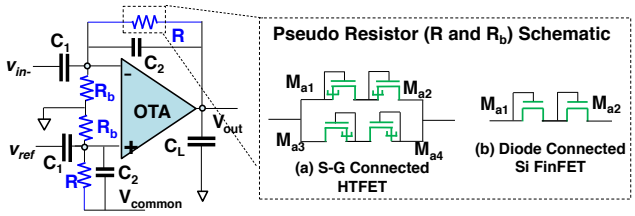


Figure 9. Closed-loop neural amplifier topology and pseudo resistor schematics.

$1/2V_{out,dc}$. A diode connected Si FinFET as in [1, 4-10] is used to construct the pseudo-resistor R_b and R for the Si FinFET neural amplifier, where a W/L of 0.2 µm/8 µm is used for M_{a1-2} (Fig. 9b). For the HTFET neural amplifier, shorted source-gate connections [16] can be applied by taking advantage of the asymmetrical source/drain characteristic, while an additional conduction path through M_{a3-4} (Fig. 9a) is required due to the uni-directional transistor characteristics. A W/L of 0.2 µm/6 µm is applied to M_{a1-4} in the HTFET neural amplifier. The values of the capacitors are selected as $C_2 = 500\ fF$, and $C_1/C_2 = 100$ to provide a 40 dB mid-band gain. C_L is varied from 500 fF to 2 pF to tune the pass band of the amplifier. For the Si FinFET neural amplifier, $C_2 = 500\ fF$ and $C_1/C_2 = 50$ are used, due to the degraded open-loop gain.

5.2 Voltage Gain and Noise Performance

The gain and output noise vs. frequency characteristics are shown in Fig. 10, comparing HTFET and Si FinFET neural amplifier designs at different load capacitor conditions (f_H decreases as C_L increases). A midband gain of 39.4 dB is achieved in the HTFET neural amplifier, as compared to 28.1 dB in the Si FinFET neural amplifier. This gain advantage of the HTFET neural amplifier arises from the improved g_m originating from the steep SS induced high g_m/I_{DS}. The output thermal noise spectrum exhibits similar characteristics as in Fig. 2c, for both Si FinFET and HTFET neural amplifiers. For a frequency range below 10 Hz, the noise contribution from the pseudo-resistor dominates the overall output noise, while the thermal noise of the OTA dominates the frequency range between f_L and f_H. As discussed in Section 2, the low cutoff frequency f_L is determined by R and C_2, while C_1/C_2 is constant. Thus, the bandwidth of the designed neural amplifier can be tuned by varying R (R_b) and C_2 to satisfy the operational bandwidth requirement in different application domains.

5.3 Power-Noise Tradeoff

The input-referred noise spectrum for HTFET and Si FinFET neural amplifiers are shown in Fig. 11a. At the same I_{bias} of 10 nA, the HTFET neural amplifier exhibits over 4 times reduction of the input-referred noise within the pass band compared to the Si FinFET neural amplifier. Moreover, reducing the input-referred noise of the Si FinFET neural amplifier can only be achieved by degrading its power performance. When increasing I_{bias} by 4 times (40 nA) and 16 times (160 nA) while increasing all the transistor widths accordingly (4 times at $I_{bias} = 40\ nA$, 16 times at $I_{bias} = 160\ nA$), the input-referred noise of the Si FinFET neural amplifier is reduced by 2 times and 4 times, respectively. Such noise reduction is due to the increased $g_{m1,2}$ of the OTA at a fixed g_m/I_{DS} (at a constant NEF). The Si FinFET neural amplifier shows comparable input-referred noise at $I_{bias} = 160\ nA$ and $V_{DD} = 1\ V$ as the HTFET neural amplifier at $I_{bias} = 10\ nA$ and $V_{DD} = 0.5\ V$. Hence, an approximate 32 times power reduction over the Si FinFET design is achieved in the HTFET neural amplifier, considering the design target to obtain the same input-referred noise level.

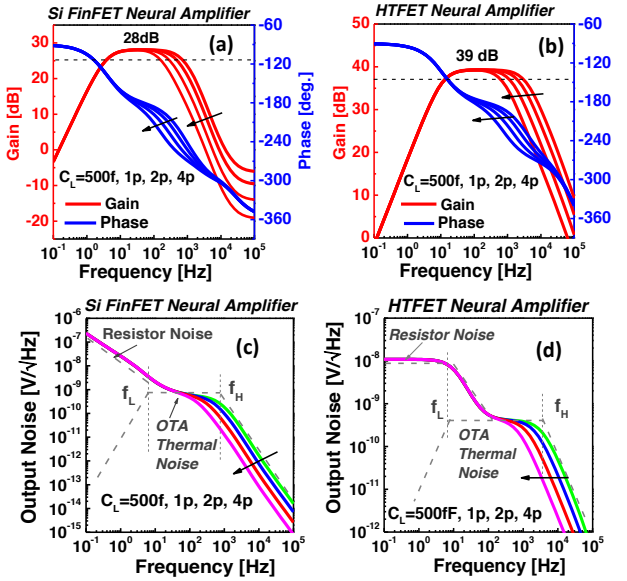


Figure 10. Si FinFET(a, c) and HTFET(b, d) neural amplifier gain vs. frequency and output noise vs. frequency.

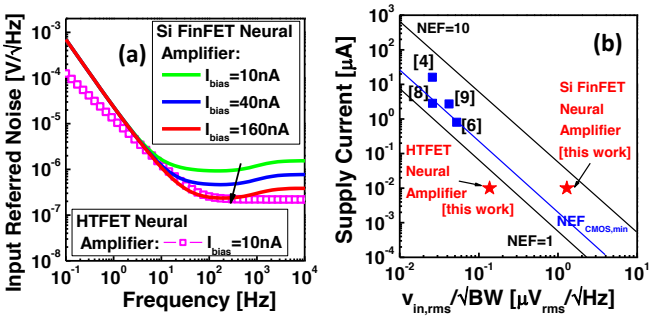


Figure 11. (a) Input referred noise spectrum for HTFET and Si FinFET neural amplifiers and (b) Supply current vs. $v_{in,rms}/\sqrt{}$bandwidth for NEF benchmarking.

The performance metrics of the HTFET and Si FinFET neural amplifiers at $C_L = 2\ pF$ and $I_{bias} = 10\ nA$ are summarized in Table 3 and compared with other designs [4, 6, 8, 9, 16]. A bandwidth of 12 Hz (f_L) to 2.1 kHz (f_H) and power consumption of 5 nW are achieved in the HTFET design with an input-referred noise of 6.27 µVrms integrated over 10 Hz to 1 kHz, which is close to the estimated minimum $v_{ni,rms}$ of 5.26 μV_{rms} achieved by an ideal OTA at $C_L = 2\ pF$ and $A_M = 40\ dB$ [1]. The Si FinFET neural amplifier, however, shows a bandwidth from 4 Hz to 529 Hz at the same I_{bias} (10 nA), while f_H is degraded due to the limited g_m. The increased $v_{ni,rms}$ at nanowatt power levels imposes inevitable drawbacks on practical applications of the Si FinFET amplifier. Both *CMRR* and *PSRR* are improved in the HTFET amplifier compared to the Si FinFET design. A competitive linearity performance of the HTFET and Si FinFET amplifiers, indicated by the total harmonic distortion (*THD*), is also achieved (compared to Si FinFET, the impact of I_{ds}-V_{gs} non-linearity in HTFET is compensated by the stable operation bias at low-V_{DD}). For a single-channel, the total transistor area of 259.2 μm^2 is achieved in HTFET amplifier compared to 452 μm^2 in Si FinFET amplifier.

Compared to the reported CMOS designs, the HTFET neural amplifier exhibits superior power-noise performance (Fig. 11b). A *NEF* of 0.64 (Table 3) is obtained in the HTFET neural amplifier

Table 3. Performance Comparison with Other Simulation Works

	HTFET Amplifier (this work)	FinFET Amplifier (this work)	Shoaran 2012 [8]	Trivedi 2013 [16]
Technology	20 nm HTFET	20 nm Si FinFET	.18 µm CMOS	90 nm SiGe TFET
Bias Current	10 nA	10 nA	2.84 µA	~3 nA
Supply Voltage	0.5 V	1 V	1.8 V	1 V
Power	5 nW	10 nW	5.11 µW	3.6 nW
Closed-loop Gain	39.4 dB	28.1 dB	39.9 dB	27.7 dB
Bandwidth (f_L-f_H)	12 Hz-2.1 kHz (C_L=2 pF)	4 Hz-529 Hz (C_L=2 pF)	30Hz-2.5kHz (tunable)	0.036 Hz-3.2 kHz (N/A)
Input-Referred Noise	6.27µVrms (10Hz - 1kHz)	29.7µVrms* (10Hz-1kHz)	1.30 µVrms (1Hz-100kHz)	3.1 µVrms** (N/A)
CMRR	56 dB	42 dB	78 dB	64 dB
PSRR	70 dB	58 dB	57 dB	55 dB
THD	0.69% (2 mV_{p-p})	0.67% (2 mV_{p-p})	-	-
NEF	*0.64*	*5.2*	*1.94*	-

*At I_{bias}=160 nA, integrated input-referred noise of the Si FinFET neural amplifier from 10Hz to 1kHz is 6.99 µVrms with corresponding 16x increase of transistor width. ** Tunnel diode noise model at a fano factor of 1 for shot noise were used for [16] with thermal noise neglected.

owing to the steep SS, which outperforms the *NEF* of 5.18 in the baseline Si FinFET design. This low *NEF* achieved by the HTFET design also outperforms the optimal *NEF* for both CMOS ($NEF_{min}=2.02$) and Bipolar ($NEF_{min}=1$) based designs. Moreover, the new HTFET neural amplifier shows significant gain improvement compared to the SiGe TFET design in [16], benefiting from the cascaded transistors and steeper *SS* of III-V HTFETs. The telescopic OTA topology employed by our design is also known to be more power-noise efficient [7, 8] compared to the symmetrical current-mirror OTA topology in [16]. The comparison of the noise performance cannot be applied here because of the different assumption of the Fano factor for shot noise and neglecting of the thermal and flicker noise in [16].

6. CONCLUTIONS

In this paper, we investigate the unique device characteristics of steep slope HTFET for multi-channel biosignal acquisition. By exploring the high g_m/I_{DS} characteristics, we propose a new HTFET neural amplifier design using a shared telescopic OTA topology to enable a nanowatt power-level operation, which also provides a voltage gain improvement and noise reduction compared to the Si FinFET-based design. Using a comprehensive noise model, we analyze the power-noise tradeoff in HTFET neural amplifier designs, which highlights advantages of the steep SS and low-V_{DD} operation for mitigating the aggravated thermal noise limit from the power reduction. At a highly downscaled bias current of 10 nA and supply voltage of 0.5 V, our proposed HTFET neural amplifier design exhibits a midband gain of 40 dB, a -3dB bandwidth from 12 Hz to 2.1 kHz, and an approximate 32 times power reduction over the baseline Si FinFET design to achieve the same input-referred noise level. The performance evaluation further reveals the superior power-noise efficiency of the HTFET-based design, including a *NEF* of 0.64 significant lower than the theoretical *NEF* limits using CMOS or Bipolar technologies. The remarkable performance improvement and desired power-noise tradeoff confirm the advantages of HTFET technology for multi-channel biosignal acquisition system, offering new perspectives to overcome the CMOS technology barrier for ultra-low power analog applications.

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