Device Circuit Co Design of FEFET Based Logic for Low Voltage Processors

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***Abstract*— Ferroelectric FETs (FEFETs) are emerging devices with potential for low power applications. The unique feature which makes these devices suitable for ultra-low voltage operation is the steep slope achieved by negative capacitance of the ferroelectric oxide based gate stack. This property is being actively explored to overcome the fundamental 60 mV/decade sub threshold swing limit associated with conventional MOSFETs. In this paper, we focus on the circuit implications of the steep slope behavior of the FEFETs. We analyze the characteristics of FEFETs to get insights into their performance, and show both higher ON current and higher gate capacitance compared to standard transistors. We design and simulate a ring oscillator and a Kogge Stone adder using FEFET devices and evaluate the impact of ferroelectric layer thickness on the performance. Our analysis shows that FEFET based circuits consume lower energy compared to CMOS circuits at V_{DD} < 0.17V at iso delay for the Kogge Stone adder. For example, we get 9.21% energy reduction at ferroelectric layer thickness of 3nm and 36% energy reduction for a ferroelectric layer thickness of 6nm at the iso carry path delay of 3.1 ns for an 8 bit Kogge Stone adder.**

Keywords- FEFETs; NCFETs; Kogge Stone Adder; Low Power Processor;

I. INTRODUCTION

The design of ultra-low power integrated circuits has been an active area of research, especially with the rise in the demand for portable electronics, implantable bio-medical devices, battery operated systems and energy harvesting nonvolatile processors [1]. The key solution to power reduction is usually linked to low supply voltage and technology scaling. However, one issue with reducing the supply voltage is the challenge to achieve a sufficiently high ON-state current with a fixed OFF current. This challenge is related to the fundamental limitation of standard transistors that the sub-threshold swing cannot reduce below 60mV/decade at room temperature. As an alternative, steep slope devices are being actively explored to tackle this challenge [2] [3]. Steep slope is beneficial for logic devices to be operated at ultra-low voltages.

Fig. 1(a) shows the transfer characteristics of a standard transistor and a steep slope transistor, depicting lower sub-threshold swing in the latter device, which enables aggressive supply voltage (V_{DD}) scaling. Tunnel FET (TFET) devices and ferroelectric FETs (Negative Capacitance FETs) are two of the most popular steep slope devices. TFETs use the inter-band tunneling mechanism to achieve lower sub threshold swing [4] [5]. One drawback of

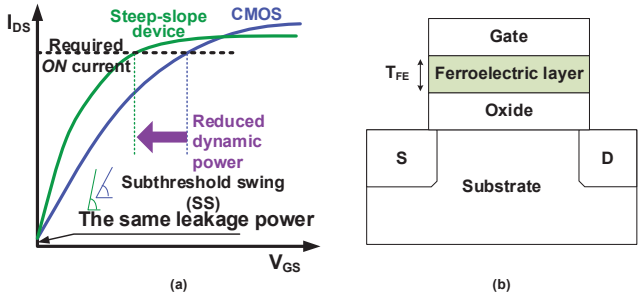

Figure 1. (a) Steep Slope Characteristics; (b) FEFET structure;

TFETs is unidirectional current flow, which raises challenges when designing circuits like SRAMs and flip-flops [6]. In contrast to TFETs, ferroelectric FETs (FEFETs) utilize the negative capacitance of the ferroelectric layer [7-10] to obtain voltage amplification at the gate of the transistor leading to the steep switching behavior.

FEFETs exhibit distinctive properties like steep slope behavior and hysteresis in their drain current (I_{DS}) versus gate voltage (V_{GS}) characteristics [7] [11]. The slope in the $I_{DS} - V_{GS}$ of the FEFET increases with the thickness of the ferroelectric layer (Fig. 3) sandwiched between the gate and oxide of the transistor (Fig. 1(b)). Increase in the ferroelectric layer thickness beyond a certain value leads to hysteresis, which may not be useful for the design of high speed logic gates. However, it is possible to tailor the hysteresis to span the positive and negative V_{GS}, which enables the FEFET to be used as a non-volatile memory device [7]. An interesting aspect of the FEFETs is that they offer a potential to design non-volatile memories and low power logic circuits with the same underlying device structure.

Steep slope devices are attractive as ultra-low power devices due to the comparatively high ON current (I_{ON}) at low voltages. However, the unique gate structure of the FEFETs also leads to high input gate capacitance. Since the power consumption and delay of a circuit are a strong function of its gate capacitance and I_{ON}, there is a need to investigate the performance of FEFET as a low power device by performing proper circuit analysis.

In this work, we carry out extensive analysis of the FEFET-based logic devices and circuits to understand the benefits and trade-offs of FEFETs as post-CMOS devices. We evaluate the delay and energy characteristics as a function of the thickness of the ferroelectric layer and supply voltage (V_{DD}) to find the behavioral trends of the

FEFET circuit. First, we simulate a seven stage ring oscillator to get insights into the device-circuit interactions for a range of supply voltages. Then we analyze a Kogge-Stone adder to understand the implications of FEFET based devices in larger functional blocks and carry out a performance comparison with the corresponding CMOS circuits. In this work we focus on the evaluation of FEFETs as a low power logic device only. The analysis of FEFETs for non-volatile memory design requires separate analysis [7] [12-13] and is beyond the scope of this work.

This paper makes the following contributions

1. Analysis of the FEFET device –circuit based on ring oscillator and Kogge Stone adder designs.
2. Analysis of the impact of the ferroelectric layer thickness on FEFET based circuits.
3. Exploration of the implications of FEFETs as logic component for future processors.

II. Background and Motivation

In this section, we present a brief discussion on the FEFET device to lay the groundwork for the rest of the paper. FEFETs are designed by adding a ferroelectric layer in the gate stack of the transistors (Fig. 1(a)). Ferroelectric FETs achieve lower subthreshold swing by virtue of the negative capacitance of the ferroelectric (FE), due to which an increase in the voltage produces a negative change in the polarization (Fig. 2(b)). The sub threshold swing (S) can be expressed as

$$S = \frac{d V_G}{d \log_{10}(I_{DS})} = \frac{d V_G}{d \Psi_S} \frac{d \Psi_S}{d \log_{10}(I_{DS})} = M \times N \quad (1)$$

where V_G is the gate voltage, I_{DS} is the drain current and Ψ_S is the channel potential [8-10]. Sub threshold swing can be improved by increasing 'M 'and 'N' factors in equation 1. Technologies like TFET [8] modify the transport factor N, whereas FEFET modifies the body factor M by using the negative capacitance of the ferroelectric to induce voltage amplification of the gate voltage.

Ferroelectrics are materials with a high polarizability. The behavior of the ferroelectric layer capacitance can be captured by the time-dependent Landau-Khalatnikov (LK) equation given below [10]

$$E = \alpha P + \beta P^3 + \gamma P^5 + \rho \, dP/dt. \quad (2)$$

where E represents the electric field, P represents the polarization ,α, β, γ are the static constants and ρ is the kinetic coefficient. The electric field (E) versus polarization (P) behavior of the ferroelectric capacitor is plotted in Fig. 2(b). From Fig. 2(b) we can see that there is a portion in the PE curve where the slope is negative. This portion represents the negative capacitance. The operation of the

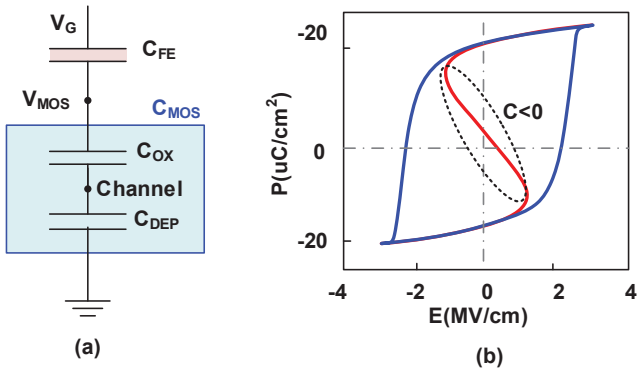

Figure 2. (a) Transistor capacitance model; (b) PE loop of ferroelectric capacitor [10].

FEFETs can be analyzed with a simple equivalent capacitance representation shown in Fig. 2(a) where C_{FE} represents the ferroelectric layer capacitance and the combination of Cox and C_{DEP} represents the underlying MOSFET capacitance [7]. The unique properties of FEFETs are obtained by the interaction between the negative capacitance of the ferroelectric layer and the positive capacitance of the underlying transistor. For example the steep slope is obtained by the voltage boost as a result of the interplay between the capacitances with the condition that $|C_{FE}| > C_{MOS}$. The voltage step-up ($=|C_{FE}|/(|C_{FE}|-C_{MOS})$ – see Fig.2(a)) can be varied by the changing the C_{FE} , which can be achieved by altering the ferroelectric layer thickness[7]. Increase in the thickness of the ferroelectric layer (FE) leads to reduction in $|C_{FE}|$, which increases the voltage gain and lowers the sub-threshold swing. Increase in thickness of FE beyond a certain point leads to emergence of hysteresis in the transfer characteristics, which is typically avoided for logic applications. Though FEFET devices are essentially steep slope devices by virtue of their ferroelectric layer negative capacitance, there is a need to investigate whether the low voltage steep slope will be translated to low power operation when implemented in bigger circuits [14]. The speed of operation of a device can be roughly estimated by CV/I metric where C is the gate capacitance, V is the supply voltage and I is the drive current of the device. The effective capacitance of the FEFET is governed by the complex interactions between its positive and negative capacitances. To get the lower power operation at iso delay for FEFET, *C*, *V* and *I* have to be optimized for which insights into the device operation is necessary. In order to build a FEFET logic processor, hysteresis free device operation is preferred. Since FEFETs are complex device with strong correlation between device parameters and its functional and electrical performance, we have performed a device–circuit simulation analysis to understand the performance implications of FEFET based circuits. To derive insights into the device-to-device and load capacitance interaction we have simulated Ring Oscillator. Subsequently, we extend our circuit analysis to a Kogge Stone adder.

III. Parameter Analysis

We perform the analysis employing an in-house SPICE model for FEFETs [15] based on the time dependent LK equation for FE coupled with the predictive technology model (PTM) high performance 10 nm model for MOSFET [16]. The parameters and coefficients used for our analysis are given in Table. 1. The static coefficients of the LK equation (α, β and γ) have been extracted from our experiments.

Table 1. Simulation Parameters

Technology node	10nm FINFET
Number of fins in the transistor	3
α	-1.05e9 m/F
β	1e7 $m^5/F/coul^2$
γ	6e11 $m^9/F/coul^4$
ρ	0.1 Ω-m
Voltage Range	0.15V -0.5V

A. Steep Slope Operation of FEFETs

The possibility of ultra-low power operation comes from the steep slope characteristics of the device. We perform a simulation study of an n-type ferroelectric FinFET to explain the device operation and the dependence of I_{DS}–V_{GS} characteristics on the ferroelectric thickness. We call the device Ferroelectric FinFETs (FEFINFETs) because we have used the PTM FinFET model as the underlying transistor technology for our simulations. Fig. 3(a) shows the I_{DS}-V_{GS} plot of FEFINFET with the ferroelectric layer thickness = 3nm and 6nm in comparison with a regular FinFET with width of the device constrained to three fins (corresponding to a 7.5 track architecture [17]). For a standard CMOS device, drain current can be increased by increasing the width of the device, reducing the threshold voltage etc. For FEFET device we can tune the additional parameter- the ferroelectric layer thickness (T_{FE}) to obtain the desired drain current.

The boosted ON current at low voltages (steep slope mode of operation) is the result of the interaction between the negative capacitance of the FE layer and the positive capacitance of the underlying transistor. The FEFET can be considered as the series combination of these two capacitances. When the input voltage V_{GS} is applied, a negative voltage is developed across the ferroelectric layer capacitance. This implies that there is a positive voltage greater than applied input voltage $V_{GS,}$ which gets developed at gate of the underlying transistor (V_{MOS} in Fig. 2(a)). This voltage is shown as V_{INT} in Fig. 3(b). It can be observed that for both the FEFINFETs (T_{FE}=3nm and 6nm), the effective voltage of the underlying MOSFETs in the model is amplified due the negative FE layer capacitor.

Fig. 3 also shows that FEFETs exhibit a steeper slope with the increase in the ferroelectric layer thickness. This can be attributed to the $|C_{FE}|$ decrease with increase in T_{FE}. As a result, more negative voltage gets dropped across the ferroelectric layer, leading to a larger voltage boost at the intermediate node. As we increase the thickness of the ferroelectric layer beyond a certain point, the device begins to exhibit hysteresis. The hysteresis occurs at the V_{GS} for which the negative FE capacitance equals the positive gate capacitance of the underlying transistor. In order to stabilize the total system capacitance ($1/C_{TOT}=1/C_{FE}+1/C_{MOSFET}$) to be positive [7], the hysteretic jump occurs at a point which makes $|C_{FE}|$ to be higher than C_{MOS} for stability. However, for logic gates, we need to carefully choose T_{FE} in conjunction with other device parameters such that the operation is hysteresis free.

The gate capacitance of the FEFET is another important parameter to optimize the energy-delay characteristics of a circuit. We show the capacitance of the device with respect to the gate voltage applied in Fig. 4. We observe that as the thickness of the ferroelectric layer increases, the total gate capacitance increases. In this context, we analyze for a range of supply voltages (V_{DD}) whether the increase in ON current by the steep slope is large enough to compensate the effective increase in the input gate capacitance. In addition, the effect of the transients associated with polarization change are also considered, which are determined by the kinetic coefficient (ρ) in the L-K equation.

It is noteworthy that the ferroelectric FET needs to be optimized simultaneously, considering the thickness of the ferroelectric layer, the width of the FET, supply voltage and

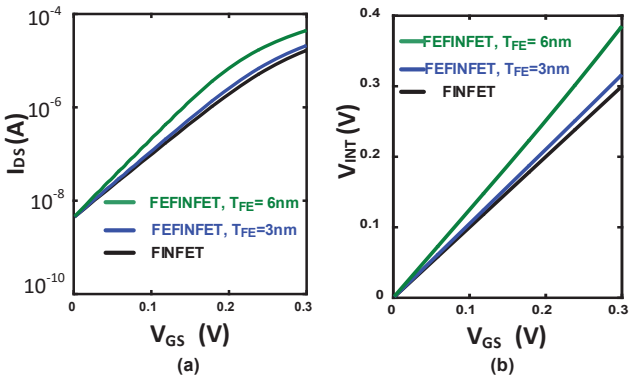

Figure 3. (a) I_{DS}-V_{GS} characteristics of the N-type FEFINFET with V_{DS}=0.3V, Number of fins=3; (b) Intermediate gate voltage Vs applied input gate voltage of the FEFINFETs with V_{DS}=0.3V, Number of fins=3;

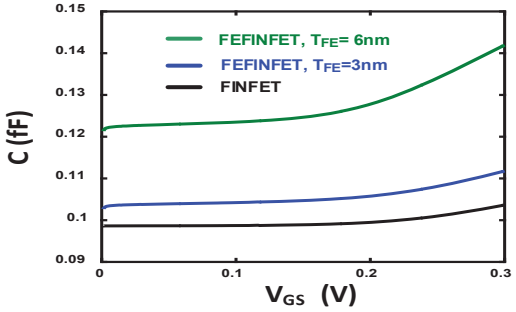

Figure 4. Gate capacitance of N-type FEFINFET and FinFET, V_{DS} =0.3V, Number of fins=3;

output load capacitance. In order to get the insight into the design trade-offs for FEFETs, we analyze the ring-oscillator in the next section.

B. Ring Oscillator Analysis

For analyzing the characteristics of the FEFET circuits, we simulate a ring oscillator and analyze the inverter characteristics under various conditions. The ring oscillator setup used for our simulations is shown in Fig. 5. Wire capacitance is equally important in determining the delay characteristics of the circuit. So we consider a range of wire capacitances in our analysis to understand its impact on FEFINFET based inverter. Also, we use a fanout of 4 (FO4 load) in the inverter chain.

Fig. 6 and Fig. 7 show the delay versus voltage and energy versus delay characteristics of the ring oscillator. From Fig. 6, we make three observations. First, at lower voltages, FEFINFETs have lower delay, which can be attributed to the comparatively higher sub-threshold slope of FEFINFETs. Second, we observe that FEFINFETs with higher thickness tends to show the lower delay at lower voltages and higher delay at higher voltages. This is mainly attributed to the transients associated with the polarization change. At high V_{DD}, the inherent delay of the transistor is lower than the time constant associated with polarization change and the latter serves as the limiting factor for the circuit delay. However, at low V_{DD}, the transistor resistance dominates and the effect of higher I_{ON} in FEFINFETs is evident in the delay decrease. Increase in T_{FE} increases the effect of the delay of polarization change on the circuit speed. Hence larger delay degradation is observed for higher T_{FE} at high V_{DD}. At the same time, the gain in I_{ON} is also larger for high T_{FE}, due to which larger delay improvements are observed at low V_{DD}. The third point to note is that with higher loads, the delay cross over point with FinFETs shifts towards higher V_{DD}. This is because the wire capacitance lowers the effect of the increased gate capacitance of FEFINFETs on the relative difference between the total load capacitance offered to FEFINFET inverters compared to the standard inverters.

Fig. 7 shows energy delay comparison of FEFINFETs. At low V_{DD}, FEFINFETs show superior characteristics, as we observed before. Note, the switching energy of FEFINFETs at a fixed V_{DD} is higher than standard FinFETs due to higher gate capacitance in the former. Despite that, we observe an energy reduction up to 15.38% at iso-delay for $V_{DD} < 0.17V$ for wire load (CW) of 1fF and ferroelectric layer thickness of 6nm. Higher circuit speed of FEFINFET at low voltages enables aggressive V_{DD} scaling leading to the operation of FEFINFET-circuits at a lower voltage compared to standard inverters, which saves power. At higher T_{FE}, larger reduction is observed in the energy dissipation at iso-delay due to steeper switching characteristics. Next, we analyze the energy and performance of FEFINFETs in comparison to FinFETs with a Kogge Stone adder as our test circuit.

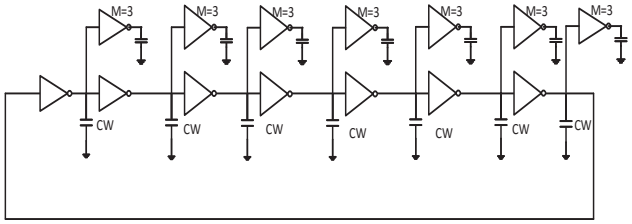

Figure 5. Seven Stage Ring Oscillator using FEFET, CW is the wire load parameter. Number of fins=3;

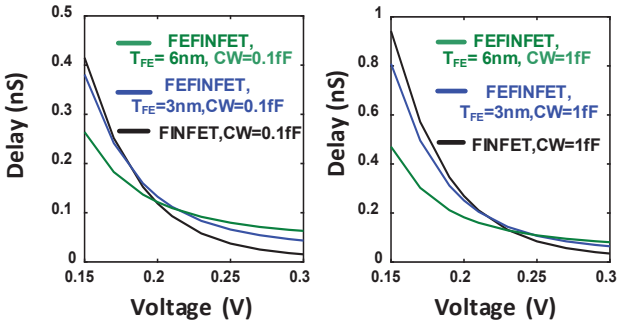

Figure 6. Delay Vs Voltage comparison of the Inverter using FINFET and FEFINFET, (CW is the wire load parameter) Number of fins=3;

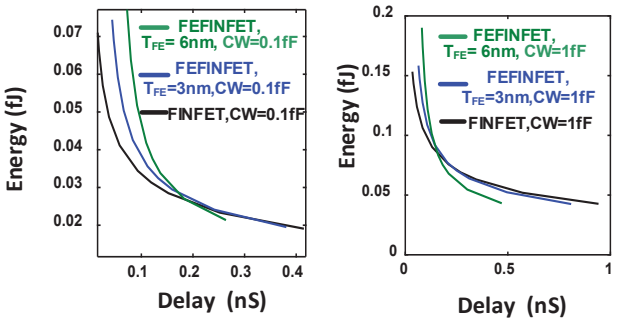

Figure 7. Energy Vs Delay comparison of Inverter using FINFET and FEFINFET, (CW is the wire load parameter) Number of fins=3;

C. Kogge Stone Adder

The Kogge Stone adder (KSA) belongs to the category of fast adders. The key benefits that make Kogge Stone adders widely used are its symmetric structure and balanced load in the internal nodes [18-19]. Addition becomes faster in Kogge Stone adders because they generate the 'carry' outputs in parallel rather than sequential rippling through the bit stages. Carry generation in KSA is done using Carry generation and propagation blocks.

The structure of an 8 bit KS adder from [18] is given in Fig. 8. It has 3 intermediate stages. In the stage 1, the propagation/carry bits of blocks containing 2 bits are computed in parallel. At stage two, carry propagation /generation bits from the previous stages are used to generate the carry for 4 bits. In the third stage, the carry for 8 bits is generated. The black box represents the carry

generation- propagation stages and grey box represent the carry generation stages.

We implemented the 8 bit KSA using FEFINFET gates. The gate level schematic of the implemented Kogge Stone is shown in Fig. 9 [20]. Kogge-Stone adder occupies a larger area compared to ripple carry adders. It is a wire intensive adder from a layout perspective. In addition, the number of individual FEFINFETS in the eight-bit adder is a few hundred. Hence, the analysis in this section presents insights into FEFINFET performance for a functional block much larger than the ring oscillator.

We assume a constant wire-load capacitance in the intermediate stages of the Kogge-Stone adder. We perform two sets of analysis keeping the intermediate wire-load of 0.001fF and 1fF. Note that, the critical path starts from input bit zero (A0/B0) to sum bit -S7 traverse through the three stages of the structure shown in Fig. 8.

D. Analysis and Results

Fig. 10 shows the output waveform of an 8 bit KSA simulation. For the delay calculation we choose a critical path from input bit A0 to carry bit C7 and values on input bits are chosen to propagate the carry until C7. For the performance analysis, we designed two flavors of FEFINFET gates with ferroelectric layer thickness 3nm and 6nm. The input slews to the adder inputs are taken from ring oscillator simulations.

Fig. 11 shows the voltage Vs delay characteristics of the FEFINFET and FinFET KS adders. The FEFINFET with larger FE thickness performs better at lower voltages. From Fig. 12, we see that the energy delay characteristics of the FEFINFET adder exhibits similar trends as that of the ring oscillator. At lower supply voltages the critical path exhibits lower delays with FEFINFET gates. Also we observe that gates with higher ferroelectric layer thickness shows lower critical path delay for the KS adder. We attribute this to the higher I_{ON} at lower voltages for FEFINFET as mentioned in section A and B. The energy delay characteristics of the KS adder also shows the expected trends where FEFINFET shows lower energy at higher delays. The higher delay regions correspond to lower operating voltages, where FEFINFET performs superior to FinFET. Our results show that at iso delay of 3.1 ns in the critical carry path, we get 9.21% energy reduction with ferroelectric layer thickness of 3nm gates and around 36% energy reduction with ferroelectric layer of thickness 6nm gates. Also, it should be noted that we have taken the above values from the simulation that incorporated wire loads=0.001fF. For higher wire-loads FEFINFETs will show larger benefits operating at near threshold voltages. For example, at the critical path iso delay of 3.1ns, we get 9.61% energy reduction with 3nm FE layer thickness gates and 38.46% energy reduction with 6nm FE layer thickness gates when the wire-load is fixed to be 1fF. We can also observe that the percentage improvement in the energy savings is higher for the KSA compared to ring oscillator with FEFINFET gates. This is attributed to the lower fanout in the KSA compared to consistent fanout of 4 in the ring oscillator. This in turn reduces the effective gate capacitance load seen in each stage reducing the delay. Note that, leakage power for FEFINFET and FinFET is the same due to equal OFF current (Fig. 3(a)).

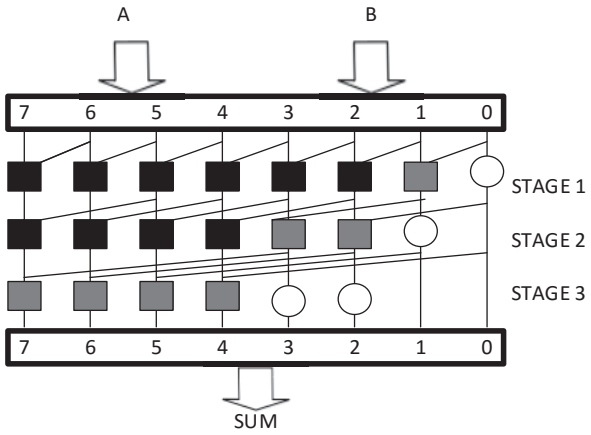

Figure 8. Schematic of an eight bit Kogge-Stone adder [18];

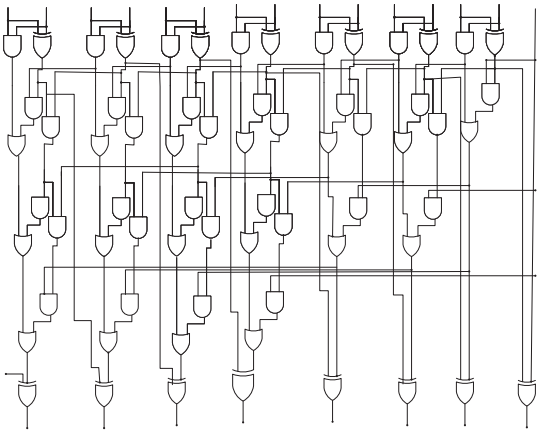

Figure 9. Gate level implementation diagram of an eight bit Kogge-Stone adder [20];

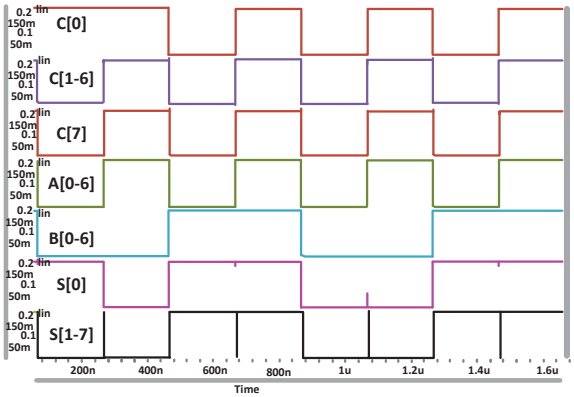

Figure 10. 8 bit KSA HSPICE waveform;

From the above simulation trends, we can conclude that FEFET based circuits are promising for low power digital logic processor, as they tend to perform better at low voltages compared to standard CMOS circuits. For low energy harvesting processors [1] [21-22], where higher circuit delays are not a major issue, FEFET logic is of significance.

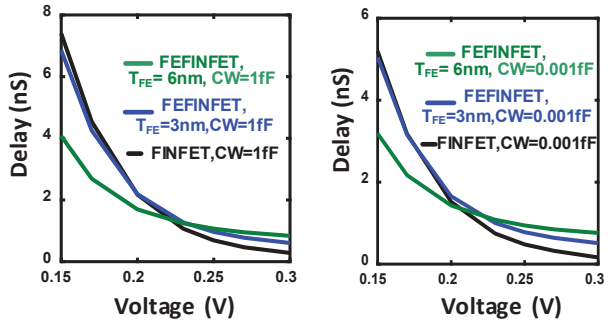

Figure 11. Carry Delay Vs Voltage diagram of the 8 bit KSA;

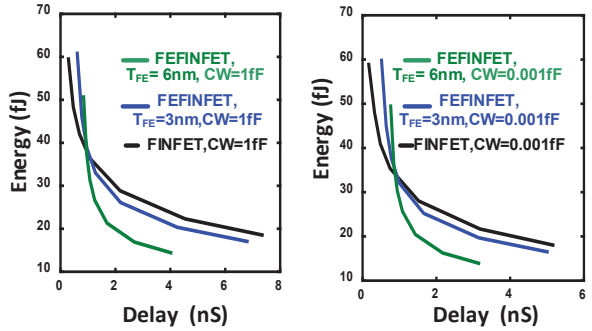

Figure 12. Energy Vs Carry Delay diagram of the 8 bit KSA;

IV. CONCLUSION

We performed the energy-delay comparison of ring oscillator and Kogge Stone adder based on FinFET and FEFET devices. Our analysis shows that FEFET based circuits consumes lower energy at iso delay for low supply voltages. For example, we get 9.21% energy reduction for ferroelectric thickness of 3nm and around 36% reduction for a ferroelectric thickness of 6nm at the iso carry path delay of 3.1 ns for an 8 bit Kogge Stone adder. From our analysis we infer that circuits built from FEFETs are more energy efficient at lower voltages compared to FinFET circuits.

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