

# Comparative Area and Parasitics Analysis in FinFET and Heterojunction Vertical TFET Standard Cells

MOON SEOK KIM, WILLIAM CANE-WISSING, XUEQING LI, and JACK SAMPSON,

The Pennsylvania State University

SUMAN DATTA, University of Notre Dame

SUMEET KUMAR GUPTA and VIJAYKRISHNAN NARAYANAN,

The Pennsylvania State University

Vertical tunnel field-effect transistors (VTFETs) have been extensively explored to overcome the scaling limits and to improve on-current ( $I_{ON}$ ) compared to standard lateral device structures for the future technologies. The benefits in terms of reduced footprint, high  $I_{ON}$  and feasibility of fabrication have been demonstrated in several works. Among various VTFETs, the asymmetric heterojunction vertical tunnel FETs (HVTFETs) have emerged as one of the promising alternatives to standard transistors for low-voltage applications. However, while such device-level benefits without parasitics have been widely investigated, logic-gate design with parasitics and layout implications are not clear. In this article, we investigate and compare the layouts and parasitic capacitances and resistances of HVTFETs with FinFETs. Due to the vertical device structure of HVTFETs, a smaller footprint is observed compared to FinFETs in cells with small fan-in. However, for high fan-in cells, HVTFETs exhibit area overheads due to infeasibility of contact sharing in parallel and series transistors. These area overheads also lead to approximately 48% higher parasitic capacitance and resistance compared to FinFETs when the number of parallel and series connections increases. Further, in order to analyze the impact of parasitics, we modeled the analytical parasitics in SPICE. The models for both HVTFETs and FinFETs with parasitics were used to simulate a 15-stage inverter-based ring oscillator (RO) in order to compare the delay and energy. Our simulation results clearly show that HVTFETs exhibit less delay at a  $V_{DD} < 0.45$  V and higher energy efficiency for  $V_{DDs}$  in the range of 0.3V–0.7V, albeit at the cost of 8% performance degradation.

CCS Concepts: • **Hardware** → **Emerging technologies; Modeling and parameter extraction**

Additional Key Words and Phrases: Standard cell, FinFET, tunnel FET, asymmetric vertical TFET, layout, area, parasitic capacitance, and parasitic resistance

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Authors' addresses: M. S. Kim, 351 Information Sciences and Technology Building, The Pennsylvania State University, University Park, PA 16802 USA; email: mqk5211@cse.psu.edu; W. Cane-Wissing, 121 Electrical Engineering East, The Pennsylvania State University, University Park, PA 16802 USA; email: wgc5032@psu.edu; X. Li, 351 Information Sciences and Technology Building, The Pennsylvania State University, University Park, PA 16802 USA; email: lixueq@cse.psu.edu; J. Sampson, 354E Information Sciences and Technology Building, The Pennsylvania State University, University Park, PA 16802 USA; email: sampson@cse.psu.edu; S. Datta, 271 Fitzpatrick Hall, University of Notre Dame, IN 46556 USA; email: sdatta@nd.edu; S. K. Gupta, 111K Electrical Engineering West, The Pennsylvania State University, University Park, PA 16802 USA; email: skg157@engr.psu.edu; V. Narayanan, 354D Information Sciences and Technology Building, The Pennsylvania State University, University Park, PA 16802 USA; email: vijay@cse.psu.edu.

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**1. INTRODUCTION**

The CMOS technology has been continuously scaling in the past few decades, leading to benefits of higher integration density, higher energy efficiency and superior performance. However, these benefits are accompanied by logic cell design challenges such as increased leakage power, fabrication yield, layout complexity and restrictions, increased susceptibility of circuits to process variations, and an increase in parasitic capacitances and resistances [Yu et al. 2002; Kuhn et al. 2010; Pacha et al. 2006; Cui et al. 2014; Xie et al. 2014]. In order to mitigate such issues, numerous alternative transistor architectures such as tunneling field-effect transistors (TFETs), nanowire, and vertical gate-all-around transistors are being widely investigated, among which asymmetric heterojunction vertical tunnel FETs (HVTFETs) show great promise [Seabaugh and Zhang 2010; Mohata et al. 2012; Liu et al. 2012; Datta et al. 2013]. HVTFETs have the advantages of (a) a reduced footprint due to the nature of the vertical structure, (b) ease of fabrication of heterojunctions, and (c) higher device performance at low voltages ( $<0.5V$ ). Meanwhile, TFET devices have been adopted in many emerging digital and analog circuit designs, such as data converters [Kim et al. 2014], power converters [Liu et al. 2014; Heo et al. 2015], and logic designs [Kim et al. 2014; Swaminathan et al. 2014], showing a great advantage in energy efficiency. However, these benefits are obtained without considering impacts of physical layout implementations, which affect not only parasitics but also device characteristics.

In addition, as described earlier, traditional scaling is accompanied by several issues, among which leakage power and fabrication process are currently well controlled with the help of device technologies (e.g., the gate last/replacement techniques, high- $\kappa$ /metal (HKMG) gate implementations, and so forth) in FinFETs [Yu et al. 2002; Kuhn et al. 2010, 2012; Natarajan et al. 2014]. However, a continuous increase in parasitic capacitances and resistances remains a challenge, as depicted in Figure 1 [Thompson et al. 2005]. In particular, parasitic capacitance becomes dominant since a large fin height ( $H_{FIN}$ ) and a small fin pitch ( $FP$ ) to obtain a higher electrical width in logic cells contribute to more parasitic capacitances [Wu and Chan 2007; Wei et al. 2009; Salas Rodriguez et al. 2013]. Hence, the analysis of parasitics is crucial for logic cells since their performance is determined by not only intrinsic device characteristics but also parasitic capacitances and resistances [Kuhn et al. 2012]. In HVTFETs, the parasitics have not been properly analyzed. Therefore, it is very important to explore advantages or trade-offs considering parasitics in HVTFETs compared to FinFETs.

In this article, we analyze two aspects: (a) layouts and (b) parasitic capacitance and resistance across logic cells based on HVTFETs and FinFETs. First, we quantify the area benefits and trade-offs by performing a detailed analysis of layouts for HVTFET cell designs in comparison with FinFETs. Since the fabrication process and integration of vertical devices are being continuously developed and refined, we use the key design rules based on Intel 22nm [Jan et al. 2012] and 14nm [Natarajan et al. 2014] for lateral FinFETs and the same metal pitches in Intel 22nm [Jan et al. 2012] and 14nm [Natarajan et al. 2014] for 20nm HVTFETs to characterize and compare FinFET- and HVTFET-based logic cell layouts. All the cell layouts are designed using the same cell-height architecture (7.5 metal track) to help with floor-planning flexibility and eventually area reduction. In the second part of this article, we analytically model the geometry-dependent parasitic capacitances and resistances based on each device

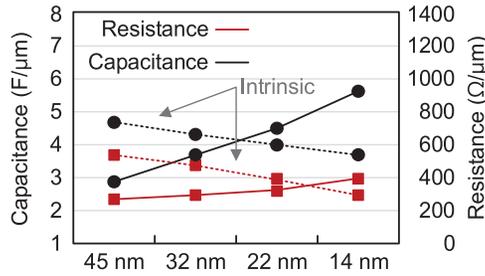


Fig. 1. Projections of parasitics [Thompson et al. 2005].

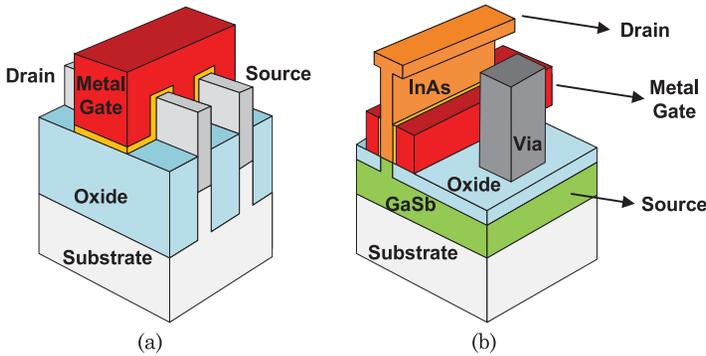


Fig. 2. Device structures: (a) FinFET and (b) asymmetric HVTFETs.

structure of the FinFET and HVTFET. In order to examine parasitics for logic cells, we systematically analyze the device structures and layouts. We implement the models for parasitics in Verilog-A [Liu et al. 2013, 2014] to explore and compare the impact of the parasitics in a 15-stage ring-oscillator (RO) [Yakimets et al. 2015a, 2015b].

This article is organized as follows. Section 2 introduces the differences in device structures between the FinFET and HVTFET. The layout analysis for both devices is described in Section 3. Section 4 discusses the modeling methodology for parasitic capacitance and resistance stemming from device structures and layouts for both FinFET and HVTFET considering parallel and series transistor connections. The ring-oscillator benchmarking across devices considering parasitics is included in Section 5. Section 6 presents our conclusions.

## 2. DEVICE STRUCTURES OF FINFET AND ASYMMETRIC HVTFET

Figure 2 shows the device structures of a FinFET [Jan et al. 2012; Natarajan et al. 2014] and an asymmetric HVTFET. FinFETs have been explored thoroughly in the past decade. A number of works have demonstrated improved short-channel behaviors of FinFETs over a conventional bulk metal–oxide–semiconductor field-effect transistor (MOSFET) [Choi et al. 2001]. With a thin-fin structure, the FinFET exhibits better electrostatic control of channel and electrical characteristics such as low leakage and higher on-current ( $I_{ON}$ ) due to reduced short-channel effects over conventional planar MOSFETs [Yu et al. 2002; Biddle et al. 2013]. Unlike the planar CMOS transistor, a FinFET has a nonplanar (three-dimensional) structure [Choi et al. 2001; Jan et al. 2012; He et al. 2010]. A FinFET is composed of fins that form a path for the current flow between the source and drain controlled by a gate voltage. The gate wraps around two lateral sides and top of the fins. Therefore, the effective electrical width of a single-fin

Table I. Process Parameters Across Estimated Technology Nodes

TECHNOLOGY	22nm	14nm	10nm	7nm	HTFET (22nm)	HTFET (14nm)
Contacted Gate Pitch (CGP) (nm)	90	70	64	48	*	*
Metal 1 Pitch (MP1) (nm)	80	64	48	36	80	64
Metal 0 Pitch (MP0) (nm)	*	56	42	32	*	56
Fin Pitch (FP) (nm)	60	42	36	27/24	*	*
Fin Height ( $H_{FIN}$ ) (nm)	34	42	*	*	*	*
Fin Thickness ( $T_{FIN}$ ) (nm)	10	8	*	*	7	7
Gate Length ( $L_g$ ) (nm)	26	20	*	*	20**	20**
Rbeol (Rb) ( $\Omega/\mu\text{m}$ )	*	*	60	135	*	*
Cbeol (Rc) ( $F/\mu\text{m}$ )	*	*	0.175	0.160	*	*
Supply Voltage (V)	0.75/0.8	0.7	0.7	0.65	<0.5	<0.5

Source: [Jan et al. 2012; Natarajan et al. 2014; Bardon et al. 2015; Liu et al. 2013].

\*Information is not available; \*\*Same  $L_g = 20\text{nm}$  HTFETs are used since HTFET is the vertical device.

Table II. Abbreviations

CGP	MP	FP	$T_{FIN}$	$H_{FIN}$	CW	CH	$W_E$	$W_{EMAX}$
Contacted Gate Pitch	Metal Pitch	Fin Pitch	Thickness of Fin	Height of Fin	Cell Width	Cell Height	Electrical Width	Maximum Electrical Width

is given by  $2H_{FIN}+T_{FIN}$  (where  $H_{FIN}$  is the fin height and  $T_{FIN}$  is the fin thickness). The width of a FinFET is thus quantized in steps of  $2H_{FIN}+T_{FIN}$  [Yu et al. 2002; Xie et al. 2014].

Recently, vertically fabricated TFETs have been widely investigated and explored to further overcome scaling issues and to improve the subthreshold slope (SS). In this device, the current flow in the channel is perpendicular to the wafer (unlike the lateral current flow in FinFETs). Further, the gate and channel length are independent of lithographic patterning methods. Figure 2(b) illustrates the three-dimensional (3-D) device structure of the HVTFET. Two gates are formed on each side of the channel between vertically aligned source and drain regions, and the gate metal is extended to form gate contacts. The source and drain contacts are formed on the top or bottom active regions. Since the HVTFET is a double gate (DG) structure, its effective electrical width is  $2 \times W_E$ , where  $W_E$  is the width of the active region.

HVTFETs are essentially a gated p-i-n tunnel diode with asymmetric GaSb-InAs (III-V) source/drain (S/D) doping [Liu et al. 2013]. The ON and OFF switching is driven by the gate-voltage-induced band-to-band tunneling (BTBT) at the source-channel junction [Saripalli et al. 2011; Mohata et al. 2012; Liu et al. 2013]. The asymmetric features result in current flow in one direction, also known as “unidirectional conduction behavior.” This is in contrast to FinFETs, which exhibit symmetric bidirectional current. This difference has important implications for layout designs in logic cells, as we will discuss later.

### 3. LAYOUT ANALYSIS OF FINFETS AND HVTFETS

In a standard cell design, the layout and area of cells are strongly dependent on the device structure and fabrication process. In this section, we perform a detailed layout analysis of FinFETs and HVTFETs in logic cell designs to examine their benefits and trade-offs.

Table I summarizes key device dimensions and design rules for the 22nm to 7nm FinFETs and 20nm gate-length ( $L_g = 20\text{nm}$ ) HVTFET. Table II expands the abbreviations used in this Table I and throughout the remainder of the manuscript. At current advanced technologies, the  $L_g$  is no longer an indication of the exact technology node dimension. As shown in Table I, for example, the  $L_g$  in 14nm FinFET is not exactly 14nm and can range from 14nm [Natarajan et al. 2014] to 20nm [Jan et al. 2012]. This

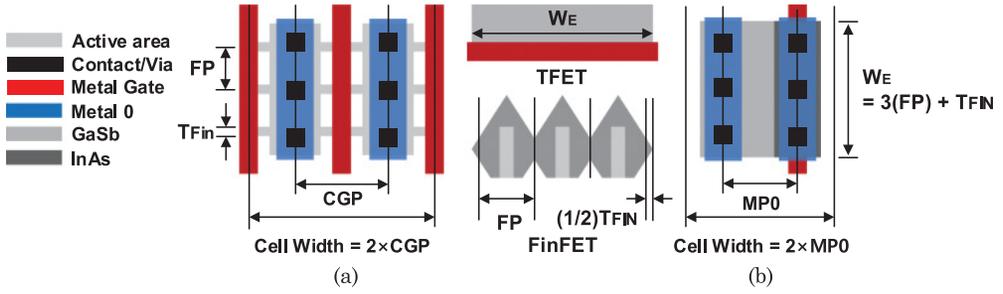


Fig. 3. Device dimensions: (a) FinFET (b) HVTFT.

trend is expected to continue for projected sub-10nm FinFET technologies [Yakimets et al. 2015b]. For vertically fabricated devices, it is even more difficult to define a technology node since the fabrication process of these devices is mainly limited by the contact placement and metal 0 pitch (MP0) rather than the contacted gate pitch (CGP) in FinFETs due to the vertical device architectures. Hence, in this article, we compare the HVTFT layout based on the process parameters (FP and MP0) of 22nm and 14nm FinFETs. To analyze implications and differences between the standard cell library based on FinFETs and the one based on HVTFTs, we consider several combinational and sequential logic gates.

For logic cell designs, the cell height (CH) is a critical design consideration and is dependent on the design requirements with regard to the optimization of density, power, and performance. For subsequent analysis, a 7.5-track (7.5 T) architecture is chosen to achieve low power, for which cell architectures with smaller height are more suitable [Hou et al. 2013].

Figure 3 presents the device dimensions used in this analysis. The baseline one-transistor layout has at most three fins (3F) because a 7.5 T architecture corresponds to 3F in the NMOS/PMOS, as we will discuss later.

### 3.1. Electrical Width Quantization

A key parameter of a cell design in a standard cell library is the maximum electrical width ( $W_{EMAX}$ ) of n- and p-devices that can fit in a given cell height (7.5 T in this article) because the electrical width ( $W_E$ ) determines a drive strength of logic gates for a fixed area or layout area of the logic gates for a fixed drive strength in a single-finger layout.

The cell-height (CH) is mainly determined by MP2 and FP [Alioto et al. 2011]. For the 7.5 T architecture, the CH equals  $7.5 \times MP2$ . For instance, with an assumption that  $MP2 = MP1$ ,  $64\text{nm} (MP1) \times 7.5$  is equal to 480nm in a 14nm technology. For FinFETs, 10 fins can be formed in a given 7.5 T as is evident from the ratio ( $4/3 \sim 3/2$ ) between the MP2 (and MP1) and FP (Table I) in a sub-20nm node.

Out of the 10 fins in the 7.5 T architecture, the total number of active fins is 6, out of which three fins form the n-type transistor, while the other three form the p-type transistor. Appropriate space is formed between n- and p-FinFETs for gate contact placement and for internal routing in a cell by etching two fins. Two more fins (one each on the top and bottom cell boundary) are removed to enable proper cell abutment and the placement of power rails of cells. Note that the p- and n-type FinFETs have equal strength due to the hole mobility improvement obtained from the adoption of SiGe for the p-type transistor [Yu et al. 2002; Jan et al. 2012; Natarajan et al. 2014; Xie et al. 2014; Biddle et al. 2013]. From this discussion,  $W_{EMAX}$  for FinFET cells in a 7.5 T architecture is obtained as [Anil et al. 2003]:

$$W_{EMAX,FinFET} = N_{FIN} \times (2H_{FIN} + T_{FIN}). \quad (1)$$

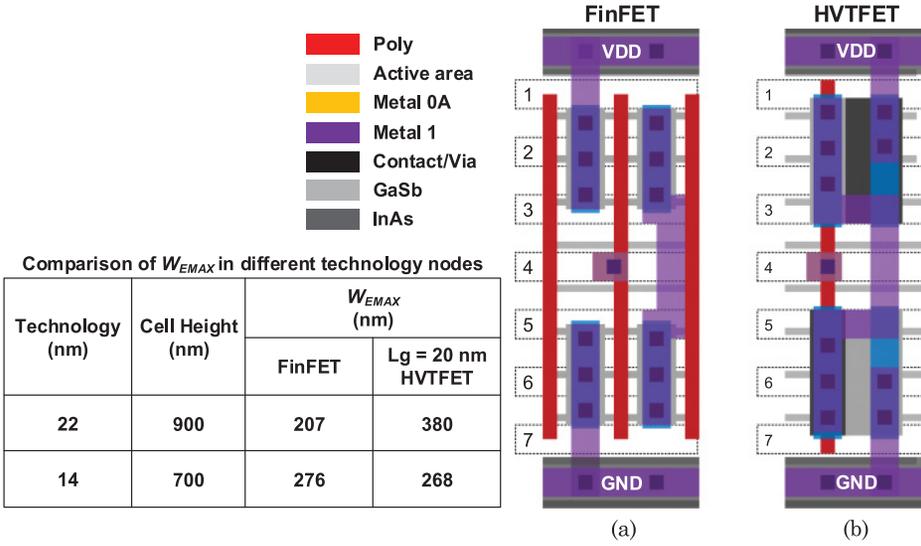


Fig. 4. The single-finger inverter layouts with the maximum electrical width ( $W_{EMAX}$ ) with respect to the technology nodes in (a) FinFET and (b) HVTFET.

where  $N_{FIN}$  is the number of fins for either n- or p-type FETs. From Equation (1) and Table I, and using  $N_{FIN} = 3$ ,  $W_{EMAX} = 276\text{nm}$  is obtained for the 14nm technology node for n- and p-type FinFET, each considering a single-finger inverter (INVX1) in a given 7.5 T cell height.

For HTVFETs, as introduced in Section 2, the  $W_{EMAX}$  can be expressed as

$$W_{EMAX, HVTFET} = 2 \times (W_E) = 2 \times (3FP + T_{FIN}). \quad (2)$$

Based on a given CH, the maximum width of the active region (or the sum of the width of n- and p- devices) is obtained as  $W_{EMAX} = 268\text{nm}$  for 14nm and  $226\text{nm}$  for 10nm technology nodes because of the double-gate structure as shown in Figure 3 and Equation (2) with an assumption of thickness of epitaxy ( $Epi$ ) =  $FP + T_{FIN}$ . In comparison to FinFETs, HVTFETs have  $\sim 1.8\times$  larger  $W_{EMAX}$  in a 7.5 T architecture in  $>20\text{nm}$  technologies but the  $W_{EMAX}$  of FinFETs is slightly higher or similar for  $<20\text{nm}$  technologies, as shown in Figure 4. This translates to  $\sim 2\times$  larger cell area in FinFETs in near-20nm technology if the two devices are designed to have the same  $W_{EMAX}$ . However, in sub-20nm,  $W_{EMAX}$  is very similar in both devices and so is the cell size at iso- $W_{EMAX}$ . In addition, HVTFETs provide higher  $I_{ON}$  density than that of FinFETs at low voltages due to their steep-slope characteristics [Seabaugh and Zhang 2010; Saripalli et al. 2011; Mohata et al. 2012; Liu et al. 2013]. Therefore, HVTFETs can provide an additional increase in the drive-ability ( $I_{DS}$ ) compared to FinFET logic cells in low-voltage ranges ( $<0.5\text{ V}$ ).

### 3.2. A Single-Finger Cell Width Comparison

The cell width (CW) of a single-finger device can be calculated using the process parameters in Table I. The CW of a device has linear dependence on CGP or MP0. For FinFETs, the CW is easily expressed by using the CGP. However, for HVTFETs, the CW is a function of MP0 rather than CGP since layouts of vertical devices are mainly restricted by MP0 due to contact placements, as shown in Figure 3. For instance, the width of a single transistor can be described as two CGP ( $2 \times CGP$ ) for FinFETs and two MP0 ( $2 \times MP0$ ) for HTFETs. With the process parameters for the 14nm and 10nm

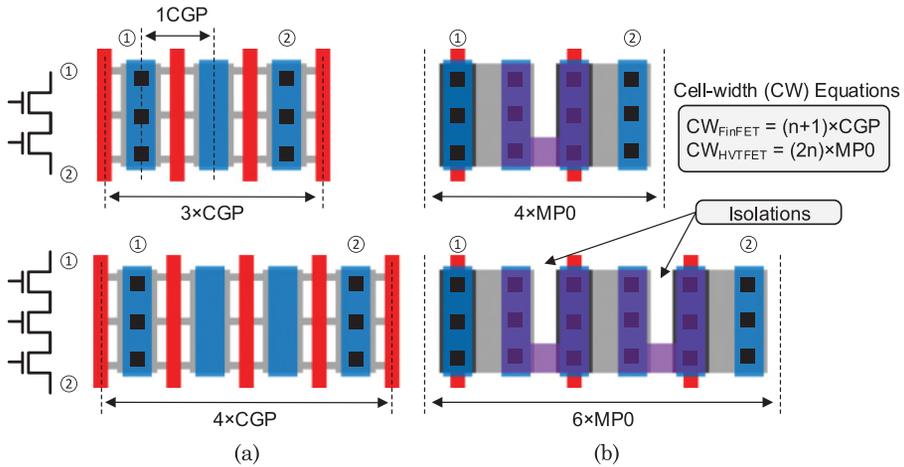


Fig. 5. Layout top-sectional views of series two and three transistors: (a) FinFETs and (b) HVTFETs.

technology nodes, the CWs for FinFETs are obtained to be 140nm and 128nm, while the widths of HVTFETs are 112nm and 84nm, respectively. The comparison results show that the 14nm and 10nm HVTFETs exhibit  $0.8\times$  and  $0.7\times$  less one-transistor footprint area than the corresponding FinFETs, respectively. Thus, the CW ratio between FinFETs and HVTFETs can be interpreted as the ratio between CGP and MP0. As mentioned earlier, it becomes a challenge to further shrink CGP compared to MP at deeply scaled sub-10nm nodes [Yakimets et al. 2015a, 2015b; Bardon et al. 2015]. Hence, the ratio of CW between FinFETs and HVTFETs, or vertically fabricated devices (e.g., vertical nanowire FETs), is expected to be significantly larger.

### 3.3. A Single-Finger Inverter (INVX1)

Figure 4 shows the layout of a single-finger inverter. The layout exhibits differences not only in  $W_{EMAX}$  but also in the CW or horizontal dimension of the cell. As described earlier, for a FinFET inverter, the CW is determined by the CGP. However, in an HVTFET inverter, the gate metal/poly deposition is performed around the vertical pillar that forms the source/channel/drain and does not require conventional lithography and patterning. Therefore, unlike FinFETs, the horizontal dimension of an HVTFET inverter is determined by the MP0 [Kim et al. 2015]. Since the CW of single-finger inverters based on FinFETs and HVTFETs are  $2\text{CGP}$  and  $2\text{MP0}$ , respectively, and typically  $\text{MP0} < \text{CGP}$  (Table I), the layout area for HVTFETs is lower compared to FinFETs. The cell area ( $\text{CH} \times \text{CW}$ ) of an INVX1 is obtained as  $0.07\mu\text{m}^2$  and  $0.05\mu\text{m}^2$  for the FinFET and HVTFET inverters, respectively. For more complex cells with a larger drive or higher fan-in, the CW is a multiple of CGP for FinFETs and MP0 for HVTFETs, as we will discuss later.

### 3.4. Series and Parallel Connections

In logic cell designs, a number of transistors are connected either in series or in parallel (a) to implement complex Boolean functions, for instance, NAND and NOR; and (b) to construct multiple fingers in order to increase the drive strength in logic cells such as INVX2, INVX4, and so forth. In this section, we describe the layout differences between FinFETs and HVTFETs.

**3.4.1. Series Connection.** Figure 5 shows two and three transistors stacked in series. The geometric layout in series connections of FinFETs is similar to the planar CMOS.

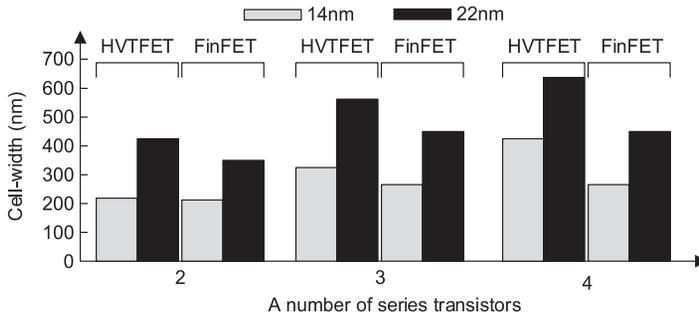


Fig. 6. CW comparison with regard to the number of series transistors in FinFETs and HVTFET.

One diffusion region is shared between stacked transistors. Unlike stacked FinFETs, HVTFETs necessarily require shallow trench isolation (STI) [Saripalli et al. 2011; Mohata et al. 2012; Liu et al. 2013] to isolate two diffusion regions of the adjacent transistors in order to connect the transistors in a series. This is because of the vertical nature of HVTFETs and unidirectional conduction behavior [Liu et al. 2013], as discussed before. Hence, the area benefit observed in a single vertical device is no longer viable because it needs  $(2 \times n) \times MP0$  for the CW while FinFETs need  $(n + 1) \times CGP$ , where  $n$  is the number of series connections. For the parameters of the 14nm technology node, the CW of each device is equal to 224nm ( $= 4 \times 56$ nm) for HVTFET and 210nm ( $= 3 \times 70$ nm) for FinFETs, respectively, when two transistors are stacked. Figure 6 depicts the CW comparison between FinFETs and HVTFETs versus the number of series connections. In two stacked transistors, the HVTFET exhibits almost the same layout footprint compared to FinFETs. However, the CW of HVTFET becomes wider than the CW of FinFETs due to the penalty of isolations originating from unidirectional conduction when the number of series connections exceeds two [Kim et al. 2015]. It is also noted that, if the vertical FET is not asymmetric (i.e., not unidirectional conduction), which means that the current flows bidirectionally, the expression of CW for HVTFETs can be modified as  $(2 \times n - 1) \times MP0$ . It helps to further reduce the layout footprint by 20 ~ 30% compared to both FinFETs and HVTFETs.

**3.4.2. Parallel Connection.** The layouts of transistors connected in parallel are illustrated in Figure 7 for both FinFETs and HVTFETs. For FinFETs, the active/diffusion regions are shared between adjacent transistors, resulting in fewer diffusion breaks and a smaller area [Wang and Gupta 2014]. As an example,  $(n - 1)$  active regions would be shared by adjacent transistors if  $n$  transistors are connected in parallel.

For HVTFETs in parallel, the bottom diffusion region can be shared. The shared bottom source is connected through the via contact between two top diffusion regions with retaining the constant  $MP0$ . Wang and Gupta [2014] introduce the compact layout strategy for vertical FETs, which removes the contacts between top drains. However, we keep the shared source with contacts while maintaining the  $MP0$  between two top drains to avoid large parasitic source resistance.

An example of three transistors connected in parallel for FinFETs and HVTFETs is shown in Figure 7. For FinFETs, the CW is equal to  $(n + 1) \times CGP$  when  $n$  transistors are connected in parallel. The CW of  $n$  parallel chains in HVTFETs is  $(2 \times n - 1) \times MP0$ . Figure 8 also shows the CW versus the number of parallel chains. As expected, two parallel transistor chains in HVTFETs have less width compared to FinFETs. However, the CW of HVTFETs exceeds that of FinFETs as the number of parallel transistors exceeds three. It is evident that the area of HVTFET-based cells will be larger than FinFET-based cells when either the drive strength or the number of inputs increases.

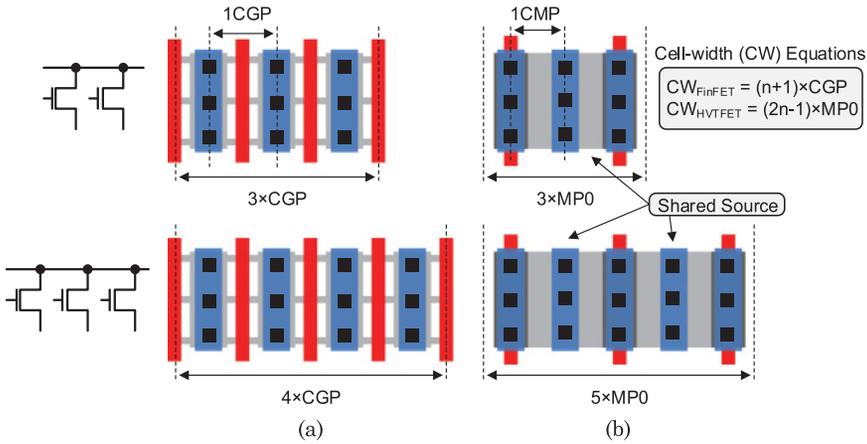


Fig. 7. Layout top-sectional views of parallel two and three transistors: (a) FinFETs and (b) HVTFETs.

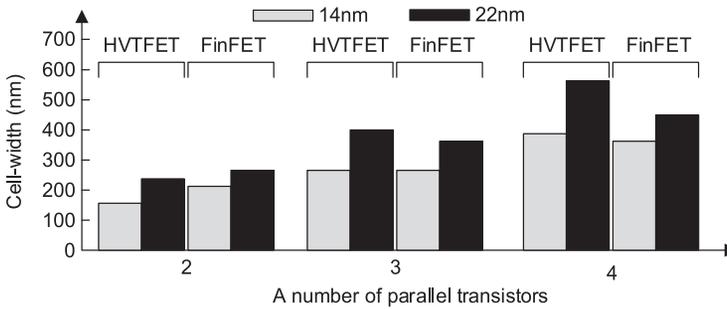


Fig. 8. CW comparison with regards to the number of parallel transistors in FinFETs and HVTFET.

Figure 6 and 8 show CW differences with respect to the number of parallel and series transistors. The CW of HVTFETs exceeds the CW of FinFETs as the number of connections increases due to (a) the isolation penalty for series connections and (b) contact placement for sharing sources (or drains) for parallel transistors. In particular, the series transistor connection has an additional isolation penalty, as discussed earlier; therefore, HVTFETs exhibit a larger area compared to FinFETs when the number of series connections exceeds two in >20nm technology nodes and three in the 14nm technology node, respectively.

### 3.5. Area Analysis of Logic Cells in FinFETs and HVTFETs

Considering parallel and series transistor connections, the layout analysis in logic cells for the standard cell library shows an area overhead in HVTFET-based cells. Table III compares the cell width of HVTFET- and FinFET-based INV, NAND, and-or-inverter (AOI) and D flip-flop (DFF) logic gates for different drive strength and different technology nodes. Above 20nm technologies, most cells (e.g., X1) based on FinFETs have area benefit compared to cells based on HVTFETs due to the isolation penalty stemming from the asymmetric device characteristic in HVTFETs. In addition, like parallel and series transistors, the areas for HVTFETs become even worse as the number of inputs and drive strength increase. However, the area benefits in HVTFETs are evident from Table III for sub-20nm technology nodes. The reason is that the ratio

Table III. Cell-Width (CW) Changes in Comparison With FinFET-Based Cells

Devices	INV			NAND		AOI21	AOI22	DFF	
	X1	X2	X4	X1	X2	X1	X1	with Reset	without Reset
10nm FinFET	128nm	192nm	320nm	192nm	384nm	320nm	384nm	1.41 $\mu$ m	1.54 $\mu$ m
HVTFET	84nm	168nm	294nm	168nm	294nm	210nm	336nm	1.09 $\mu$ m	1.26 $\mu$ m
CW	-34%	-13%	-8.1%	-13%	-23%	-34%	-13%	-23%	-18%
14nm FinFET	140nm	210nm	350nm	210nm	420nm	350nm	420nm	1.54 $\mu$ m	1.68 $\mu$ m
HVTFET	112nm	168nm	392nm	224nm	392nm	280nm	448nm	1.46 $\mu$ m	1.68 $\mu$ m
CW	-20%	-20%	+11%	+6.3%	-6.7%	-20%	+6.3%	-5.1%	0.0%
22nm FinFET	180nm	270nm	540nm	270nm	540nm	450nm	540nm	1.98 $\mu$ m	2.16 $\mu$ m
HVTFET	160nm	320nm	640nm	320nm	560nm	400nm	640nm	2.08 $\mu$ m	2.40 $\mu$ m
CW	-11%	+15%	+15%	+16%	+4.0%	-11%	+15%	+4.8%	+10%

\*Positive: area increases; Negative: area decreases.

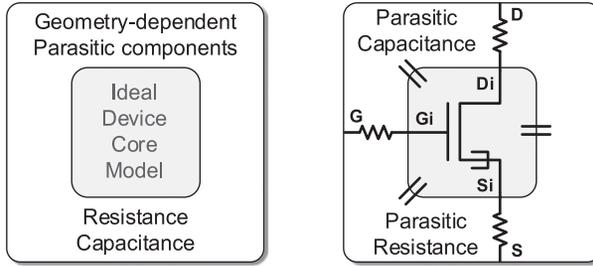


Fig. 9. Modeling of geometry-dependent parasitic components with ideal core model.

between  $MP_0$  and  $CGP$  decreases (e.g.,  $MP_0/CGP = 0.9$  for 22nm, 0.8 for 14nm, and 0.7 for 10nm). It leads to reduction of the CW in HVTFET-based cells.

#### 4. EXTRACTIONS OF PARASITICS IN FINFETs AND HVTFETs

As technology is continuously scaling, the fabrication process is becoming dense and more complicated. Consequently, the parasitic resistive and capacitive components become comparable to, and even larger than, the intrinsic resistive and capacitive components [Pacha et al. 2006]. This parasitic resistance results in a significant degradation of current drive capability, leading to the severe degradation of performance in logic cells. The parasitic capacitances may dominate the intrinsic device characteristics in analog/RF systems [Pacha et al. 2006; Wu and Chan 2007]. Also, in the digital domain, these parasitics lead to the degradations of speed and power efficiency due to increased capacitance and reduced  $I_{ON}$  [Wu and Chan 2007; Wei et al. 2009]. Hence, in order to perform accurate power and timing analysis through the synthesis flow in logic cells, it is crucial to capture parasitic resistance and capacitance originating from geometry-dependent device structure.

In the following section, we describe the analytically estimated parasitics appended to an ideal device core model [Liu et al. 2013], as illustrated in Figure 9. Note that the parasitics until the metal 0 trench contact (M0A) are evaluated and the parasitics of upper-trench contacts are ignored since this article focuses on parasitics originating from the differences among device structures rather than interconnect parasitics.

##### 4.1. Basic Capacitive Component Modeling

The parasitic capacitances in FinFETs have already been analyzed in a number of articles [Wu and Chan 2007; Salas Rodriguez et al. 2013; Bhoj et al. 2013]. A multigate FinFET structure entails significant attention to the newly formed parasitic

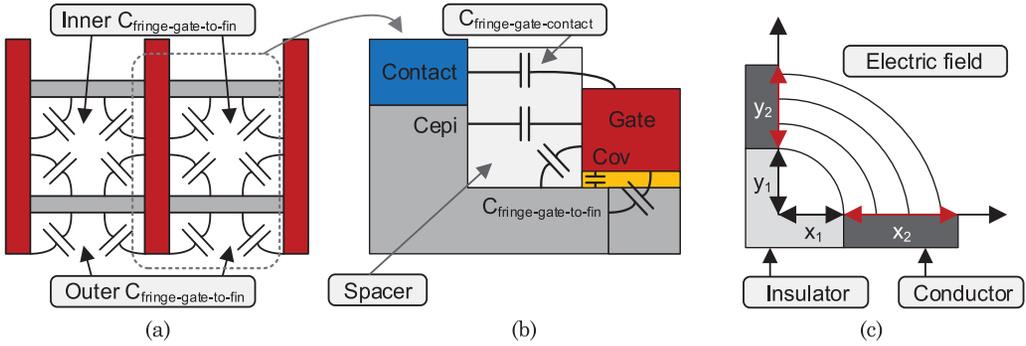


Fig. 10. (a) and (b) New parasitic capacitances by a nature of geometry in FinFETs and (c) coordinate parameter descriptions for fringing capacitance ( $C_{fri}$ ).

capacitances (i.e., fringing capacitance by sidewalls of fins) associated with 3-D fins, multigates, dummy gates, and trench contacts [Bhoj et al. 2013] as presented in Figures 10(a) and 10(b).

Like the advent of new parasitic capacitances in FinFETs, HVTFTs also introduce new parasitic capacitances, stemming from the asymmetric doping (III-V doping profiles) [Liu et al. 2013; Kim et al. 2014] and vertically fabricated structure. In the following section, we analytically examine the parasitic capacitances based on the following primary components: (1) the inner and outer fringing capacitance ( $C_{fri}$ ) arising from the gate electrodes; (2) the parallel-plate capacitances ( $C_{pp}$ ) including drain/source (S/D) extensions; and (3) overlap capacitance ( $C_{ov}$ ).

**4.1.1. Fringing Capacitance ( $C_{fri}$ ).** The fringing capacitances correspond to the capacitive components associated with the electric field coupling between the adjacent electrodes, which are not parallel and separated by an insulator [Lacord et al. 2012; Salas Rodriguez et al. 2013]. The fringing capacitance due to the nature of the perpendicular structure of the FinFET and HVTFT could be calculated by Equations (3), (4), and (5) in Lacord et al. [2012]:

$$C_{fri} = C_1(\text{if } x_1 \neq x_2) + C_2(\text{if } x < x_1, y < y_1) \quad (3)$$

$$C_1 = \frac{2 \cdot \epsilon_{rel-p} \cdot \epsilon_{free} \cdot W}{\pi} \left[ \begin{array}{l} \sinh^{-1} \left( \sqrt{\frac{x_1^2 + \min(y_2, x_2)^2 + 2y_1 \min(y_2, x_2)}{\sqrt{|x_1^2 - y_1^2|}}} \right) \\ - \sinh^{-1} \left( \sqrt{\frac{x_1}{\sqrt{|x_1^2 - y_1^2|}}} \right) \end{array} \right], \quad x \neq x_1 \quad (4)$$

$$C_2 = 0.35 \frac{\epsilon_{rel-p} \cdot \epsilon_{free} \cdot W}{2\pi} \ln \left( \frac{\pi W}{\sqrt{|x_1^2 - y_1^2|}} \right), \quad x < x_1 \text{ and } y < y_1 \quad (5)$$

where  $\epsilon_{rel-p}$  is the relative permittivity of dielectric,  $\epsilon_{free}$  is the permittivity in free space,  $W$  is the device width, 0.35 is a fitting parameter, and  $x_1$ ,  $x_2$ ,  $y_1$ , and  $y_2$  are the geometric coordinate parameters illustrated in Figure 10(c) [Lacord et al. 2012].

In FinFETs, the fringing capacitances can be categorized into the inner fringing and outer fringing capacitance accounting for the coupling between multifins and gate electrodes. Figures 10(a) and 10(b) depict the fringing capacitances in FinFETs. Among fringing capacitances, the gate electrode to fin-sidewall fringing capacitances ( $C_{g,fri}$ )



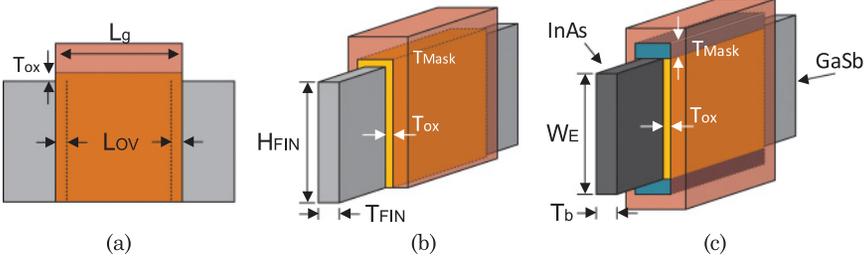


Fig. 12. (a) Geometry parameters for overlap capacitance (a)  $L_{ov}$ , (b) FinFET, and (c) HVTFTs.

$\theta$  (Figure 11(c)). Here, we assume that  $\theta$  is the same for angles of the gate and via.

$$C_{gs,via}(\theta) = N_{via} \cdot W_{via} \cdot \sin \theta \cdot (L_g + 2 \cdot L_{ov}) \cdot \frac{\epsilon_{ILD} \cdot \epsilon_{free}}{MPO - \left( \frac{1}{2} T_b + T_{ox} + T_{gate} + \frac{W_{via} - H_{via}}{2} \tan \theta \right)} \quad (8)$$

If  $\theta$  is  $80^\circ$  and employing the device parameters (e.g.,  $T_{ox} = 2\text{nm}$ ,  $T_b = 7\text{nm}$ ,  $T_{gate} = 5\text{nm}$ ,  $W_{via} = 15\text{nm}$ , and  $H_{via} = 105\text{nm}$ ) of HVTFTs [Liu et al. 2014] and process parameters of the 14nm node,  $C_{gs,via}$  in HVTFTs is equal to 0.34 aF/via. This parasitic capacitance originating from the additional vias increases as the feature dimensions reduce in accordance with technology scaling. Other capacitance components such as the  $W_E$ -dependent  $C_{pp}$ ,  $C_{fri}$ , and  $C_{ov}$  decrease due to reduction of  $W_E$  at a fixed CH (i.e., from  $W_E = 380\text{nm}$  at the 22nm node to  $W_E = 268\text{nm}$  at the 14nm node (Figure 4)).

**4.1.3. Overlap Capacitance.** The overlap capacitance ( $C_{ov}$ ) originates from the overlap between S/D regions and the gate, as shown in Figure 12(a).  $C_{ov}$  includes the gate-source lateral extension overlap capacitance along the sidewall  $C_{gs1,ov}$ , and  $C_{gs2,ov}$  and the gate-drain overlap capacitance  $C_{gd1,ov}$  and  $C_{gd2,ov}$  [Liu et al. 2013].  $L_{ov}$  of 1nm is employed from the edge of the gate electrode to the S/D region [Liu et al. 2013] for each device. Since the traditional calculation based on parallel-plate capacitor concept is not appropriate to FinFETs due to the finite thickness of the gate and S/D region [Wu and Chan 2007], the expression for  $C_{ov}$  is derived by considering a tri-gate structure and using equations in Wu and Chan [2007]:

$$C_{ov} = N_{FIN} \cdot (2T_{FIN} + 4H_{FIN}) \cdot c_{ov}(T_{ox}), \quad (9)$$

where  $c_{ov}(u) = \frac{\Delta(u) + L_{ov}}{u} \epsilon_{ox} + \frac{2\epsilon_{Si}}{\pi} \ln[1 + \frac{x_j}{u} \sin(k)]$ ,  $k = \frac{\pi}{2} \cdot \frac{\epsilon_{ox}}{\epsilon_{Si}}$ ,  $\Delta(u) = \frac{u}{2} [1 + \frac{1 - \cos(k)}{\sin(k)}]$ , and  $x_j$  is the junction depth and assumed to  $T_{FIN}/2$  for  $2T_{FIN}$  term and  $H_{FIN}/2$  for  $4H_{FIN}$  term [Wu and Chan 2007]. The  $\epsilon_{ox}$  and  $\epsilon_{Si}$  denote the dielectric constant for the gate oxide and silicon, respectively. For HVTFTs, there are two components of  $C_{ov}$  originating from the asymmetric structure and different doping profiles (e.g., GaSb and InAs) of S/D regions, unlike FinFETs. The  $C_{ov}$  can be modified by using Equation (9) considering the ultra-thin-body (UTB) vertical structure of HVTFTs:

$$C_{ov} = \left[ \begin{array}{l} 2T_b \cdot c_{ov}(T_{Mask}, W_{EMAX}/4) \\ + W_{EMAX} \cdot c_{ov}(T_{ox}, T_b/2) \end{array} \right]_{InAs} + \left[ \begin{array}{l} 2T_b \cdot c_{ov}(T_{Mask}, W_{EMAX}/4) \\ + W_{EMAX} \cdot c_{ov}(T_{ox}, T_b/2) \end{array} \right]_{GaSb}, \quad (10)$$

where  $c_{ov}(u, v) = \frac{\Delta(u) + L_{ov}}{u} \epsilon_{ox} + \frac{2\{\epsilon_{GaSb}, \epsilon_{InAs}\}}{\pi} \ln[1 + \frac{v}{u} \sin\{k_{GaSb}, k_{InAs}\}]$ ,  $k = \frac{\pi}{2} \cdot \frac{\epsilon_{ox}}{\{\epsilon_{GaSb}, \epsilon_{InAs}\}}$ ,  $\Delta(u) = \frac{u}{2} [1 + \frac{1 - \cos\{k_{GaSb}, k_{InAs}\}}{\sin\{k_{GaSb}, k_{InAs}\}}]$ . The  $\epsilon_{GaSb} = 15.7$  and  $\epsilon_{InAs} = 15.1$  indicate each dielectric constant for the GaSb and InAs in HVTFTs [Liu et al. 2013], respectively.

Applying device parameters in Liu et al [2013] and  $W_{EMAX}$  in Figure 4 reveals that  $C_{ov}$  in HVTFTs is 28.0% larger than FinFETs in 22nm node (e.g., 40.2 aF for FinFETs and 51.5 aF for HVTFTs). However, in 14nm node,  $C_{ov}$  in HVTFTs become less than

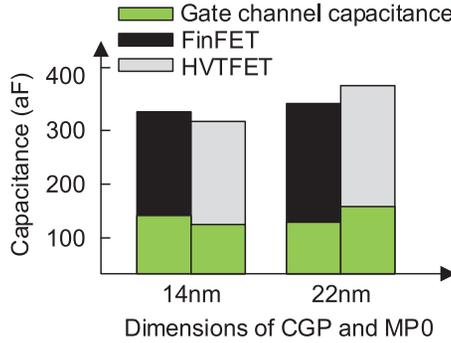


Fig. 13. The overall capacitance breakdown in different technology nodes: different device width at a given cell height (Figure 4).

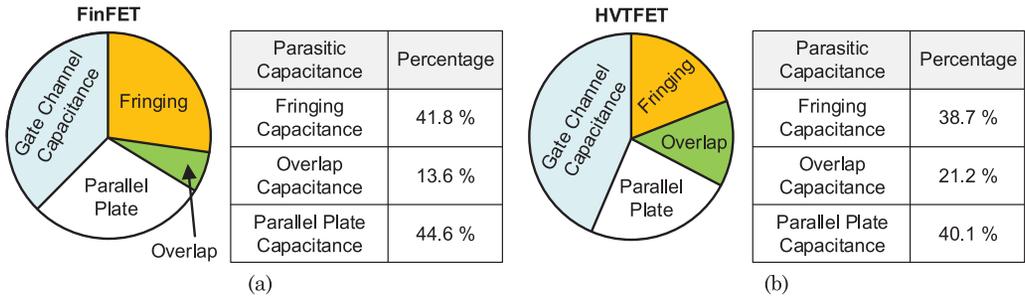


Fig. 14. The parasitic capacitance comparison based on the 14nm technology: (a) FinFET and (b) HVTFET.

FinFETs at a given  $W_{EMAX}$  (e.g., 39.7 aF for FinFETs and 36.9 aF for HVTFETs). HVTFETs exhibit larger reduction in  $C_{ov}$  compared to FinFETs as technology scales because  $W_E$  scales to a larger extent from the 22nm node to the 14nm node (Figure 4).

**4.1.4. Parasitic Capacitance versus Gate Channel Capacitance.** As CGP scales with technology, the parasitic capacitance ( $C_{par}$ ) becomes comparable and may even exceed the gate channel capacitance ( $C_g$ ) in FinFETs. The portion of  $C_{par}$  with respect to  $C_g$  increases further due to the reduced  $FP$  and higher  $H_{FIN}$  at the advanced technology nodes, as described in Figure 1. This trend is also shown in Figures 13 and 14(a), which illustrate the ratio of  $C_{par}$  and  $C_g$  at different technology nodes. At the 14nm node, for example,  $C_{par}$  is 66% of the total capacitance ( $C_{tot}$ ), for which the  $W_E$  is 276nm.

Figures 13 and 14(b) show the capacitance breakdown for HVTFETs. In contrast to FinFETs, the  $C_{tot}$ , including intrinsic gate channel capacitance and parasitic capacitances, decreases in accordance with shrinking MP0. This is the reason that the  $C_{fri}$ ,  $C_{pp}$ , and  $C_{ov}$  decrease accordingly because the  $W_E$  decreases (Figure 4) when the technology node moves from 22nm to 14nm with the reduced CH in nanometers (e.g.,  $FP \times 10$ ). For the ratio between  $C_{par}$  and  $C_g$ , as presented in Figure 13, the  $C_{par}$  is 62% of the  $C_{tot}$ , showing a similar result to FinFETs in the 14nm technology.

As shown in Figure 14,  $C_{par}$  exceeds over the  $C_g$  in both FinFET and HVTFETs. Two devices exhibit different percentages of fractions in the total capacitance. For FinFETs, fringing and parallel-plate capacitances are the dominant components of the  $C_{tot}$  because of the 3-D fin structure. On the other hand, for HVTFETs, the contributions of the fringing, parallel-plate, and overlap capacitances are almost even.

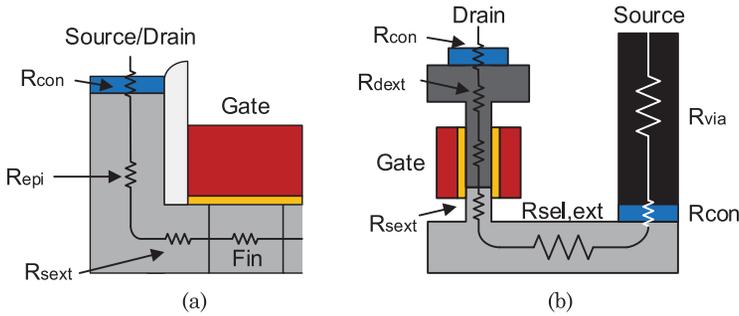


Fig. 15. The parasitic resistance modeling from device structures: (a) FinFET and (b) HVTFET (Note: Gate resistance ( $R_{gext}$ ) is not shown).

## 4.2. Basic Resistive Component Modeling

Parasitic resistance ( $R_{par}$ ) extraction is always a trade-off between accuracy and computing resources. As processes become denser, finding a trade-off is becoming more difficult because the process is becoming more complex and the number of gates is increasing. In this section, we discuss key parasitic resistances that lead to the significant degradation of  $I_{ON}$ .

There are two primary parasitic resistances: (1) gate resistance and (2) S/D series resistances. The gate parasitic resistance and capacitances (Section 4.1) are critical in determining the gate resistance–capacitance ( $RC$ ) delay [Wu and Chan 2007]. S/D parasitic resistance is also a crucial factor to determine the  $I_{ON}$  degradation compared to the ideal core device model without parasitics.

The main difference in the parasitic resistance of FinFETs and HVTFETs is that, unlike FinFETs, HVTFETs exhibit unequal source and drain resistances ( $R_s$  and  $R_d$ , respectively). The symmetric structure of FinFETs leads to the same parasitic resistances on the source and drain sides. However, unlike FinFETs, additional via required to place contacts on the bottom active region, asymmetric doping profile, and different heights of S and D pillars in HVTFETs lead to unequal  $R_s$  and  $R_d$ . In this section, we explore the parasitic resistances in HVTFETs and compare the parasitic resistances across FinFETs and HVTFETs.

**4.2.1. Analysis of Parasitic Resistance in Device Structures.** Figure 15 presents the parasitic resistances in the FinFET and HVTFET. For sake of simplicity, we assume that all regions have perfect rectangular shapes.

In FinFETs, the  $R_{par}$  due to the contact placement (both silicide and trench contact (MOA)), epitaxial diffusion region, and extension of the fin and gate are considered as presented in Figure 15. All geometry parameters are based on Table I and the contact material is assumed as tungsten (W). Also, the parameters of Silicon (Si) and SiGe related to the resistance are used for n- and p-type FinFETs, respectively.

HVTFETs also have the contact resistance ( $R_{con}$ ) and S/D extension resistance ( $R_{dext}$  or  $R_{sext}$ ). Further, the additional parasitic resistances, such as the bottom diffusion extension for the contact ( $R_{sel,ext}$ ) and via resistance ( $R_{via}$ ), are also considered since one of diffusion area (source or drain) is placed on the bottom, resulting in an additional via implementation on the bottom diffusion region, as mentioned earlier. The same geometry parameters and contact material are used. Other parameters related to the materials (i.e., resistivity, doping level, work function, and so forth) are based on Liu et al. [2013].

All resistances are calculated by Equation (11) with the resistivity of numerous materials if all regions corresponding to the device structures have perfect rectangular

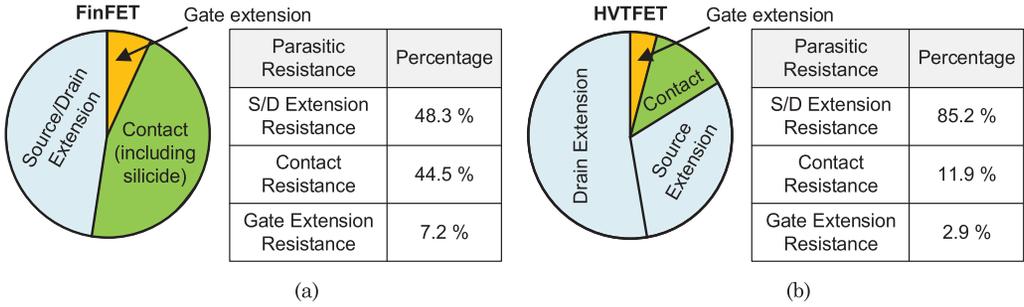


Fig. 16. The parasitic resistance comparison based on the 14nm technology: (a) FinFET and (b) HVTFET.

shapes:

$$Resistance[\Omega] = (\rho \cdot L)/A, \quad (11)$$

where  $\rho$  is the resistivity of a material,  $A$  is the orthogonal area related to the current path, and  $L$  is the length of the current route. The via resistance,  $R_{via}$ , for instance, depends on the dimensions (e.g., via size and height) and resistivity of the tungsten of the via. With an assumption of  $15 \times 15\text{nm}$  via cross-sectional area in 14nm node [Natarajan et al. 2014], the  $R_{via}$  and  $R_{silicide}$  are calculated as  $21.86 \Omega$  and  $85.43 \Omega$ , respectively.

Figure 16 summarizes the parasitic resistances for both FinFETs and HVTFETs. In FinFETs, the major components in the overall parasitic resistance are S/D extension resistance due to the thin body of fins and contact resistances, which are 49% and 28% of the total parasitic resistance, respectively. In HVTFETs,  $R_d$  is much larger than other parasitic components since HVTFETs have a longer drain pillar as opposed to a shorter source pillar due to the asymmetric doping [Liu et al. 2012].

The HVTFET requires a higher doping source to enable more tunneling current and a lighter doping drain to reduce the leakage current (e.g., the tunneling from drain-channel-source due to the unipolar transport). Hence, the junction line (channel drain) at the drain side will be pushed toward the drain contact more. In this case, a longer drain for HVTFETs is necessary to ensure that the drain depletion region is still within the device [Rajamohanam et al. 2013; Liu et al. 2012]. Due to a large  $R_d$  from Figure 16, the ratio of  $R_d$  and  $R_s$  is 60% and 37% even with  $R_{sel,ext}$  and  $R_{via}$ .

### 4.3. Parasitics by Series and Parallel Connections

Similar to the analysis of impact of different device architectures on the layout that we presented in Section 3, the analysis of the effect of parasitics in logic gates with series and parallel transistors is also crucial.

**4.3.1. Series Connections.** As discussed in Section 2, HVTFETs exhibit unidirectional conduction, originating from the asymmetric doping and p-i-n device structure. Because of this behavior, isolation is necessary to separate two transistors. This isolation results in an additional parasitic capacitance arising from the STI between HVTFETs when they are connected in a series (Figure 5 in series). Hence, increasing the number of series connections increases the parasitic capacitances compared to FinFETs. However, this capacitance originating from STI is not a prominent portion relative to other parasitic components due to fairly wide MP0 compared to other feature parameters. Therefore, the total capacitance and resistance can be calculated by the number of series transistors times the parasitics, resulting in more total parasitics than FinFETs,

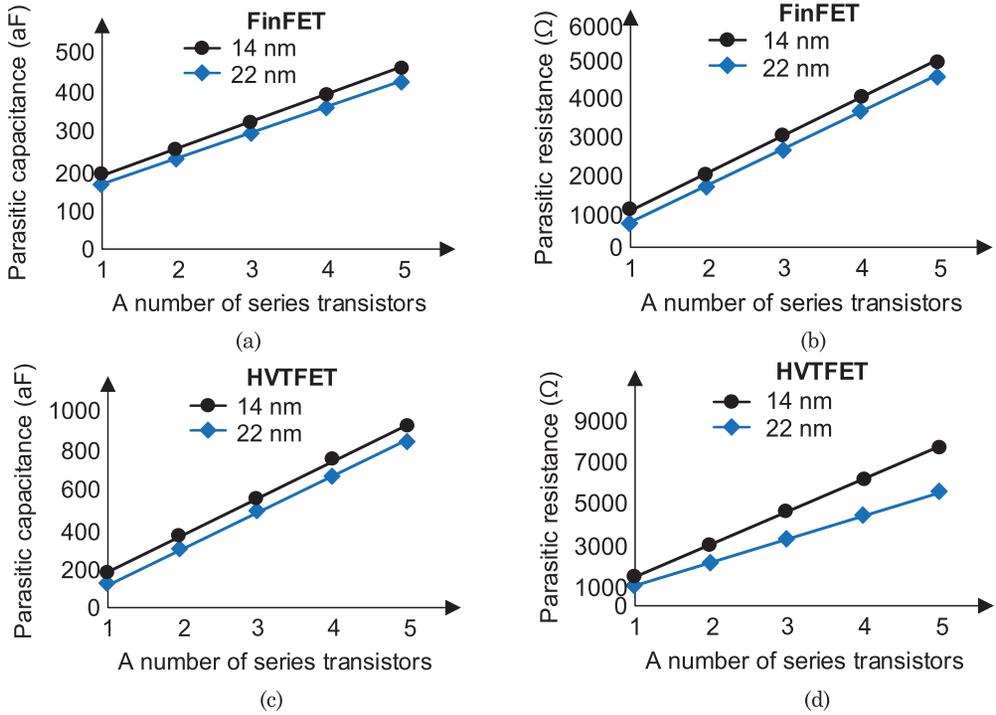


Fig. 17. The parasitic capacitance and resistance with a number of series transistors.

as shown in Equation (12) and Figure 17.

$$\begin{aligned}
 R_{tot-par(n),FinFET} &= R_{par,FinFET} + (n-1) \cdot (R_{epi} + R_{sext}) \approx n \cdot R_{par,FinFET} \\
 C_{tot-par(n),FinFET} &= 0.5(n+1) \cdot C_{par} - n \cdot C_{fringe-gate-contact} \\
 R_{tot-parasitic(n),HVTFET} &= n \cdot R_{par,HVTFET} \\
 C_{tot-par(n),HVTFET} &= n \cdot C_{par}
 \end{aligned} \quad (12)$$

where  $R_{tot-par}$  and  $C_{tot-par}$  are the total parasitic resistance and capacitance, and  $n$  is the number of transistor connections.

Unlike HVTFETs, FinFETs share a diffusion region between two gate electrodes in series, resulting in less parasitics than HVTFETs. As the number of series connections increases, additional parasitic capacitances by  $1 \times CGP$  are added, equal to  $3 F \times (\text{inner fringing capacitance and outer fringing capacitance}) + (1 \times C_{fringe-gate-contact}) + C_{Epi}$ . For resistance, since one diffusion area is shared, half of the total parasitic resistance in a single-finger FinFET is added when the number of series connections increases.

The parasitic capacitance and resistance in series connections are presented in Figure 17. When the number of series connections exceeds 2, the total parasitic capacitance in HVTFETs becomes larger than FinFETs. In addition, the total parasitic resistance in HVTFETs is always worse than FinFETs because of (a) unique geometry structure (e.g., asymmetric pillar heights for each source and drain) [Mohata et al. 2012], (b) electrical parameters (e.g., resistivity) [Liu et al. 2013], and (c) isolation between active area [Liu et al. 2013] in HVTFETs, especially for a larger number of series transistor connections.

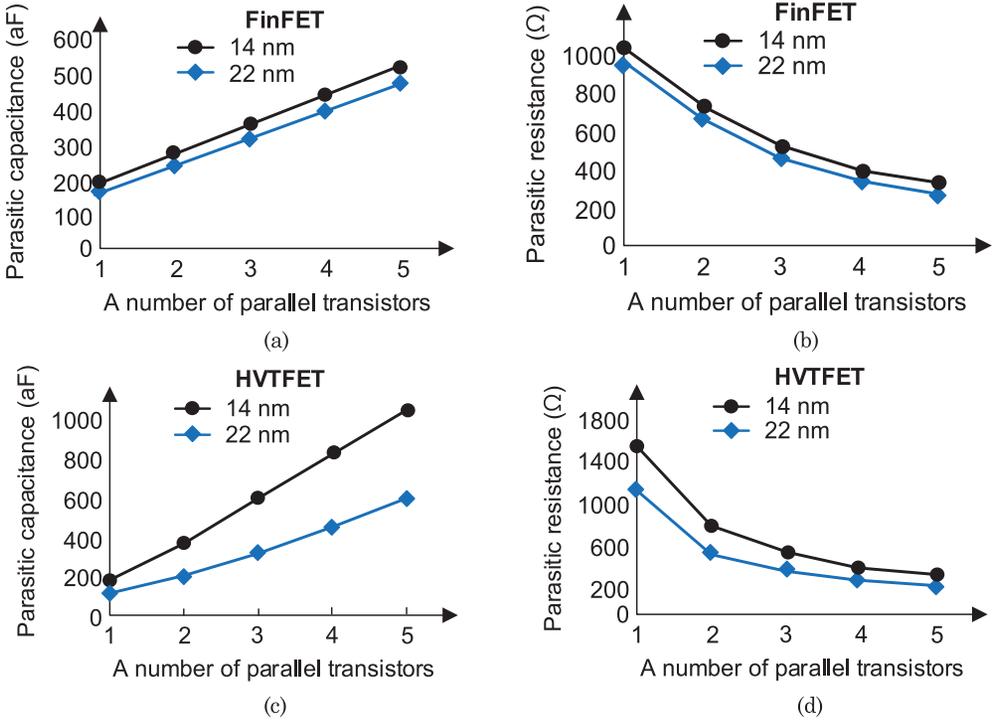


Fig. 18. The parasitic capacitance and resistance with a number of parallel transistors.

**4.3.2. Parallel Connections.** Figure 18 depicts the  $R_{par}$  and  $C_{par}$  when a number of parallel connections increase. As opposed to the series connections, the STI isolation is not necessarily placed and the bottom source is shared by parallel transistors, leading to a decrease of the parasitic resistance for HVTFETs. In the case of parasitic capacitance, the capacitance increases when a number of transistors are connected in parallel similar to the series connections. However, the relationship of the increased capacitance due to parallel connections is not linear because of the shared bottom source, as expressed in Equations (13.1) and (13.2).

$$R_{tot-par(n),FinFET} = \begin{cases} \frac{4}{n+1} R_{par,FinFET}, & \text{if } n = \text{odd}, \\ \frac{4n+4}{n^2+2n} R_{par,FinFET}, & \text{if } n = \text{even} \end{cases}$$

$$C_{tot-par(n),FinFET} = 0.5(n+1) \cdot C_{par} \quad (13.1)$$

$$R_{tot-parasitic(n),HVTFET} = \begin{cases} R_{par,drain} + R_{par,source} & \text{if } n = 1, \\ \frac{1}{n} R_{par,drain} + \frac{1}{n-1} R_{par,source} & \text{if } n > 1 \end{cases}$$

$$C_{tot-par(n),HVTFET} = \begin{cases} n \cdot C_{par}, & \text{if } n < 3 \\ n \cdot C_{par} + (n+1)C_{par,via}, & \text{if } n \geq 3 \end{cases} \quad (13.2)$$

When two transistors are connected, the parasitic capacitance is also doubled, but the additional  $C_{ds,ext}$  and  $C_{gs,via}$  are added when the number of parallel connections exceeds two ( $\geq 3$ ) due to the via implementations between drain electrodes, resulting in higher parasitic capacitance than FinFETs.

For FinFETs, the parallel connections bring slightly larger  $C_{par}$  and  $R_{par}$  compared to the series connections because of the additional contact to gate electrode fringing

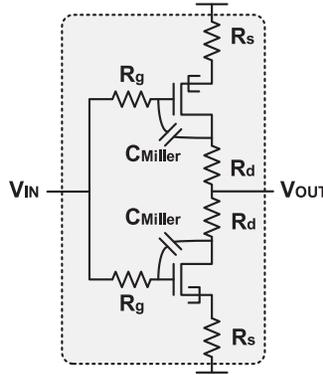


Fig. 19. The major parasitic components ( $R_g$ ,  $R_s$ ,  $R_d$ , and Miller capacitance) in an inverter.

capacitance ( $C_{fringe-gate-contact}$ ),  $R_{con}$ , and  $R_{silicide}$ . However, both  $C_{par,FinFET}$  and  $R_{par,FinFET}$  are lower than HVTFETs when the number of parallel connections exceeds 3. This is because HVTFETs need via implementations in every parallel connection, leading to the additional resistance and capacitance through vias compared to FinFETs. Although  $R_{via}$  can be decreased by the increase of a number of parallel connections, the  $R_{par}$  of HTVTFETs are still larger than FinFETs due to  $R_{via}$ .

## 5. CIRCUIT PERFORMANCE WITH PARASITICS

Circuit performance is determined not only by the parasitic capacitance, including Miller capacitance, but also by S/D resistances. As the dimensions of transistors shrink, the impacts of S/D resistances increase due to the reduction of the contact dimensions. Figure 19, for instance, shows the major parasitic components in an INVX1, including  $C_{pp}$  and  $C_{fri}$  as the Miller capacitance incorporated with  $C_{gs}$  and  $C_{gd}$ , and S/D resistances.

### 5.1. Model Refinement

The simulation models based on the geometric device dimensions, material profiles, and layouts are inevitable to extract the parasitics in logic cells for performance evaluations. In the previous section, we consider the layout and 3-D device dimensions-based parasitics according to the device metrics (Table I) in both FinFETs and HVTFETs as well as the parasitics as a function of the number of parallel and series transistors. In this section, we introduce the full schematics of implemented parasitics models with an ideal device model [Liu et al. 2013] for both FinFETs and HVTFETs, as illustrated in Figure 20. To implement the parasitics, the equations mentioned in previous sections for parasitic calculations, including the parallel and series transistor connections, are incorporated with the existing Verilog-A model [Liu et al. 2014].

In this model, we assume that all the geometry dimensions are the same for p- and n-type transistors except the drain (D) and source (S) heights in HVTFETs due to the dependency of the asymmetric doping (Section 4.2). For other parameters determined by materials, the resistivity and dielectric constants of SiGe for p-type FinFETs are used for the epitaxial materials [Yakimets et al. 2015a, 2015b; Bardon et al. 2015].

For HVTFETs, the  $C_{fri}$  and  $C_{pp}$  for the drain and source are connected in parallel to the gate. Capacitances associated with the vias  $C_{gs,via}$  and  $C_{ds,via}$  are also modeled. Further, all the parasitic resistances based on the device structure and layouts, including  $R_{via}$ , are included in the Verilog-A model. Like HVTFETs, all the parasitic components

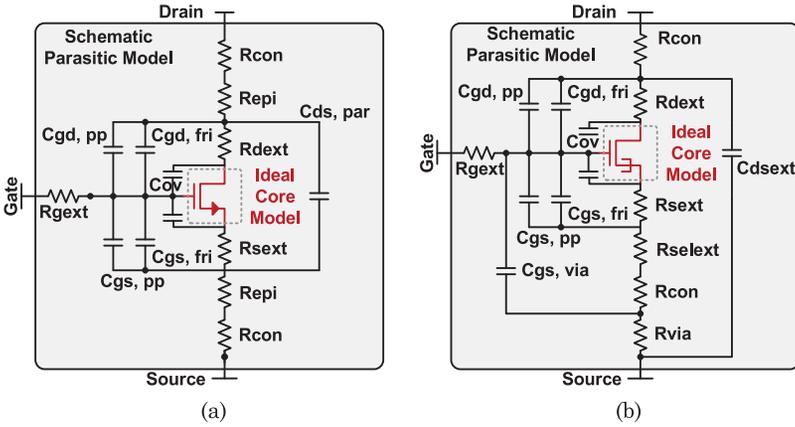


Fig. 20. The parasitic elements modeling in the schematic view: (a) FinFETs and (b) HVTFETs.

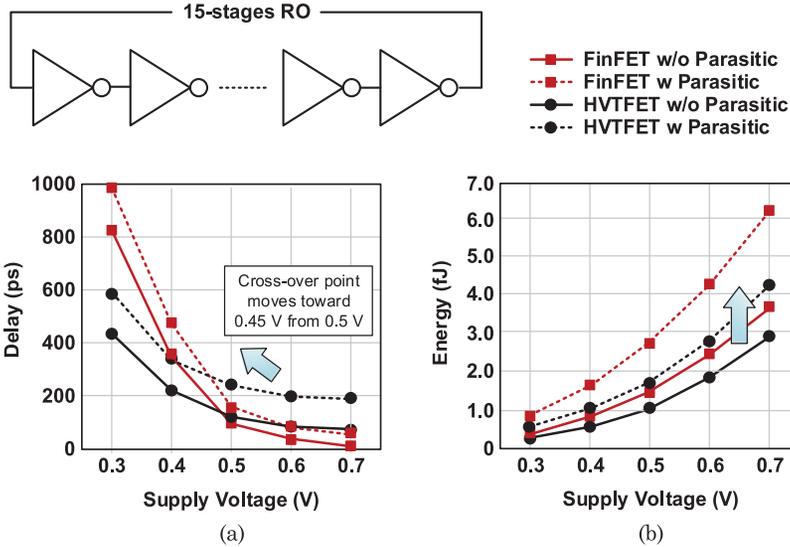


Fig. 21. Delay and energy comparison in 15-stage RO without/with parasitics.

induced by the geometric device structure, number of fins and layouts are incorporated except the parasitics from the not-self-aligned vias in FinFETs.

### 5.2. Ring Oscillator (RO)–Based Benchmarking.

For the benchmarking, we use the 15-stage INVX1-based RO with parasitics discussed earlier but ignore those due to interconnections. In order to analyze the impacts of parasitics, the simulations are performed using models with and without the device parasitics in SPICE. All the CHs of INVX1 are set to 7.5 T based on the metal pitch as described in Section 2.

Figure 21 shows the delay and energy comparisons without and with parasitics for FinFET and HVTFET [Liu et al. 2013] based on geometric parameters in 14nm technology node (Table I) at multiple supply voltages. At a 14nm technology node, the electrical width is set to 276nm for FinFETs and 268nm for HVTFETs for each p- and n-type transistor, as shown in Figure 4. For comparisons, the delay and energy

cross-over point is observed near 0.45V. Below this point, HVTFETs outperform FinFETs even with smaller  $W_E$  because of the larger current driving ability (high  $I_{ON}$ ) stemming from steep-slope switching [Mohata et al. 2012; Liu et al. 2013]. However, over 0.45V, FinFETs can provide better performance due to higher current driving ability of FinFETs at a higher  $V_{DD}$  [Mohata et al. 2012; Liu et al. 2013]. The parasitics lead to an approximately 20% delay degradation in HVTFETs. The delay increase in FinFET-based cells because of parasitics is less than 12%. The larger degradation of delay in HVTFETs compared to FinFETs is due to (a) an increase in parasitic capacitances, mainly  $C_{fri}$  and  $C_{pp}$ , and (b) relatively higher parasitic resistance ( $R_s$  and  $R_d$ ) plus the bottom diffusion area extension ( $R_{sel,ext} + R_{via}$ ) for the vias.

The energy comparison is shown in Figure 20(b). The FinFETs have not only larger  $W_E$  but also the  $1.2\times$  higher total capacitances, including intrinsic and parasitic, than HVTFETs, resulting in higher energy compared to HVTFETs [Liu et al. 2012, 2013]. Further, for the evaluation with parasitics, as presented in Figure 13, the parasitic capacitances in FinFETs are also more than HVTFETs, leading to 36% higher energy. Figure 20(b) shows that energy efficiency degrades approximately 47% with parasitics at various  $V_{DDs}$  compared to the results without parasitics.

## 6. CONCLUSION

In this article, we have examined the layout implications of the asymmetric vertical heterojunction tunnel FET (HVTFET) compared to FinFETs for a standard cell library with a fixed height of  $7.5 \times$  metal 2 pitch (7.5 T). The benefits and trade-offs in the layout analysis are also investigated by considering parallel and series transistor connections based on the Boolean function implementations in logic cells. In addition, the device parasitics are explored for both FinFETs and HVTFETs. The total parasitics in HVTFETs and FinFETs are compared with various technology dimensions. Also, the parasitics related to series and parallel transistor connections are evaluated to explore the benefits and trade-offs in the logic cells. In this analysis, the parasitic capacitance of one transistor is lower than FinFETs. However, the parasitic capacitance increases significantly with more series or parallel transistor connections. In most cases, more than two transistor connections exhibit more parasitic capacitance. For parasitic resistances, HVTFETs always show more parasitics than FinFETs due to high drain pillar resistance and additional  $R_{via}$ . Further, in order to investigate the impacts on circuit performance, we have incorporated the parasitic capacitance and resistance in a Verilog-A model, and examined the impacts of parasitics in the 15-stage ring oscillator. Based on the benchmarking, although HVTFETs have more performance degradation with parasitics, HVTFETs still can provide higher energy efficiency at various supply voltages (0.3V–0.7V) than FinFETs.

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