A 14-bit 250-MS/s current-steering CMOS digital-to-analog converter*

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Abstract: A 14-bit 250-MS/s current-steering digital-to-analog converter (DAC) was fabricated in a 0.13 μm CMOS process. In conventional high-speed current-steering DACs, the spurious-free dynamic range (SFDR) is limited by nonlinear distortions in the code-dependent switching glitches. In this paper, the bottleneck is mitigated by the time-relaxed interleaving digital-random-return-to-zero (TRI-DRRZ). Under 250-MS/s sampling rate, the measured SFDR is 86.2 dB at 5.5-MHz signal frequency and 77.8 dB up to 122 MHz. The DAC occupies an active area of 1.58 mm^2 and consumes 226 mW from a mixed power supply of 1.2/2.5 V.

Key words: DAC; current-steering; SFDR; wide-band; time-interleaved

DOI: 10.1088/1674-4926/34/8/085013 **EEACC:** 2570

1. Introduction

With the increasing development of both wired and wireless communications, data processing is moving towards the digital domain to provide services with higher quality at a lower cost[1−5]. In these applications, wide-band digital-to-analog converters (DACs) with a high spurious-free dynamic range (SFDR) have been a critical component in the interface between the digital processors and the analog world[1−5].

Many papers have been published on the design of wide-band high-SFDR CMOS DACs in recent years[1−4]. It has been revealed that the nonlinear distortions in the code-dependent switching glitches are one bottleneck in these designs[1, 4−7]. This paper presents a 14-bit 250-MS/s current-steering DAC in 0.13 μm CMOS process, using time-relaxed interleaving digital-random-return-to-zero (TRI-DRRZ) to overcome this bottleneck. When sampled at 250-MS/s, the measured SFDR is 86.2 dB at 5.5-MHz signal frequency and 77.8 dB up to the Nyquist band.

2. Solutions to the code-dependent switching glitches

For wide-band digital-to-analog conversions, current-steering architecture has been widely used because of its intrinsic high speed and ability to drive resistive loads directly[1−7]. Figure 1 shows a diagram of the traditional current-steering DAC architecture, where a series of weighted current sources are switched to the output port according to the decoded digital inputs. The output current of the DAC forms a differential voltage on the differential resistive loads. The current sources in Fig. 1 can also be realized with NMOS transistors, along with NMOS switches and resistive loads connected to the power supply.

The switching operations in Fig. 1 also cause undesired code-dependent glitches with nonlinear distortions in the output. As the control signals of the switches change, the direct coupling through the capacitance between the gates and the current output routes causes fluctuations at node X and the output terminals. Another factor is the charge or discharge at node X if the current sum of the two switches does not equal I_0 when switching. In traditional designs where the control signals are code-dependent, these glitches are also code-dependent. The second-order and third-order harmonics in the spectrum of the glitches limit the SFDR of the DAC. As the signal frequency increases, the switch changes more frequently and the energy of the glitches increases. As a result, this effect has become a bottleneck in designing wide-band DACs with a high SFDR.

There are two main types of solutions to the nonlinear distortions in code-dependent switching glitches. The first type focuses on reducing the energy of the glitches. For example,

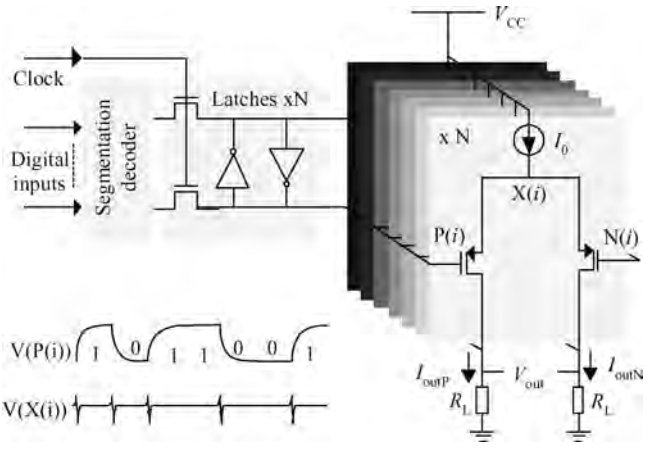

Fig. 1. The traditional current-steering DAC architecture and code-dependent switching glitches.

* Project supported by the National High Technology Research and Development Program of China (No. SS2013AA011203) and the Specialized Research Fund for the Doctoral Program of Higher Education of China (No. 20110002110058).

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Received 9 January 2013, revised manuscript received 4 March 2013

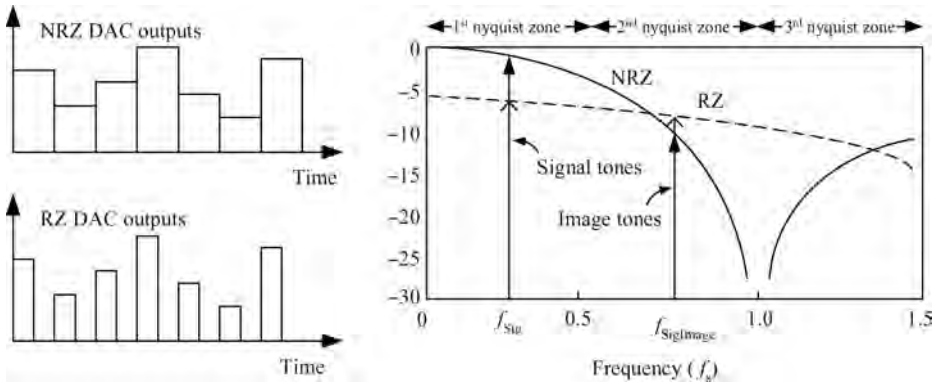


Fig. 2. The $sinc$ roll-off in the spectrum of NRZ, RZ outputs[9].

the coupled energy through the capacitance could be reduced by lowering the voltage swing of the control signals, and by minimizing the switch sizes[6, 7]. Appropriate crossover point adjustment of the differential control signals also helps to reduce the charge or discharge at node X[8]. Return-to-zero (RZ) techniques to short the output to ground when switching are another effective way to isolate the output from glitches[5, 9].

The second type of solution turns the nonlinear distortions into noise instead of nonlinear distortions. For example, quad-switching techniques for constant switching glitches in each clock cycle[4, 8] and random switching techniques[3, 10]. The DRRZ approach[1] utilizes both RZ and random switching techniques, being the first CMOS DAC with $>$ 70 dB SFDR up to 500-MHz signal frequency. However, there are several disadvantages in the RZ (and DRRZ) techniques. The first one is the tightened timing requirements by the RZ operations, in which both the output current and the control signals need to settle within half a clock cycle. This fact makes it more challenging to design a high-speed DAC. The other disadvantages are illustrated in Fig. 2, where the spectral roll-off in both non-return-to-zero (NRZ) and RZ outputs is plotted for comparison. Due to the RZ operations, the signal loss of the RZ output is -6.0 dB at DC and -6.9 dB at $f_s/2$, where f_s is the sampling frequency[9]. More importantly, as illustrated in Fig. 2, the roll-off envelope of RZ outputs is flattened by the RZ operations, which makes the anti-aliasing filter design much more difficult.

To prevent the disadvantages in using RZ techniques, the TRI-DRRZ approach is employed in this paper to suppress nonlinear distortions. The function diagram is illustrated in Fig. 3, where an additional identical sub DAC and a pseudo random number generator (PRNG) are used. In $(2n)$th clock cycle, $n = 0, 1, 2,\ldots$, the segmentation decoder controls subDAC-1 to give an NRZ output, while the PRNG controls subDAC-2 to return to zero. The RZ operation of subDAC-2 is achieved by randomly selecting half of the DAC's current to the positive output port and the left current to the negative output port. In $(2n + 1)$th clock cycle, $n = 0, 1, 2, \ldots$, the actions of subDAC-1 and subDAC-2 interchange, i.e., subDAC-1 returns to zero and subDAC-2 gives an NRZ output. The DAC's outputs are illustrated in Fig. 3(b).

After inserting random RZ operations in the TRI-DRRZ, the switching glitches in each current source and switch unit are no longer code-dependent. As a result, the nonlinear distortions are significantly suppressed. As illustrated in Fig. 3(b), the signal-energy loss problem due to RZ operations is solved by the time-interleaving technique. In addition, the timing problem is also solved by reducing the RZ operations of each current source and switch unit to once in $2T_{\rm clk}$, rather than once in a $T_{\rm clk}$ as in conventional RZ techniques ($T_{\rm clk}$ represents a clock cycle).

It should be noted that the signal-energy loss problem could be solved by a parallel dual RZ scheme operating in opposite clock phases[5]. However, this method does not solve the timing problem. On the contrary, the proposed TRI-DRRZ approach not only solves this timing problem, but also delivers an SFDR higher than a traditional dual RZ scheme. This is because the number of switching times in a TRI-DRRZ DAC, as shown in Fig. 3, is only half of that in the parallel dual RZ solution. In other words, the energy of nonlinear distortions due to switching is reduced by 6 dB. Compared with DRRZ, the SFDR of TRI-DRRZ is also higher, because the signal energy is increased while the number of switching times remains the same.

The penalty of using TRI-DRRZ is the additional cost of power consumption and silicon area. As illustrated in Fig. 3, a PRNG generator, a swapper, and an additional sub-DAC are obligatory. Most of the increase of the power and silicon area come from the additional sub-DAC, which doubles the power and chip area of analog blocks, i.e., current sources and switches.

In this paper, the PRNG generator is realized by using a linear-feedback-shift-register (LFSR), as illustrated in Fig. 4. The LFSR uses 35 registers, of which the states are represented as $D[i][k]$ in kth clock cycle, $i = 1, 2, 3, \ldots, 35$. The feedback function the LFSR is set to be

$$D[i][k+1] = D[i][k] \oplus D[i+2][k], \quad i = 1, 2, 3, \ldots, 33, \tag{1}$$

$$D[34][k+1] = D[1][k], \tag{2}$$

$$D[35][k+1] = D[2][k]. \tag{3}$$

The sequence length of the LFSR in Fig. 4 is 2^{35}–1, which is sufficiently large to maintain the required randomization. In each clock, the LFSR has a 35-bit parallel output $D[1 : 35]$, which will be used to control the switches in the two sub DACs.

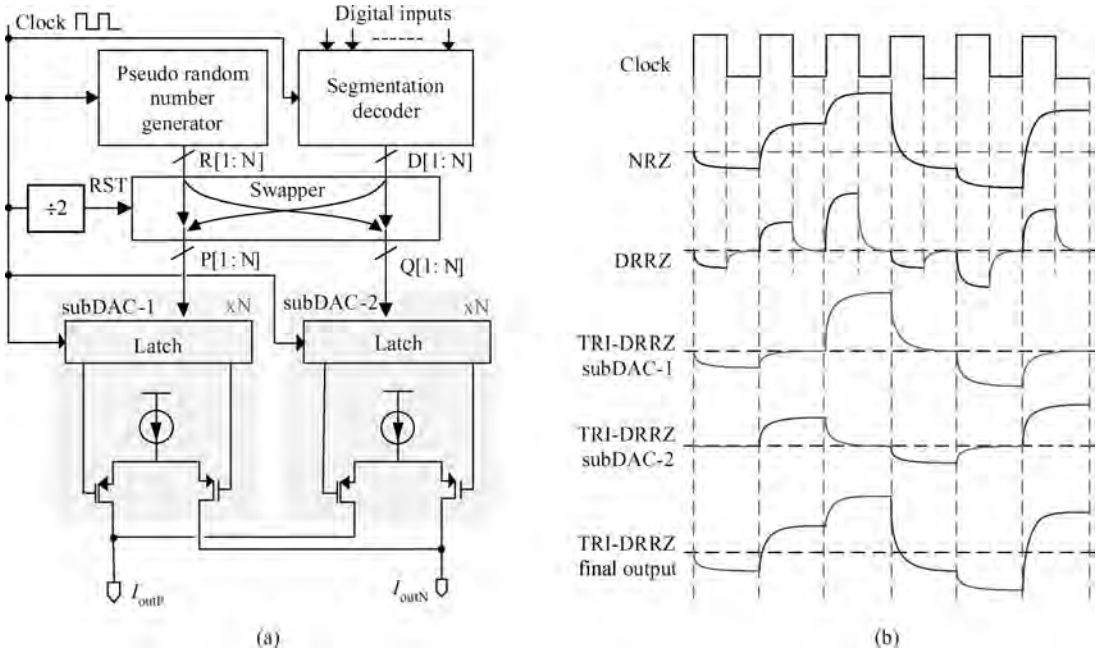


Fig. 3. The applied TRI-DRRZ approach to suppressing code-dependent switching glitches.

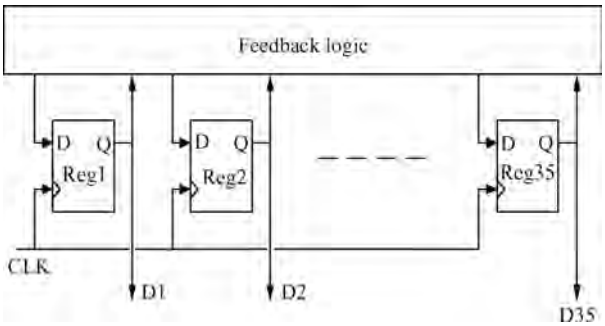


Fig. 4. The PRNG generator.

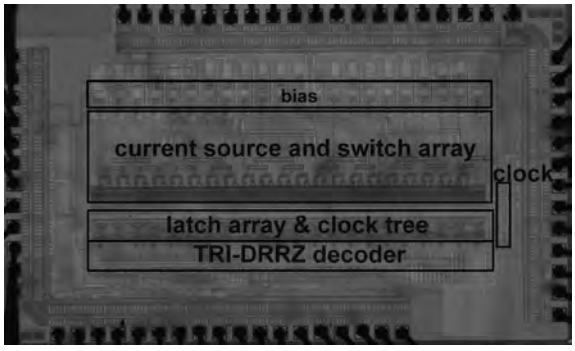


Fig. 5. Micrograph of the fabricated DAC.

3. DAC implementations

Figure 5 shows the micrograph of the fabricated 14-bit 250-MS/s DAC in 0.13 μm CMOS process. The size of the entire chip is 2.5 × 1.5 mm^2, with an active area of 1.86 × 0.85 mm^2. In the following, the DAC architecture, current source and switch units, latches, and the TRI-DRRZ realizations will be introduced.

3.1. DAC architecture

Figure 6 illustrates the DAC architecture. The 14-bit digital binary input is decoded into three segments: 6 most-significant bits (MSB), 4 upper-significant bits (USB), and 4 least-significant bits. In each sub DAC, the MSB and USB segments are thermometer-decoded to control $2^6 - 1 = 63$ and $2^4 - 1 = 15$ unary current sources, respectively. The LSB segment is binary-decoded to control 4 binary-weighted current sources. The current output of all MSB, USB, and LSB segments in two sub DACs forms a full-scale differential current output of 16 mA. The resistive load on each output port of the DAC is 25 Ω. The differential output voltage is 0.8 Vpp. This DAC has a mixed power supply of 2.5 V (analog) and 1.2 V (digital).

3.2. The current source and switch unit

Figure 6 also shows the current source and switch unit of the DAC. Each current source in the MSB segment generates a nominal current of $16I$, and a current source in the USB segment generates I. The current in the LSB segment is scaled according to the weight of each bit. For static matching, the current source of I in the USB segment is reused in the MSB and LSB segments. In the MSB segment, 16 such current sources are connected in parallel. In the LSB segment, the current source of I is divided by the cascode current transistor into two parts: the required signal current and a dummy current. Dummy switches are also added in the USB and LSB segments for the same load of the control signals.

Matching between the current sources is important, because insufficient matching results in a large integral nonlinearity (INL) and deteriorates the SFDR. It is revealed that the relative standard deviation of a LSB current source $\sigma(I)/I$ needs to satisfy

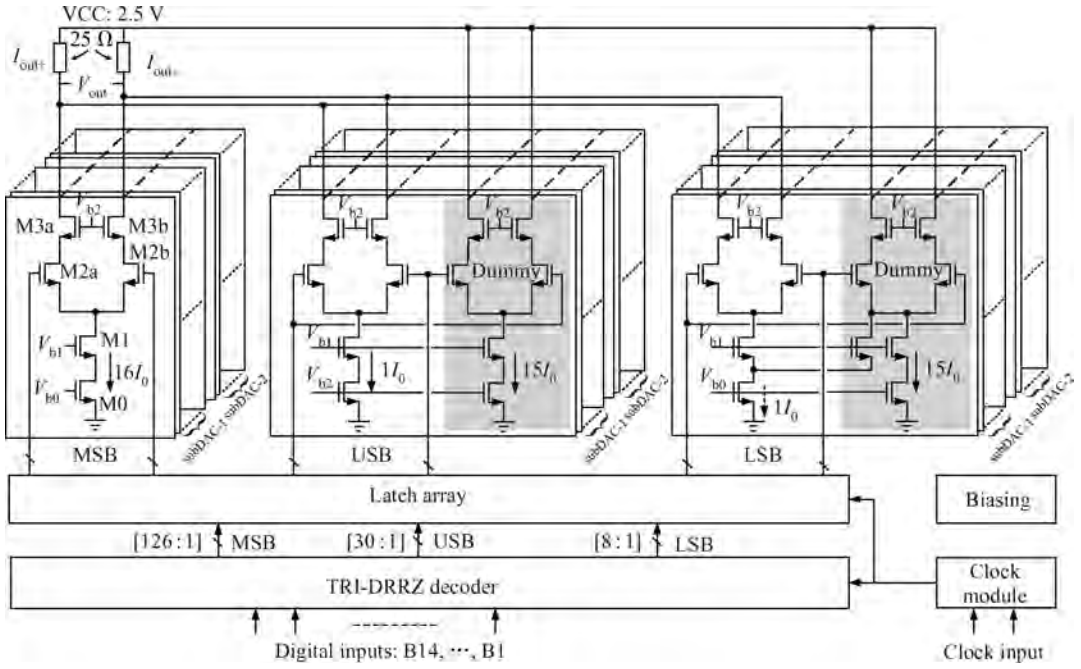


Fig. 6. DAC architecture.

$$\sigma(I)I \leqslant (2^N C)^{-0.5} \text{ with } C = \text{inv\_norm}(0.5 + \text{Yield}/2), \tag{4}$$

where N is the DAC resolution, inv_norm is the inverse cumulative normal distribution, and Yield is the expected relative number of DACs with an INL < 0.5 LSB[11]. In this 14-bit DAC design, the required $\sigma(I)/I$ should be less than 0.61% for Yield $= 90.0\%$. Then the required transistor area of the LSB current source could be obtained through

$$S_{\min} = \left[\frac{2A_{\text{VT}}^2}{(V_{\text{gs}} - V_{\text{th}})^2} + \frac{A_\beta^2}{2}\right] \Big/ \left[\frac{\sigma(I)}{I}\right]^2, \tag{5}$$

where A_{VT} and A_β are technology parameters[12].

High output impedance of the current source and switch unit is also important for wide-band DACs, because it affect SFDR as:

$$\text{SFDR} = (2^{2-N} Z_{\text{O}}/R_{\text{L}})^2, \tag{6}$$

where R_{L} is the resistive load on each port of the DAC, N is the resolution of the DAC in bits, and Z_{O} is the output impedance of the LSB current source and switch unit[2]. For high output impedance, the sizes of the switches M1, M2a, M2b, M3a, and M3b are minimized for minimum capacitance.

3.3. Layout of the current source and switch unit

Figure 7 shows the layout diagram of the MSB current source and switch unit in Fig. 6, where all the transistors are placed close together for the shortest interconnection. By doing this, the parasitic capacitance is also minimized for the highest output impedance to satisfy the requirements in Eq. (6). As a result, all the current source and switch units are placed in parallel in a line (which is different from traditional 2-D layout floorplan), forming a current array of about 400×1700 μm^2.

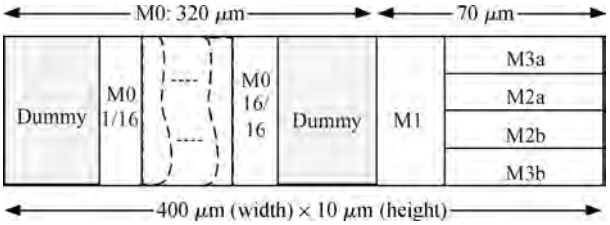


Fig. 7. The layout of the MSB current source and switch unit in Fig. 6 for high output impedance.

In the large 1-D current source array, it should also be noted that the gradient matching errors limits the matching between two distant current sources. The gradient errors are mainly a result of fabrication non-idealities, such as the oxide thickness gradients and doping gradients[13]. Figure 8 shows typical linear and quadratic gradient error distributions in the chip when all the current sources share the same biasing voltage[13]. It is generally assumed that linear and quadratic gradient error distributions are adequate to model the gradient errors in a chip. As illustrated in Fig. 8, the matching errors between distant current sources must be carefully dealt with to guarantee the required matching requirements. In this paper, the biasing technique in Ref. [14] is employed. The entire current source array is partitioned into several smaller blocks, inside which local biasing provides the biasing voltages. All local biasing currents are generated from an accurate global biasing array. Because all current sources inside a small block match well and all local biasing currents are accurately generated, the gradient matching error between two distant current sources are significantly reduced[14].

3.4. The fast latch

Figure 9 shows the fast latch for synchronizations of the switch control signals. The clock input of the latch induces

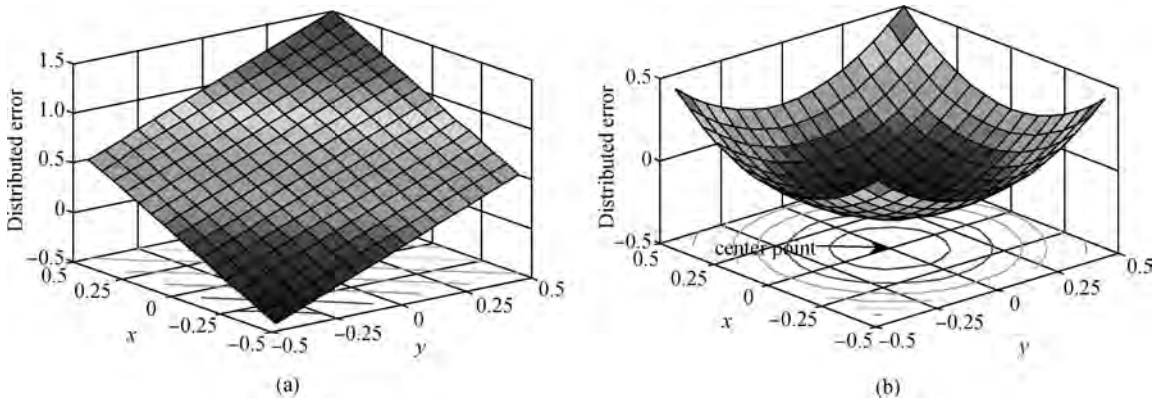


Fig. 8. Typical zero-averaged models of gradient error distributions in the chip. (a) Linear errors. (b) Quadratic errors.

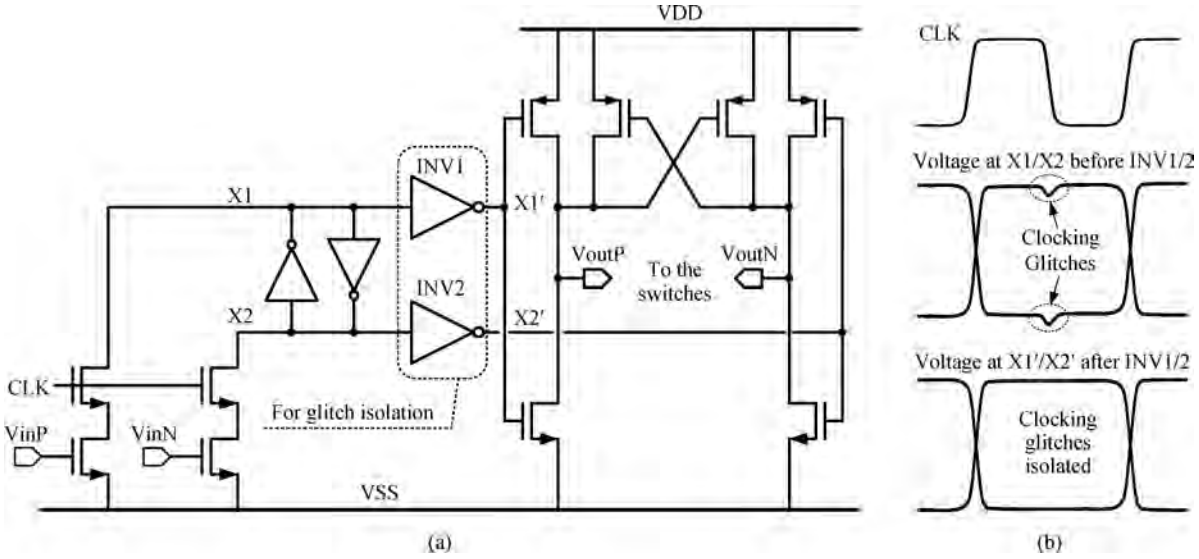


Fig. 9. (a) The applied latch and (b) the corresponding waveform illustrations of nodes X1/X2/X1'/X2'.

glitches at nodes X1 and X2 at every edge of the clock. To prevent glitches at nodes X1 and X2 spreading to the gates of the switches in the current routes, an additional two inverters, i.e., INV1 and INV2 in Fig. 9 are added to the latch in Ref. [2]. With INV1 and INV2, the clocking glitches are isolated because the gain of an inverter is far less than one with such a glitch input around VDD or GND. INV1 and INV2 may also help for larger driving ability. The transistors in the latch are sized for a proper crossover point of VoutP and VoutN in Fig. 9 to minimize the glitch energy in the DAC's output.

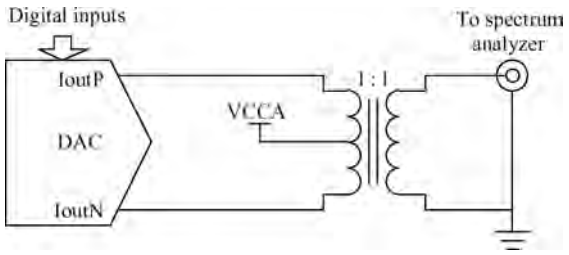


Fig. 10. The measurement setup diagram.

4. Measurement results

Figure 10 shows the dynamic measurement setup. The differential output of the DAC is connected directly to a transformer with an impedance conversion of 1 : 1. The output of the transformer is synthesized by a spectrum analyzer. In this setup, the spectrum analyzer provides a load of 50 Ω to the DAC through the transformer. Because the full-scale differential output current is 16 mA in the measurements, the signal provided by the DAC has a 0.8 Vpp amplitude and 2.0 dBm power.

Figure 11 shows that the 14-bit DAC has a measured INL of −4.39 LSB. The differential nonlinearity (DNL) is 2.22 LSB. Considering no calibration is applied, the effectiveness of the layout implementations is confirmed by the INL performance.

Figure 12 shows the single-tone spectra with TRI-DRRZ OFF at 250 MS/s. The measured SFDR is 75.36 dB at 5.5 MHz signal frequency and 69.37 dB at 122 MHz. Figure 13 shows the measured spectra with TRI-DRRZ ON at 250 MS/s. The SFDR is 86.18 dB at 5.5 MHz and 77.83 dB at 122 MHz. The SFDR improvement is 10.82 dB at 5.5 MHz and 8.46 dB at 122 MHz.

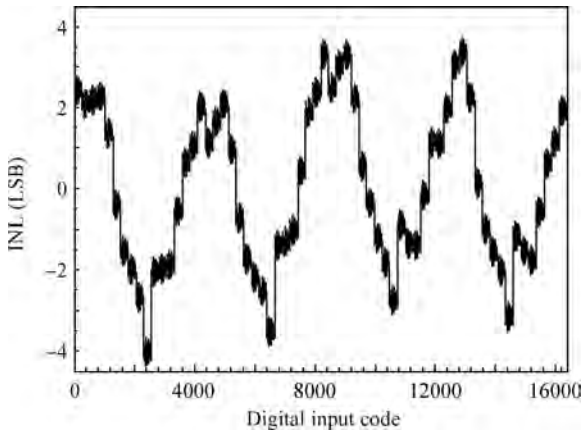
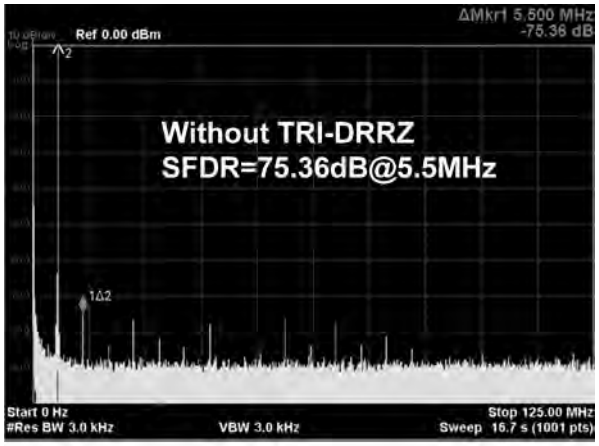
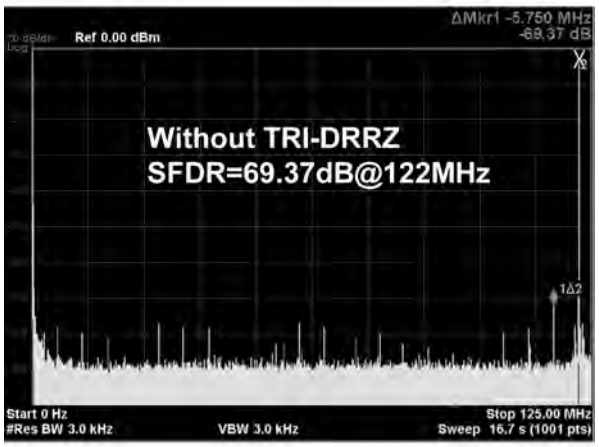


Fig. 11. The measured INL performance of the 14-bit DAC.

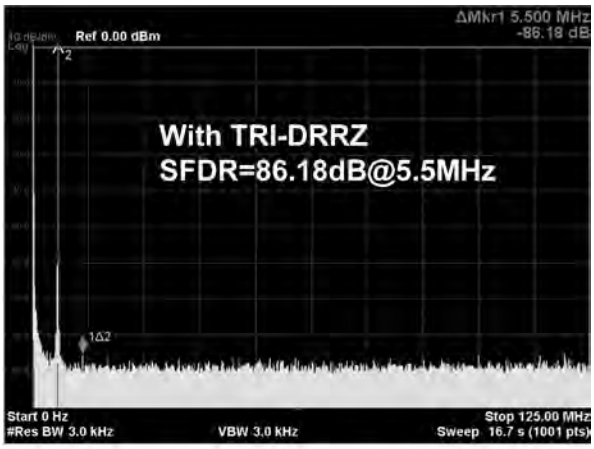


(a)

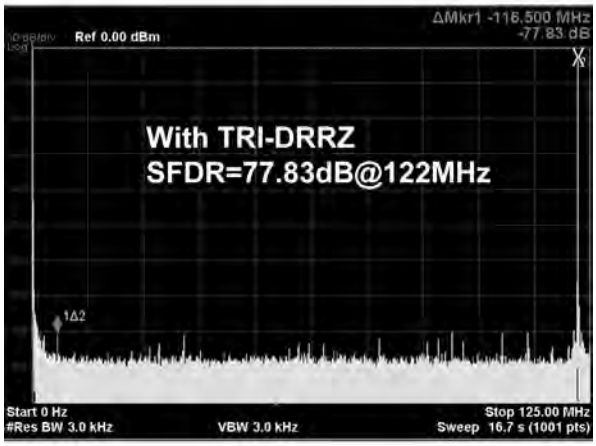


(b)

Fig. 12. The measured SFDR without TRI-DRRZ at (a) 5.5-MHz and (b) 122-MHz.



(a)



(b)

Fig. 13. The measured SFDR with TRI-DRRZ at (a) 5.5-MHz and (b) 122-MHz.

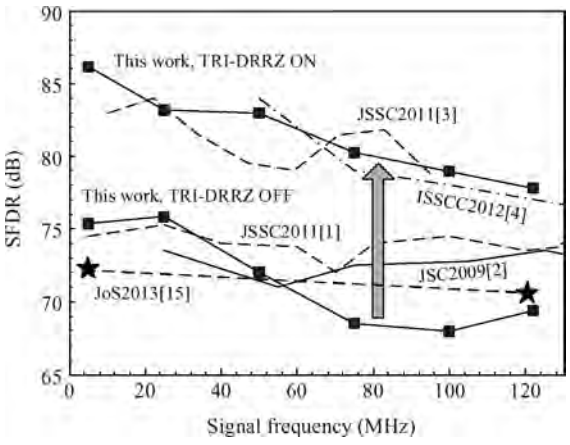


Fig. 14. SFDR performance comparison.

Table 1 shows the comparisons with recently published 12–14-bit CMOS DACs with ⩾ 200-MS/s sampling rates. Meanwhile, Figure 14 plots the SFDR curves of these DACs. After enabling TRI-DRRZ, the SFDR of this design is increased by about 10 dB, achieving > 77.8 dB SFDR in the entire Nyquist band. Compared with Refs. [1, 2, 15], the SFDR of this design within the entire Nyquist band is the highest. Compared with Ref. [3], this design has higher bandwidth and comparable SFDR. Compared with Ref. [4], the design occupies a much smaller active chip area and needs no negative power supply. To evaluate these DACs comprehensively, the figure of merit (FOM)[1, 16] is adopted as

Table 1. Comparisons between recently published ⩾ 200-MS/s, 12–14-bit CMOS DACs.

Specifications	This work	JSSC2011[1]	JSSC2009[2]	JSSC2011[3]	ISSCC2012[4]	JoS 2013[15]
Technology (nm)	130	90	65	140	180	65
Core area (mm^2)	1.58	0.825	0.31	1.27	4.0	1.56
Supply (V)	1.2/2.5	1.2/2.5	1.0/2.5	1.8	–1.5/1.8/3.0	1.0/2.5
Sampling rate (GS/s)	0.25	1.25	2.9	0.2	3 ∼ 6	1.0/0.25
Resolution (bits)	14	12	12	14	14	14
INL/DNL (LSB)	4.4/2.2	1.2/0.51	0.5/0.3	1.8/2	–	2.5/1.6
Calibration	No	Yes	No	DMM	–	Yes
Full-scale current (mA)	16	16	50	20	20	16
DAC power (mW)	226	128	188	270	600	82@1.0-GS/s
$SFDR_{LF}$	86.2	75	74	84	84.5	72.4@250-MS/s
$SFDR_{f_s/2}$	77.8	66	52	78	52	70.1@250-MS/s
FOM in Eq. (7) (10^4 Hz/mW)	11.8	7.32	2.09	6.24	4.48	4.42@250-MS/s
Approach for high SFDR	TRI-DRRZ	DRRZ	Always-on biasing	DMM	Quad-switching	[2]+[4]

$$\mathrm{FOM} = \frac{2^{\frac{\mathrm{SFDR_{LF}}-1.76}{6.02}} \times 2^{\frac{\mathrm{SFDR_{fs/2}}-1.76}{6.02}} \times f_\mathrm{s}}{P_\mathrm{DAC} - P_\mathrm{sig}}, \qquad (7)$$

where $SFDR_{LF}$ is the measured SFDR at a low signal frequency, $SFDR_{f_s/2}$ is the measured SFDR at the Nyquist band, f_s is the sampling rate, and P_{DAC} and P_{sig} are the power of the DAC and the output signal, respectively. A higher FOM in Eq. (7) implies higher power efficiency. The calculated FOM of these DACs are included in Table 1. The FOM of this design is 11.8×10^4 Hz/mW, while the other DACs in Table 1 give a best FOM of 7.32×10^4 Hz/mW.

5. Conclusion

A 14-bit 250-MS/s current-steering DAC in a 0.13 μm CMOS process has been presented. The power consumption is 226 mW while achieving > 77.8 dB SFDR up to the Nyquist band with a remarkable FOM. The bottleneck of the nonlinear distortions in the code-dependent switching glitches is solved by the TRI-DRRZ approach. High output impedance of the current source and switch units is achieved by compact layout implementation, and a local biasing technique is adopted to mitigate the gradient errors.

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