A 14-bit 500-MS/s DAC with digital background calibration*

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Abstract: The linearity of current-steering digital-to-analog converters (DACs) at low signal frequencies is mainly limited by matching properties of current sources, so large-size current source arrays are widely used for better matching. This, however, results in large gradient errors and parasitic capacitance, which degrade the spurious free dynamic range (SFDR) for high-frequency signals. To overcome this problem, calibration is an effective method. In this paper, a digital background calibration technique for current-steering DACs is presented and verified by a 14-bit DAC in a 0.13 μm standard CMOS process. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are 0.4 LSB and 1.2 LSB, respectively. At 500-MS/s, the SFDR is 70 dB and 50.3 dB for signals of 5.4 MHz and 224 MHz, respectively. The core area is 0.69 mm^2 and the power consumption is 165 mW from a mixed power supply with 1.2 V and 3.3 V.

Key words: digital to analog converter (DAC); current-steering; digital background calibration
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1. Introduction

Current-steering digital-to-analog converters (DACs) are widely used in high-speed and high-resolution systems, such as arbitrary waveform generators, communication transmitters and direct digital frequency synthesizers[1−3]. For a high-resolution DAC, the spurious free dynamic range (SFDR) at low frequencies is limited by current source mismatch[2]. Usage of large-size transistors and special layout techniques[4] are straightforward methods to improve the static linearity. However, these methods result in large parasitic capacitance, complex routing and signal coupling. Furthermore, the increased area leads to a higher cost.

Recently, many techniques have been published to implement high-resolution DACs without large-size current sources, such as trimming[5], dynamic element matching (DEM)[6], error mapping[7] and calibration[8−10]. Among these, calibration is the most effective method because it eliminates both random and systematic mismatch errors[11].

Calibration schemes can be classified into two categories: analog calibration and digital calibration[8]. Because of the channel-charge injection and leakage current from analog switches and the holding capacitor, digital calibration is preferred. Calibration schemes can also be classified into foreground and background calibration[11]. Compared with foreground calibration, background calibration can eliminate not only the mismatch error of the current sources induced by the nonideal manufacture process, but also the effect of environmental condition changes[12]. Therefore, digital background calibration is more suitable for present DACs.

This paper proposed a digital background calibration technique that further develops the potential of Ref. [9]. Compared with Ref. [9], the proposed technique ensures uninterrupted data processing during the calibration. The presented implementation consists of three elements: a current comparator for extracting the actual errors, a finite state machine (FSM) for implementing the sequence of operations and a calibration DAC (CALDAC) attached to each MSB for compensating the measured errors.

2. DAC architecture

The architecture of the proposed 14-bit DAC with digital background calibration is shown in Fig. 1. The 14-bit DAC is segmented into a 6-bit thermometer-decoded MSB array, a 4-bit thermometer-decoded upper LSB (ULSB) and a 4-bit binary-weighted lower LSB (LLSB). Delay is added to make the signals of the LLSB current sources synchronized with the outputs of the thermometer decoders. The differential outputs of the latches are used to control the switches in the current routes. They have mainly two functions: to synchronize all the control signals of the switches to decrease the timing difference[13] and to adjust the crossover voltage of the differential control signals to decrease the glitch energy in the current routes[14]. The MSB current source array consists of 64 unary current sources, 63 of which are used for data conversion and one for generating LSB current comprised of the ULSB and LLSB current. Only MSB current sources are calibrated because their impact on static linearity of the DAC is greater than the impact of the LSB part and 8-bit accuracy for LSB is practically achievable without calibration[11].

The calibration circuit is composed of a current comparator, a FSM, 65 CALDACs, a reference current source, an additional current source and 65 analog MUXs. One MSB current

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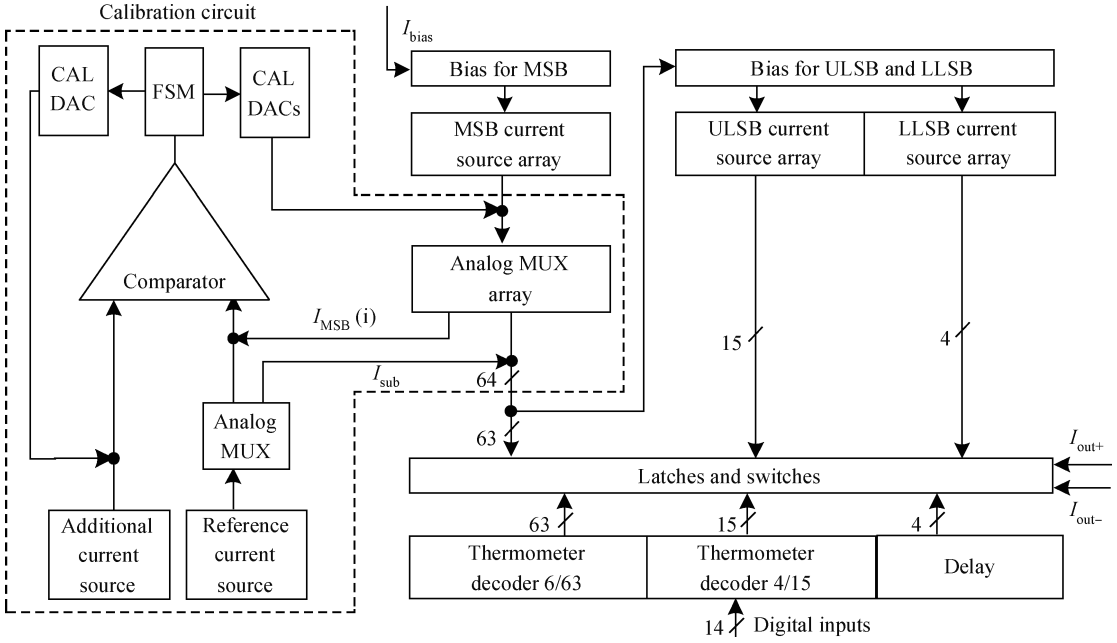

Fig. 1. The architecture of the proposed 14-bit DAC.

source is selected to be calibrated by the analog MUXs; the current calibration is carried out through the current comparator, FSM, and the CALDAC.

3. Digital background calibration

Figure 2 shows the architecture of the simplified calibration circuit. To save area, the intrinsic accuracy of the DAC is designed to be lower than its resolution. During chip usage, the calibration circuit improves the accuracy up to the specified 14-bit level. In this design, the accuracy before calibration is 11-bit, the $\sigma(I)/I$ is 0.36% for Yield = 90%[15]. Then the transistor area of a LSB current source could be obtained through the formula[2]

$$2\left[\frac{\sigma(I)}{I}\right]^2 = \frac{4A_{VT}^2}{WL(V_{GS}-V_T)^2} + \frac{A_\beta^2}{WL}, \tag{1}$$

where A_{VT} and A_β are technology parameters.

The gain of the switch transistors is important, because the output voltage results in the variation of the output delay and the output-dependent delay differences deteriorate SFDR of a high-speed high-accuracy DAC[16]. Using cascoded switches and optimizing the size of the switch transistors are good methods to increase the gain.

3.1. Calibration of the MSB array

When an MSB current source is calibrated, M2/M3/S1 are turned on and M1/M5/S2 are turned off. M4 instead of M0 participates in the data conversion to ensure uninterrupted data processing during the calibration. The actual error between I_{MSB} and I_{ADD} can be measured through the current comparator. The error is measured in the analog domain but corrected in the digital domain. The FSM regulates the input digital code of CALDAC1 according to the output of the current comparator; CALDAC1 generates an appropriate current to node X. The processing algorithm of the FSM is based on the binary search algorithm. When calibration ends, M2/M3/S1 are turned off and M1 is turned on. The required input digital code of CALDAC1 is stored in the latch. The FSM will then choose the next MSB current source for calibration.

3.2. Calibration of the reference current source

The current comparator introduces input offset current I_{off}, which is caused by the input offset voltage of the voltage comparator and the mismatch between M6 and M7. In order to eliminate I_{off}, the reference current source should be calibrated before the MSB current source array. In this step, M5 is turned on and M1/M2/M3 are turned off. The FSM regulates the input digital code of CALDAC2 and the required input digital code will be stored in the latch. I_{off} is compensated by two measurements: the reference current I_{REF} versus the additional current I_{ADD} and the reference current I_{REF} versus the calibrated MSB current I_{MSB}:

$$\begin{cases} I_{REF} \approx I_{ADD} + I_{off}, \\ I_{MSB} \approx I_{ADD} + I_{off} \approx I_{REF}. \end{cases} \tag{2}$$

3.3. The voltage comparator

Figure 3 shows the schematic of the voltage comparator[17]. It consists of a voltage-to-time converter and a binary phase detector. When CLK is high, the capacitor C will be charged to VDD through transistors M5 and M6. When CLK is low, the voltage-to-time converter generates a pulse delay difference. The binary phase detector manifests the difference in OUT. The accuracy of the voltage comparator should be more than 14-bit; it could be improved by increasing the value of C and R_D, although this would slow down the operating speed, which is not a major consideration in background calibration. The original current comparator in Ref. [18] is not employed because of the larger input offset and lower accuracy.

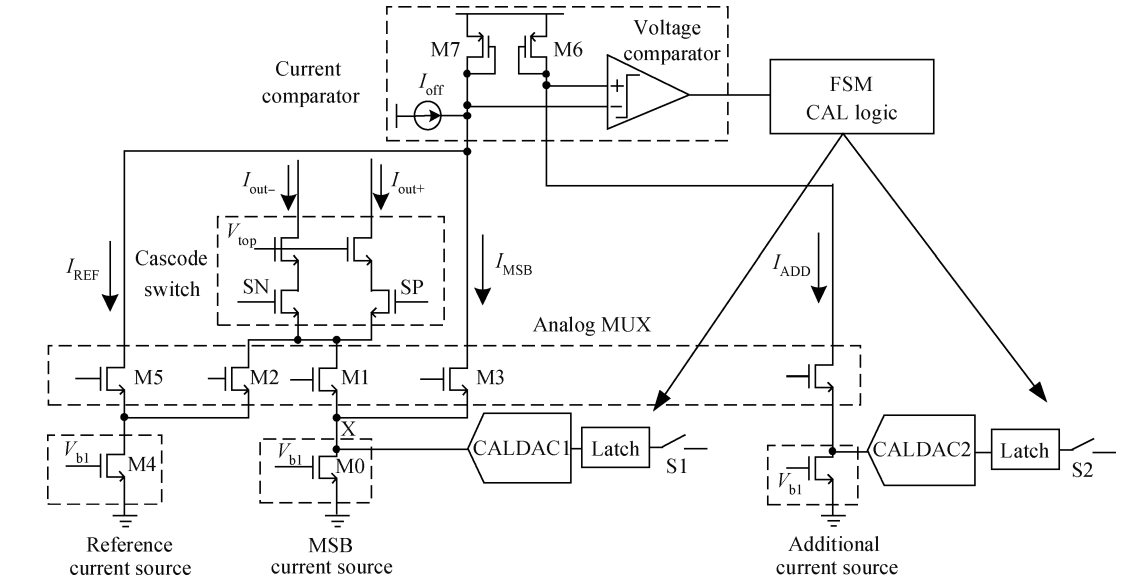

Fig. 2. Simplified calibration diagram.

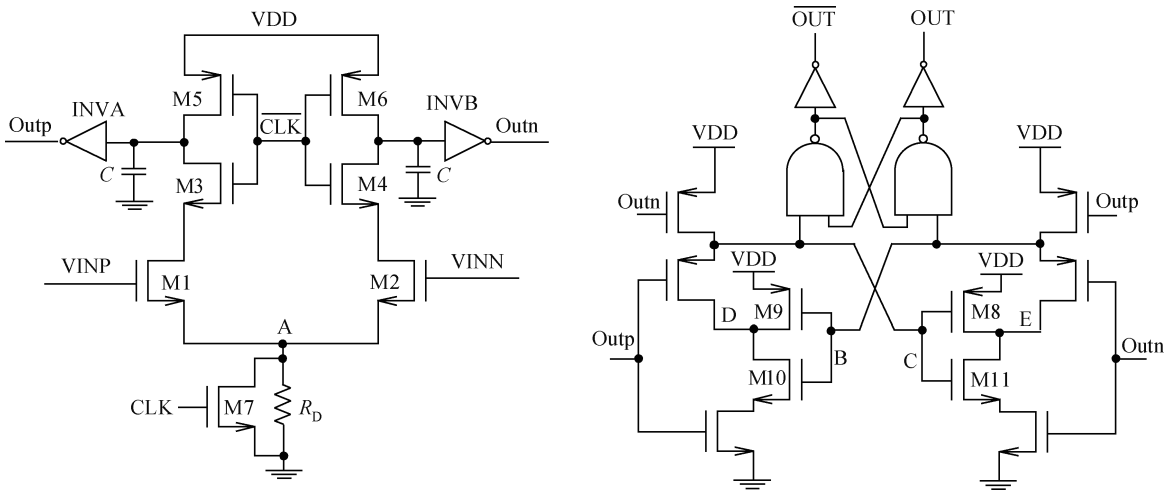

Fig. 3. Schematic of the voltage comparator[14].

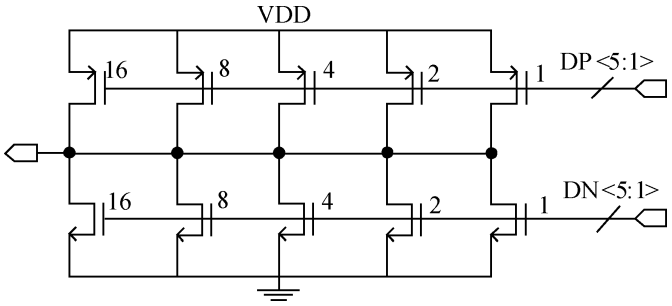

Fig. 4. Schematic of the CALDAC.

3.4. The calibration DACs (CALDACs)

The expected mismatch of the MSB current sources determines the full scale of each CALDAC and the LSB step size of the CALDAC determines the calibration accuracy. The LSB step size should be small enough to guarantee the accuracy, but this would increase the complexity of the calibration circuit. A trade-off should be made between calibration accuracy and complexity in the implementation of the CALDAC. Figure 4 shows the schematic of the CALDAC. It is capable of either sourcing or sinking currents, providing either positive or negative current to eliminate mismatch errors. The full scale is -4 LSB_{main} to $+4$ LSB_{main}, where LSB_{main} represents the LSB step size of the 14-bit DAC.

3.5. Algorithm

The background algorithm implements the sequence of operations and adjusts the compensation current. It forms a loop that is executed simultaneously along with the data conversion. A detailed FSM chart of the background algorithm is shown in Fig. 5, with P indicating the output of the current comparator, X1P/X1N the input digital code of CALDAC1 for the calibrated MSB current source and X2P/X2N the input digital code of CALDAC2.

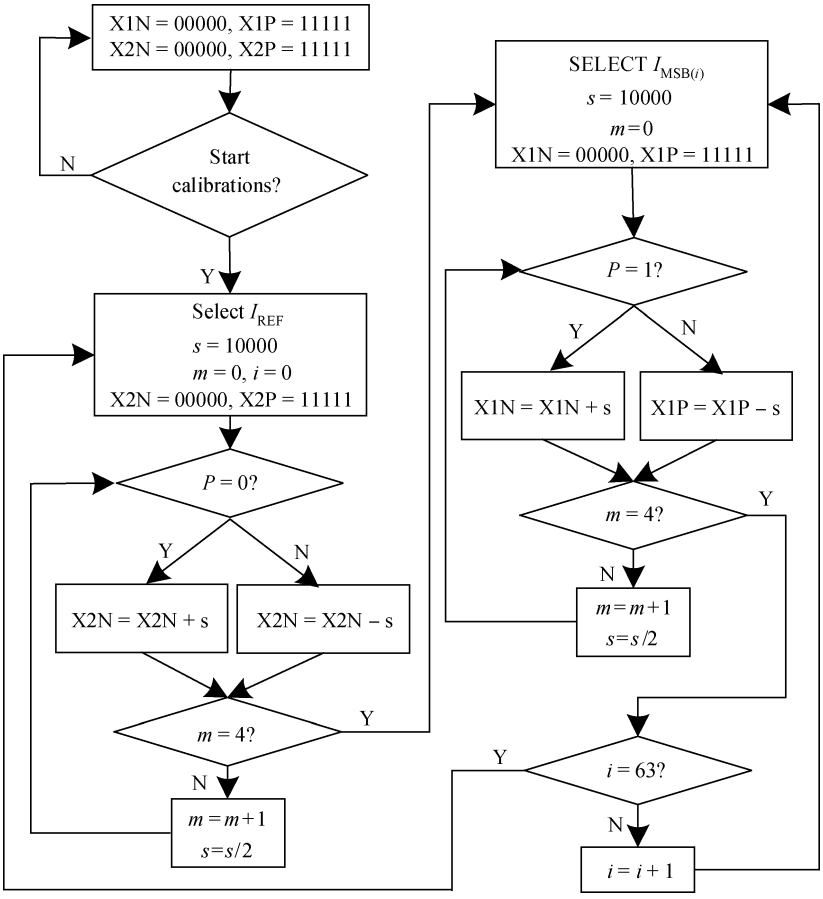

Fig. 5. FSM chart of the calibration algorithm.

4. Measurement results

The 14-bit DAC was designed in a 0.13 μm standard CMOS process and the die micrograph was presented in Fig. 6. The size of the entire chip is 2.3 × 1.3 mm^2, with a core area of 1.2 × 0.57 mm^2. This power consumption is 165 mW with a mixed power supply of 1.2 V and 3.3 V for digital and analog circuits, respectively. Figure 7 shows the static performance after calibration. The differential nonlinearity (DNL) and integral nonlinearity (INL) are 0.4 LSB and 1.2 LSB, respectively, which indicates an intrinsic accuracy of nearly 14-bit. If the DAC had been designed for 14-bit linearity based on the intrinsic matching, the area of the current source array should have increased by 8 times[17]. Reference [4] uses the Q^2 random walk switching scheme to obtain full 14-bit accuracy without any other techniques; the die area is 13.1 mm^2, which is much larger than this design. This clearly illustrates the superiority of calibration.

The dynamic measurement setup diagram is shown in Fig. 8. The differential outputs of the DAC are connected to a transformer. The output of the transformer is synthesized by a spectrum analyzer which provides a 50 Ω load to the DAC through the transformer. Figure 9 shows the output spectrum after calibration at 500-MS/s for 5.4 MHz and 224 MHz input signal frequencies. The SFDR is 70 dB and 50.3 dB, respectively. Figure 10 shows SFDR versus input signal frequency at 500-MS/s.

Table 1 compares the performance of the presented work with other calibrated DACs. This design achieves the highest sampling frequency and the smallest core area using the digital background calibration in 0.13 μm technology. Compared with Refs. [11, 19, 20], the SFDR of this design at the Nyquist frequency is the highest. Compared with Refs. [12, 19], the design occupies much smaller INL/DNL. The calculation of FOM[21], which assesses the efficiency of the DAC, is defined as:

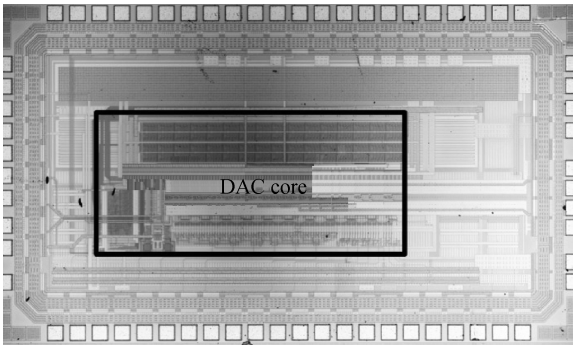

Fig. 6. Micrograph of the 14-bit DAC.

$$\mathrm{FOM} = \frac{P_{\mathrm{total}}}{10^{\mathrm{SFDR}_{f_s/2}/20} \times f_s}, \tag{3}$$

where $\mathrm{SFDR}_{f_s/2}$ is the measured SFDR at the Nyquist frequency, f_s is the sampling rate and P_{total} is the power of the DAC. The FOM of this design is 1.07 pJ/step, which is close

Table 1. Summary of experimental perfomance in comparision with other calibrated CMOS DACs.

Specification	This work	JSSC 2007[19]	ICSICT 2010[12]	ESSCIRC 2010[11]	MWSCAS 2012[20]
Calibration	Digital background	Digital background	Analog background	Digital foreground	Analog background
Process (nm)	130	180	130	180	180
Resolution (bit)	14	14	14	12	14
Sampling rate (MS/s)	500	200	100	250	200
INL/DNL (LSB)	1.2/0.4	1.4/0.8	4.3/3.1	0.5/0.5	—
Core area (mm^2)	0.69	3	1.29	0.78	1.26
Power (mW)	165	210	—	25	125
$SFDR_{LF}$ (dB)	70	78	72.8	71.7	80
$SFDR_{f_s/2}$ (dB)	50.3	43	—	43	42
FOM (pJ/step)	1.01	7.43	—	0.71	4.96

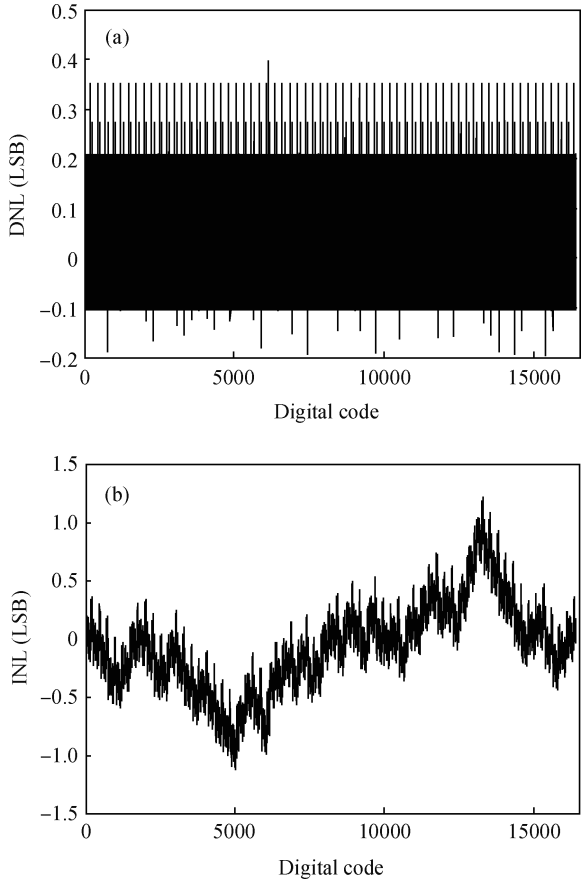

Fig. 7. Static performance after calibration. (a) DNL. (b) INL.

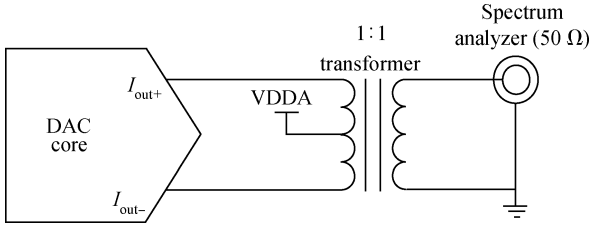

Fig. 8. Dynamic measurement setup diagram.

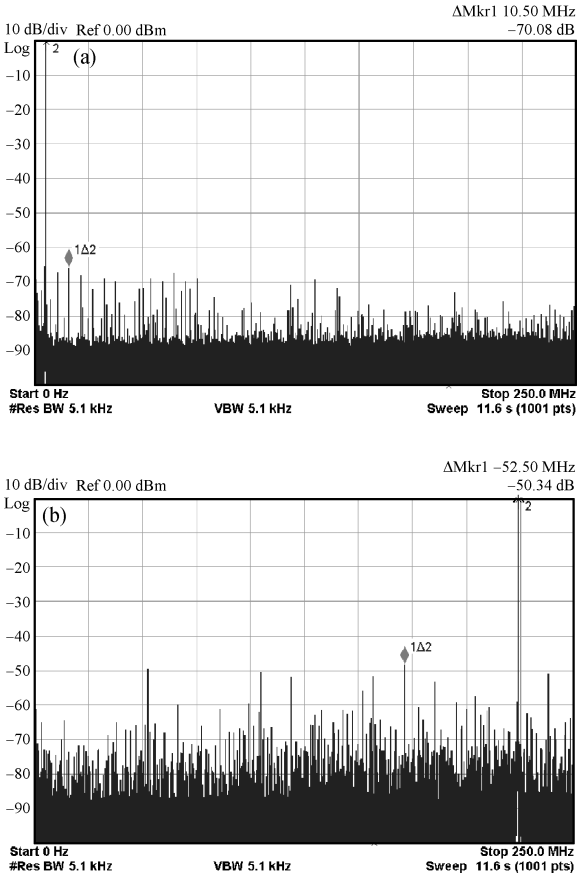

Fig. 9. The measured SFDR at 500-MS/s (a) 5.4 MHz and (b) 224 MHz input signal frequencies.

to Ref. [11] and much lower than Refs. [19, 20].

5. Conclusion

A 14-bit 500-MS/s DAC with digital background calibration is implemented in a 0.13 μm standard CMOS process. The proposed digital background calibration technique reduces the parasitic capacitance and gradient errors associated with small core area while guaranteeing the matching performance. The optimized architecture of the DAC ensures uninterrupted data processing during the calibration. Adopting the modified digital background calibration technique, this proposed DAC

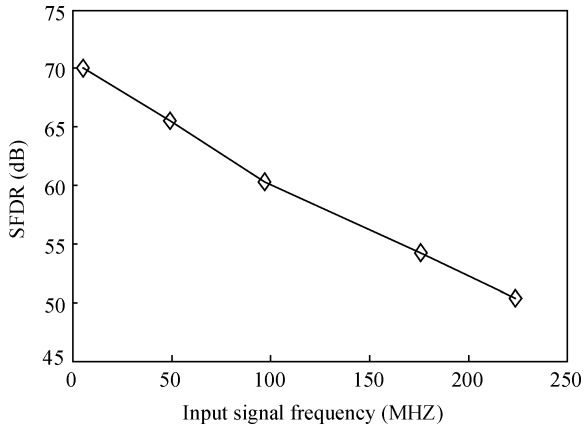

Fig. 10. Measured SFDR versus input signal frequency at 500 MS/s.

achieves 70 dB and 50.3 dB SFDR for signals of 5.4 MHz and 224 MHz, respectively. The DNL/INL are 0.4/1.2 LSB and the core area is only 0.69 mm^2.

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References

[1] Huang Q, Francese P A, Martelli C, et al. A 200 MS/s 14 b 97 mW DAC in 0.18 μm CMOS. IEEE ISSCC Dig Tech Papers, 2004: 364

[2] Pelgrom M, Duinmaijer A, Welbers A. Matching properties of MOS transistors. IEEE J Solid-State Circuits, 1989, 24(5): 1433

[3] Tseng W H, Fan C W, Wu J T. A 12-bit 1.25-GS/s DAC in 90 nm CMOS with > 70 dB SFDR up to 500 MHz. IEEE J Solid-State Circuits, 2011, 46(12): 2845

[4] Vander Plas G A M, Vandenbussche J, Sansen W, et al. A 14-bit intrinsic accuracy Q^2 random walk CMOS DAC. IEEE J Solid-State Circuits, 1999, 34(12): 1708

[5] Bugeja A, Song B S. A self-trimming 14-b 100-MS/s CMOS DAC. IEEE J Solid-State Circuits, 2000, 35(12): 1841

[6] Chan K L, Zhu J, Galton I. Dynamic element matching to prevent nonlinear distortion from pulse-shape mismatches in high-resolution DACs. IEEE J Solid-State Circuits, 2008, 43(9): 2607

[7] Doris K, Lin C, Domine L, et al. D/A conversion: amplitude and time error mapping optimization. Proc IEEE ICECS, 2001: 863

[8] Yusuke I, Akira M. Digital calibration method for binary-weighted current-steering D/A-converters without calibration ADC. IEICE Trans, 2007, 90(6): 1172

[9] Radulov G I, Quinn P J, Hegt H, et al. An on-chip self-calibration method for current mismatch in D/A converters. Proc IEEE ESSCIRC, 2005: 169

[10] Chi J H, Chu S H, Tsai T H. A 1.8-V 12-bit 250-MS/s 25-mW self-calibrated DAC. Proc IEEE ESSCIRC, 2010: 222

[11] Radulov G. Flexible and self-calibrating current-steering digital-to-analog converters: analysis, classification and design. PhD Thesis, Eindhoven University of Technology, 2010

[12] Qiu D, Fang S, Xie R, et al. A 14-bit 100 MS/s self-calibrated DAC with a randomized calibration-period. IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2010: 312

[13] Chen T, Gielen G G E. The analysis and improvement of a current-steering DACs dynamic SFDR-I: the cell-dependent delay differences. IEEE Trans Circuits Syst I, 2006, 53(1): 3

[14] Schafferer B, Adams R. A 3 V CMOS 400 mW 14 b 1.4 GS/s DAC for multi-carrier applications. IEEE ISSCC Dig Tech Papers, 2004: 360

[15] Van den Bosch A, Steyaert M, Sansen W. An accurate statistical yield model for CMOS current-steering D/A converters. IEEE Int Symp Circuits and Systems (ISCAS), 2000: IV.105

[16] Chen T, Gielen G. The analysis and improvement of a current-steering DAC's dynamic SFDR—II: the output-dependent delay differences. IEEE Trans Circuits Syst I, 2007, 54(2): 268

[17] Fan H, Han X, Wei Q, et al. A 12-bit self-calibrating SAR ADC achieving a Nyquist 90.4-dB SFDR. Analog Integrated Circuits and Signal Processing, 2013, 74(1): 239

[18] Traff H. Novel approach to high speed CMOS current comparators. Electron Lett, 1992, 28(3): 310

[19] Chen T, Georges G E. A 14-bit 200-MHz current-steering DAC with switching-sequence post-adjustment calibration. IEEE J Solid-State Circuits, 2007, 42(11): 2386

[20] Cheng L, Chen C X, Ye F, et al. A digitally calibrated current-steering DAC with current-splitting array. IEEE International Midwest Symposium on Circuits and Systems, 2012: 278

[21] Ali A M A, Dillon C, Sneed R, et al. A 14-bit 125 MS/s IF/RF sampling pipelined ADC with 100 dB SFDR and 50 fs jitter. IEEE J Solid-State Circuits, 2006, 41(8): 1846