NCFET Based Logic for Energy Harvesting Systems

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Abstract—**Negative Capacitance FETs (NCFETs) are emerging devices that could be utilized for designing power-efficient nonvolatile energy harvesting processors. The unique feature which makes these devices suitable for ultra-low power operation is the steep slope achieved by negative capacitance of the ferroelectric oxide based gate stack. This property is being actively explored to overcome the fundamental 60 mV/decade subthreshold swing limit in conventional MOSFET. NCFETs also show a hysteresis I_{ds}-V_{gs} behavior, with which we propose to build nonvolatile circuits and noise immune logic. However, because large hysteresis may prevent further V_{DD} scaling for NCFET based digital circuits, we analyze the circuit implementations and explore novel device and circuit techniques, to overcome the limitations and utilize the unique properties of the NCFETs for low-power nonvolatile noise immune systems.**

Keywords—**NCFET, hysteresis, steep-slope devices, low power, tunability, nonvolatile processor, negative capacitance**

1. Introduction and Motivation

Design of energy harvesting systems is becoming critical with the increase in demand for applications like Internet of things, wearable health monitoring devices, and portable video gadgets, etc [1-3]. These are battery-less systems powered by ambient energy resources like solar, RF, Piezo and thermal sources. A high-level overview of such a self-powered system is given in Fig. 1 [2][3]. The heart of such a system is a low-power nonvolatile processor (NVP). One important aspect of NVP is that it should be capable of performing computations using limited amount of energy. Also, non-volatility is essential for NVP to achieve more forward progress (FP) by maintaining the computation states efficiently during power failures which otherwise require checkpointing or roll-back techniques at additional power and performance costs [2].In addition, energy harvesting systems face noisy interference at both the signal interconnections and the voltage supply. Such systems will benefit from circuits with noise immunity. Therefore, design exploration of low-power nonvolatile processors with noise immunity is of great significance in dimensions of device, circuit, and architecture.

Negative capacitance FETs (NCFETs), as one emerging device, is one promising candidate with unique characteristics to overcome these challenges. As reported in [4], NCFETs are steep-slope devices with subthreshold swing (SS) lower than the CMOS limit of 60 mV/decade. They may also exhibit tunable hysteretic behavior in their I_{ds}–V_{gs} characteristics which leads to non-volatility and noise immunity. As will be discussed in detail in this paper, we will show the exploration of design techniques that could transform these NCFET features into a power-efficient NVP with noise immunity.

2. Low-Power Nonvolatile Processor with Noise Immunity

Stand-alone logic and memory are two main constituting building blocks of a conventional processor and need

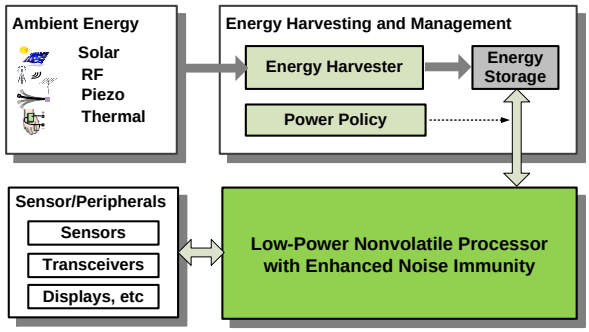


Fig. 1. Overview of an energy harvesting system.

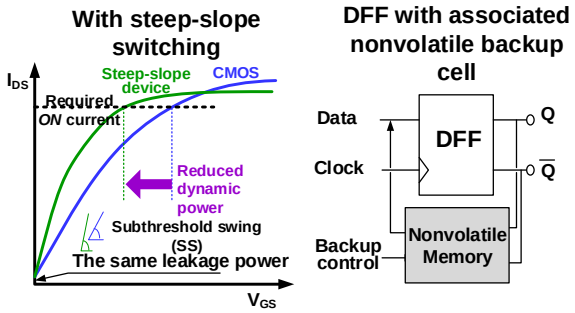


Fig. 2. Steep slope and nonvolatility.

optimization to build an power-efficient system. This can be done in a heterogeneous manner by independently optimizing the logic or memory by considering these as separate functional blocks, for example, using hybrid CMOS-STTRAM combinations with each optimized[6]. One innovative approach will be unifying the memory logic functionalities in the same block. This could be possible if we could use the same device structure to build both functions. In our work, we focus on improving the overall system design by focusing on NCFET feature like steep slope and non-volatility. Also we explore the possibility of merging the logic and memory functionalities by utilizing the unique NCFET features.

Supply voltage reduction is a key component in Dennard scaling of semiconductor devices to reduce the power density. However, one issue with further reducing the supply voltage is the challenge to suppress the OFF-state leakage current while achieving a sufficiently high ON-state current with a low-voltage supply. This forces the need to have steep-slope devices which have a low Subthreshold. Fig. 2 shows how a steep-slope device can outperform a conventional CMOS device in terms of power savings. With the same leakage current, steep-slope devices provide higher ON-state current at a lower voltage. NCFETs are one such steep-slope device that enables the processor to operate at a low voltage leading to lower power.

With regard to the non-volatility for an energy harvesting processor, Fig. 2 shows a method to incorporate non-volatility

into the flip-flop. If we could devise a technique to maintain the polarization of the Ferroelectric layer in an NCFET in the absence of gate voltage, it will be possible to realize a nonvolatile flip-flop (NVFF).

While noise is another issue that needs to be tackled in energy harvesting systems, we argue that the hysteresis tuning in the NCFETs could improve the noise margin on both logic and SRAMs built with NCFETs, though it has been traditionally viewed as an undesired feature. Also, the possibility of dynamically tuning the hysteresis to the zero-gate-voltage region will pay way to novel memory-logic interchangeable circuits for energy harvesting processors. However, large hysteretic characteristics may prevent V_{DD} scaling for NCFET digital circuits. Hence, it is of extreme importance to understand such hysteresis. In the rest of the paper we discuss our analysis and findings on the NCFET characteristics and methods of tweaking those to suit implementation of low-power nonvolatile processor tackling issues and possibilities discussed above.

3. NCFETS:Background

NCFETs are implemented by adding a ferroelectric material layer in the gate stack of MOSFETs. The schematic is given in Fig. 3(a). A lower SS is achieved in NCFETs with the help of "negative capacitance" which is contributed by the deposited ferroelectric layer. Ferroelectrics are materials with a high polarizability. Ferroelectric capacitors tend to exhibit nonlinear capacitance, where the change in voltage produces a negative change in polarizability. The free energy of ferroelectric is represented by the Laundu Theory[9][10] as

$$Fp = \frac{1}{2}\alpha P^2 + \frac{1}{4}\beta P^4 + \frac{1}{6}\gamma P^6 - E \cdot P, \quad (1)$$

where P is the polarization, E is the electric field, Fp is the free energy of ferroelectrics, α, β, γ are coefficients [5][7][10]. For a system to be at equilibrium where the energy state is minimized dFp/dE should be zero, there for E can be written as

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5. \quad (2)$$

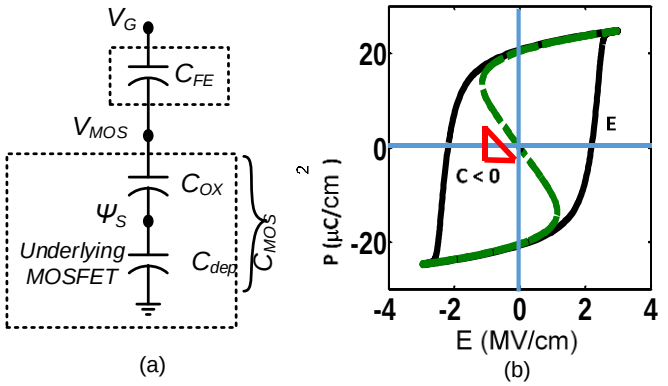


Fig. 3. NCFET capacitance model from [5] (b) in (a) P-E loop in (b).

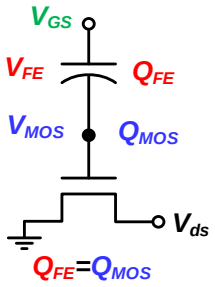
Fig. 3 shows the NCFET capacitance model. It can be seen from the Fig. 3(b) that there is a portion in the P-E curve where the change in polarization with respect to the electric field is negative. Non-volatility comes from the fact the polarization direction is retained even if we remove the electric field.

4. NCFET Modeling

For simulation purpose, we use the HSPICE model shown in Fig. 4. A ferroelectric capacitor is placed in series with a MOSFET to emulate the NCFET structure. The 45 nm PTM model is used for MOSFET simulations. Because the ferroelectric capacitor and MOSFET are in series, they have the same charge all the time, and the interconnecting equation can be written as

$$V_{gs}(Q) = V_{FE}(Q) + V_{MOS}(Q), \quad (3)$$

where $V_{gs}(Q)$, $V_{FE}(Q)$, $V_{MOS}(Q)$ represent the gate to source voltage of the NCFET,Voltage across Ferro layer and voltage to the MOSFET respectively. Using (3), our model consistently solves Landau Khalatnikov (LK) equations[10] along with MOSFET model. Simulation parameters are given in the Table I. We have done extensive DC simulations to study the NCFETs characteristics to devise new design schemes that could realize an efficient nonvolatile processor. With the device parameters tuning, NCFETs can operate in either hysteresis or non-hysteresis mode. More details are discussed in the following section.



parameters	value
α	-4.24e8
β	2.3e8
γ	3.8e10
Width	1u
Lg	45n
eox_par	3.9
toxp_par	1e-9

(b)

Fig. 4. NCFET model schematic in (a) and model parameters in (b).

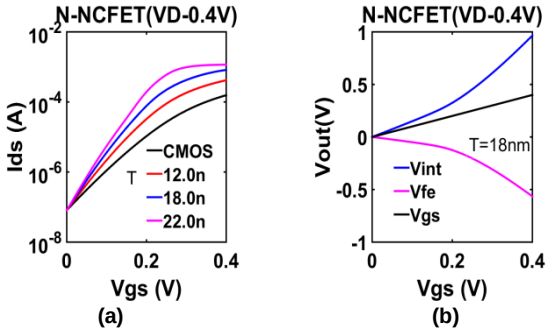


Fig. 5. I_{ds}–V_{gs} characteristics of N-type NCFETs showing steep-slope behavior with different ferroelectric layer thickness (T) in (a). Intermediate voltages for 18nm ferroelectric layer thickness in (b).

5. NCFET Simulations

We have done our study on NCFET characteristics using simulation and our discussion on analysis and findings are presented in the following sections based on the nature of hysteresis characteristics and the circuit under simulation.

5.1. Steep-Slope(Non-Hysteresis) Mode

The steep-slope mode of operation of NCFET is shown in Fig. 5. For the same V_{gs}, NCFET generates higher I_{ds} compared to a CMOS transistor. The increase in I_{ds} in the subthreshold

region comes from the fact that the negative voltage drop across the ferroelectric layer V_{FE} which causes an increased gate voltage in the V_{MOS}. The intermediate voltage at V_{MOS} is greater than the applied input voltage V_{gs} because V_{FE} and V_{MOS} are of opposite polarities. V_{FE} gets negative polarity due to the negative capacitance of the ferroelectric layer in the gate stack. This acts as a voltage boost to get higher gain in drain current. This is illustrated in Fig. 5(b) for an NCFET with an 18 nm ferroelectric layer. It can be seen that the intermediate voltage V_{int} which goes to the MOSFET input is higher than actual applied input voltage V_{gs}. Also we could observe from the figure that with an increase in the ferroelectric layer, *SS* deceases. As the ferroelectric layer thickness increases, C_{FE} decreases, resulting more negative voltage drop across the ferroelectric layer and thus increases the positive V_{MOS} and I_{ds}.

5.2. Hysteresis Mode

Further increasing the thickness of the ferroelectric layer, NCFET tend to exhibit hysteresis shown in Fig. 6. Taking NCFET with 25.5 nm ferroelectric layer thickness as an example, the I_{ds}–V_{gs} characteristics is shown in Fig.7. Hysteresis loop in I_{ds}–V_{gs} results from the interplay of negative ferroelectric capacitance and the positive MOSFET capacitance. Since that the ferroelectric layer capacitor is in series with MOSFET capacitor, they maintain same charge *Q*, and the total capacitance of the system, C_{total}, can be written as

$$\frac{1}{C_{total}} = \frac{1}{C_{FE}} + \frac{1}{C_{MOS}}, \tag{4}$$

where CFE and CMOS represent the Ferro layer capacitance and the MOSFET capacitance , respectively.

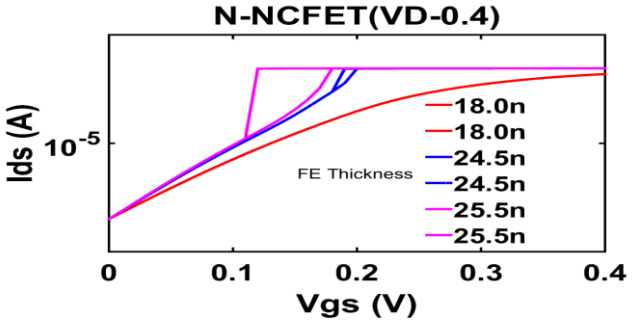


Fig. 6. I_{ds}–V_{gs} characteristics of N-type NCFETs with hysteresis.

It is noted that both CMOS capacitance and ferroelectric layer capacitance are nonlinear. The capacitance of the stand-alone ferroelectric can be obtained from the P-E curve shown in Fig. 3(b). From (4),We can infer that if the magnitude of positive MOS capacitance becomes larger than the magnitude of the negative ferroelectric capacitance, the system becomes unstable [5] as C_{FE} is negative. In order to avoid this situation, hysteretic jump in *Q* and thus in I_{ds} occurs and hence maintaining the magnitude of the positive MOS capacitance less than the ferroelectric capacitance. The onset of hysteresis where the *Q* jump occurs is denoted as point *A* in Fig. 7. In the reverse sweep, the magnitude of the negative ferroelectric capacitance and MOS capacitance become equal , then *Q* and I_{ds} take deviation to maintain the system stability. This is point *B* in Fig 7. With change in the thickness of the ferroelectric layer, the ferroelectric capacitance changes. As a result, the onset of hysteresis (A in Fig 7)(where the magnitude of ferroelectric layer capacitance equals the magnitude of MOS capacitance) changes and hence we get a different hysteresis loop with varying device parameters.

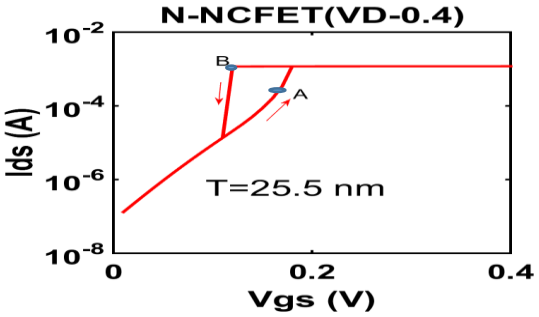


Fig. 7. Ids–Vgs of NCFET when Ferro layer thickness is 25.5 nm

5.3. Non volatility and Hysteresis

One promising ferroelectric device feature is their capability to remember its polarization state in the absence of power. In NCFETs, it is possible to observe the hysteresis around the zero gate voltage by choosing proper device parameters as shown in Fig. 8(b). We could shift the hysteresis around the origin by appropriately varying the thickness and keeping all other parameters the same. As shown by *A* and *B* in Fig. 8(b), it is possible to have a high or low resistance state when V_{gs} is zero. The location of either *A* or *B* in the hysteresis loop center is determined by the input V_{gs} sweeping direction. Such characteristics could be further converted into non-volatility as it has the potential to remember a logic high or logic low in the form of high or low resistance.

In Fig. 8(a), we propose a method to implement nonvolatile flip-flop by making use of the non-volatility of the NCFET. It can be deduced that depending on the position of the hysteresis, NCFET can be either used to implement a memory device or a pure logic device. We have shown above that the hysteresis can be tuned statically by changing the device parameters like the ferroelectric layer thickness. We also have looked into the possibility of dynamically tuning the hysteresis as it can open up the exciting possibility of realizing a memory-in-logic device.

We have also investigated the possibility of dynamically tuning the hysteresis by varying the supply voltage and body bias voltage, as discussed in the next section.

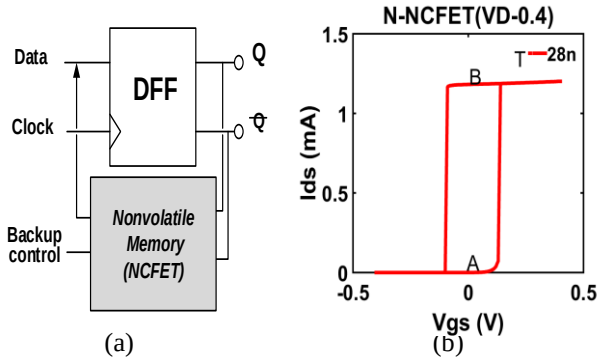


Fig. 8. NCFET nonvolatile flip-flop in (a) and I_{ds}–V_{gs} curve in (b).

5.4. Hysteresis Dynamic Tuning

In order to dynamically tune the hysteresis loop we explored the dependence of the hysteresis loop on the drain voltage and body biasing. Fig. 9(a) demonstrates the effect of a change in the drain voltage V_d. With a higher drain voltage, the hysteresis loop moves towards the region with a higher V_{gs}.

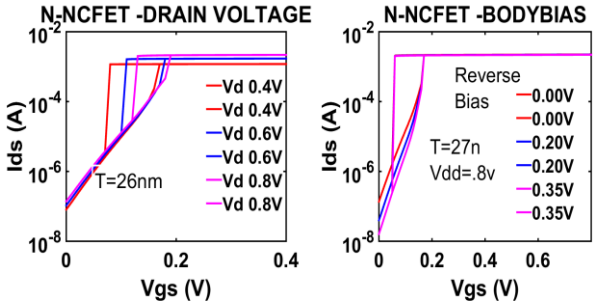


Fig. 9. I_d–V_{gs} of NCFET with various drain voltage V_d; in (a) I_d–V_{gs} of NCFET with various body biasing voltage in (b).

The mechanism behind the hysteresis tuning through the drain voltage is that the drain voltage has an impact on the Q of the channel and the capacitance of the MOSFET [5] which will change the MOSFET capacitance C_{MOS}, leading to different matching points and hysteresis shapes.

Another option that we explored for dynamic tuning is to make use of the substrate terminal of the transistor which is normally used for body biasing. In this case, body biasing is used to tune the threshold voltage and hence the capacitance of the device by changing the source to substrate potential. Application of a lower voltage to the body terminal with respect to the substrate could reduce the charge in the inversion layer. With reverse body bias, though the total charge of the channel and body remains constant, it causes the charge of the body to increase and charge of the channel decrease. Fig. 9(b) shows the effect of the reverse body bias on the hysteresis. Though in our experiments we observe a small change in hysteresis with body bias, making use of a fourth terminal to control the device characteristics could be an effective option, which needs to be studied in detail.

5.5. Inverter

In order to understand how to use NCFET to design circuits, we introduce an NCFET inverter as an example. As we mentioned in the previous section, changing the device parameters affects the NCFET behavior. For the NCFET inverter, Fig. 10(a) shows the input-output voltage transfer curve. It is observed that compared to the CMOS inverter, the NCFET inverter has a sharp state transition which is beneficial for digital circuits to improve the input output signal range.

The NCFET inverter characteristics also can be drastically changed by varying the device parameters. For example, changing the device ferroelectric layer thickness results in an inverter with hysteresis as shown in Fig. 10 (b). Hysteresis has been viewed as a problem with traditional circuits; However, we argue that such hysteresis could be used to make an inverter with better noise immunity. It is evident from Fig. 10(b) that a higher input voltage is required to turn on or turn off the inverter. Namely, noise added to the input within the hysteresis loop band border will not corrupt the output validity. Fig. 10(b) also shows the extended noise margin compared with CMOS inverter. Wider hysteresis yields more noise margin, yet also more delay due to late turning on/off. A trade-off should thus be made to optimize the circuit design based on the application requirement.

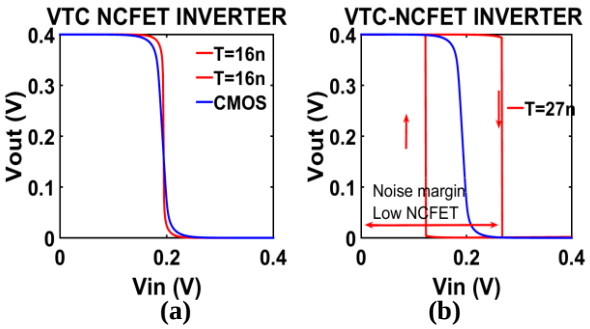


Fig. 10. NCFET inverter w/t and w/o hysteresis in (a) and (b), respectively.

6. Conclusions

NCFETs are inherently steep-slope devices which translate to low-power digital logic operation. In this paper, we have explored that NCFETs operation with tunable hysteresis as well as steep-slope mode. We have shown how to tune the hysteresis by changing the device parameters. The hysteresis observed at zero gate voltage is proposed as an intrinsic non-volatility feature to build nonvolatile flip-flop and memory cells. We also propose using NCFET hysteresis to build better noise immune circuits. These unique features imply that NCFETs are promising for energy harvesting applications in building low-power nonvolatile processors with better noise immunity on homogenous device platform. Future work on the NCFET device fabrication is of significance.

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