Enabling Internet-of-Things with Opportunities Brought by Emerging Devices, Circuits and Architectures

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Abstract. In recent years, the concept of Internet-of-Things (IoT) has attracted significant interests. Required by the applications, the IoT power optimization has become the key concern, which relies on innovations from all levels of device, circuits, and architectures. Meanwhile, the energy efficiency of existing IoT implementations based on the CMOS technology is fundamentally limited by the device physics and also the circuits and systems built on it. This chapter focuses on a different dimension, exploring how emerging beyond-CMOS devices, such as tunnel field effect transistor (TFET) and negative capacitance FET (NCFET), and the circuits and architectures built upon them, could extend the low-power design space to enable IoT applications with beyond-CMOS features.

Keywords: Internet-of-things · Emerging devices · Tunnel FET · Negative capacitance FET · Energy harvesting · Nonvolatile memory · Nonvolatile computing

1 Introduction

Improved sensing, signal processing, and communication has significantly changed the connection between humans and the world with the rise of intelligent devices being developed for the Internet-of-things (IoT) [1]. As designers seek to make these IoT systems smarter and more ubiquitous, high energy-efficiency has been the key to enhance both connectivity and IoT signal processing functionality. Cross-layer efforts in improving solid-state devices, and the circuits and systems built upon them, are the key to achieve the high energy efficiency demanded by an expanding future of IoT tasks.

Concurrently, the needs for portability and mobility, common in IoT applications, have driven devices toward battery and/or ambient energy harvesting power solutions [2]. In the past few decades, the power consumption of integrated circuits has been lowered significantly through the scaling of the CMOS technology together with signal processing techniques. Such achievement has made more and more IoT applications feasible while being powered with a modest battery capacity or ambient energy

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harvester (e.g. a solar cell). However, further power reduction has become more and more challenging for conventional CMOS technology (including FinFET innovations) and the computation and communication methodologies built upon it. The conventional means of power reduction alongside CMOS scaling of using a lower supply voltage to reduce the dynamic power consumption while simultaneously reducing threshold voltages to provide sufficient computing speed causes exponentially increasing leakage power, which can now approach magnitudes similar to dynamic power. This fundamentally limits the expansion of functionality via CMOS scaling alone, especially when IoT devices are powered by batteries or harvested energy.

Battery-less IoT systems face further challenges in obtaining sufficient energy from the low and intermittent power source in the ambient environment [3]. Existing energy-harvesting circuits may encounter a low-input voltage that leads to a low power-conversion efficiency. Low harvested power not only limits the average amount of tasks being performed, but also increases the response latency, which is a key factor of quality-of-service (QoS). Meanwhile, distinct from conventional computing systems with a stable supply, the intermittency of harvested power also requires additional backup and restore operations, which consumes extra energy and time and carries the risk of losing computation progress if a backup operation is not carried out in time.

While these fundamental challenges have become a barrier when using CMOS technology, the advent of emerging technologies have brought new opportunities. These emerging technologies include emerging transistor devices, circuits, and architectures. The new opportunities can be seen, broadly, as advances in two key directions. Firstly, the Boolean switching behavior of some emerging transistors can replace the existing CMOS transistors in conventional computing approaches with substantially improved prospects for power scaling and low-voltage operation [4]. Secondly, certain emerging devices inherently support nonvolatile data storage and computing, enabling low-energy memory access and backup/restore operations.

There have been quite a few promising beyond-CMOS emerging devices, such as single-electron devices [5], spin-transfer-torque devices [6], the tunnel field effect transistor (TFET) [7], negative capacitance FET (NCFET, aka ferroelectric FET or FeFET) [8]. This chapter introduces two types of them, including TFET and NCFET. As promising beyond-CMOS candidates, these devices could work at a lower supply voltage to enable further power reduction in Boolean computation (without higher static leakage than CMOS). Meanwhile, the substantially novel features that they exhibit could also be captured to enable new computing architectures supporting nonvolatile data storage and computing.

The remainder of this chapter proceeds as follows. Section 2 investigates the challenges in designing energy-efficient IoT systems. Section 3 introduces the three types of emerging technologies, with more emphasis on their electrical characteristics. Section 4 describes how to make use of these emerging devices to design more energy-efficient IoT systems beyond those in CMOS. Section 5 discusses future research directions and Section 6 discusses key conclusions.

2 IoT Systems and Efficiency Bottlenecks

This section presents a model of a general IoT system, describes the functionality of each block, and analyzes the bottlenecks in each block considering existing optimization efforts.

2.1 A General IoT System

While there has been a relatively long history of using solar cells to power devices, recently published battery-less IoT system designs have been demonstrated with an increasingly wide range of power sources. Devices powered by harvested radio-frequency (RF) energy have been shown to be successful for applications including a glucose level sensor on a contact lens, a highway RFID pass, bio-signal sensors on animals or insects, etc. [2]. Their system functionality varies from a simpler signal recorder to a more complex in situ signal processor, such as one with EEG signal processing, and wireless transmission. The system feature size, operating range, performed tasks, circuit design and architecture implementation, should be optimized based on the amount of obtainable energy and other quality-of-service (QoS) requirements in the applications.

The system structure varies with the specific application requirements. A general battery-less IoT system could be built as shown in Fig. 1 using ambient-energy-harvesting techniques [2, 9]. While some blocks, such as sensors and interface, memory storage, and a digital signal processor and accelerators, can be similar to conventional designs with a stable power supply, there are extra and significantly different blocks when the system is battery-less and powered by ambient energy-harvesting techniques.

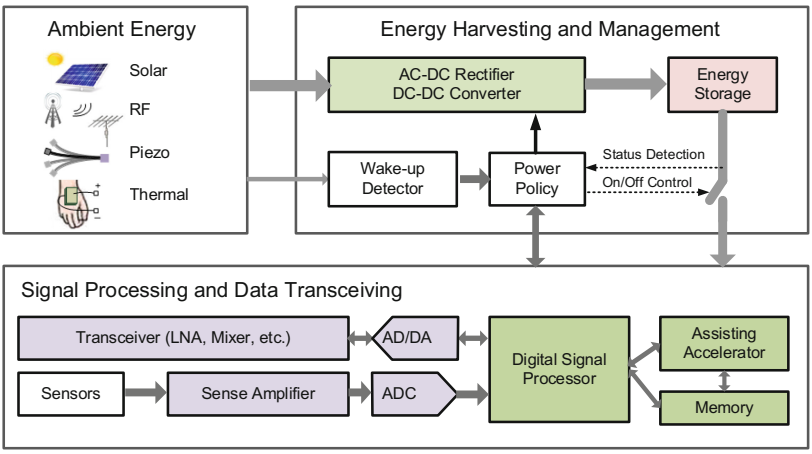

Fig. 1. A general battery-less IoT system powered by ambient-energy harvesting [9]

In addition to the external power sources, the energy-harvesting IoT system consists of two major blocks: the block of energy harvesting and management, and the block of signal processing and data transceiving. The energy harvester differs with the ambient energy source, and a wake-up receiver may be used in scenarios when an external triggering signal is used to switch the system between different power or operation modes. A temporary energy storage medium in the form of a capacitor is usually used to smooth the supply glitch and cover a temporary power income loss. As will be further discussed later, the power supply and management module, and the digital signal processing architecture for an energy-harvesting IoT system can be significantly different from conventional designs with a stable power supply. In fact, the overall system performance greatly relies on how these different blocks are built. The next sub-section (Sect. 2.2) will discuss more details of each block.

2.2 Bottlenecks and Existing Efforts

Energy sources and energy harvesting techniques. Solar, RF, piezoelectric and thermal gradients have been widely used ambient energy sources [23]. When the energy source does not directly provide the required DC voltage output, voltage converters and regulators are needed. For example, a rectifier is required to convert AC signals from an RF signal antenna and piezoelectric films. DC-DC converters can be used to convert the DC supply voltage to be higher or lower. Despite of the differences between these ambient power sources, there are three major challenges in energy harvesting and storage. The first challenge is the relatively low and varying energy density, intermittency, dependency of the efficiency on the load condition, and the unpredictability of these factors. Therefore, circuit optimizations such as tracking and adaptive operations [10] are usually required to mitigate these effects which significantly increases the design complexity. The second challenge is the low power-conversion efficiency (PCE) because of the weak power from the ambient environment. Such a weak power results in low-voltage operation and thus a high resistive energy loss with conventional CMOS technology [11, 12]. The third challenge is the leakage of the energy storage capacitors, which makes the approach of "short-time-computing, long-time-harvesting" less applicable in ultra-low input power scenarios.

Sensing, interface, and communication. While this can be similar to IoT systems with a stable supply, the increasing amount of data being transferred by the IoT devices, the relatively much lower energy budget, and the unpredictable power outages make the interface challenging. There is not yet a mature protocol to deal with frequent supply failures in IoT. Some techniques, such as passive communications (e.g. backscatter in [16]), are useful to reduce the power, but limited in the operation range, speed, and overall energy-efficiency when considering the power transmitter.

Digital signal processing. There are two main challenges in the design of digital signal processors. The first challenge, as introduced in Sect. 1, is that the slowing down of voltage scaling has become challenging because of increased leakage power. The question of how to build reliable and energy-efficient digital processing circuits under a

lower voltage has become a hot topic in device, circuit, and architecture research. The second challenge, which is a result caused by intermittent supply failure, is that the frequent backup-restore operations consume significant amounts of energy, limiting the overall forward computing progress. There has been some initial research on the optimization of nonvolatile processors (NVPs) recently, as will be discussed later, showing great potential to mitigate the impact of power intermittency [13–15]. Nevertheless, the study of signal processing algorithms, computing architectures for IoT systems is still insufficient for digital signal processing under an intermittent power supply.

Data storage. For IoT systems, especially in sensing applications, memory elements are needed to store data before they are processed and transferred. Future IoT data storage will be using more memory as the task complexity increases. While the required data storage volume varies with the application, the major challenge in data storage for energy-harvesting IoT systems is the energy efficiency in read and write access due to a low energy budget. This challenge is particularly critical for on-chip nonvolatile memory (NVM) designs, as recent research has revealed the advantage of integrated on-chip NVM to reduce access energy and delay [13–15, 17, 18]. It is likely that the co-design of data storage and signal processing architecture will be critical for overall energy efficiency, especially for some applications where memory access is the bottleneck due to frequent backup and restore operations [19].

Other issues. Other challenges, such as security and privacy [20], reliability, yield, etc., which are not covered by this chapter, will also be critical in future IoT systems.

3 Emerging Beyond-CMOS Devices

In this section, TFET and NCFET, as emerging beyond-CMOS devices, will be introduced and compared with conventional CMOS. At the device level, there are a few widely-used performance metrics to evaluate a device:

ON-state current (I_{ON}): drain current when the transistor is in the *ON* state. I_{ON} is usually measured with both the gate-source voltage (V_{GS}) and the drain-source voltage (V_{DS}) set to be equal to the supply voltage. A higher I_{ON} is equivalent to smaller on-state resistance, and is thus preferred for higher speed.

OFF-state current (I_{OFF}): drain current when the transistor is in the *OFF* state. I_{OFF} is usually measured with V_{GS} equal to zero and V_{DS} equal to the supply voltage. A lower I_{OFF} indicates larger off-state resistance, and is preferred for lower leakage current.

Subthreshold swing (SS): the required voltage change at the transistor gate to change the drain-source current by a decade in the subthreshold region. In conventional CMOS FETs, SS is limited by the thermionic emission of carriers, and is higher than 60 mV/decade at the room temperature. A transistor with a smaller *SS*, could be operating at a lower supply voltage, while providing the same I_{ON} and I_{OFF}. This capability reduces overall power consumption by reducing the dynamic power (as the voltage is lower). A smaller *SS* in analog and RF circuits is also preferred, because it also leads to higher $g_m I_D$ for higher gain and current efficiency:

$$\frac{g_m}{I_D} = \frac{\partial I_D}{\partial V_{GS}} \frac{1}{I_D} = \frac{\partial ln I_D}{\partial V_{GS}} = \frac{ln10}{ss} \tag{1}$$

Steep-slope devices: in this chapter, it is used to represent devices with *SS* lower than 60 mV/decade of conventional CMOS FETs at the room temperature.

3.1 TFET

TFET is essentially a gated p-i-n diode with reverse biasing and asymmetric doping [7]. There have been many types of reported TFET devices [7]. The double gate GaSb-InAs heterojunction TFET (HTFET) device has shown good balance between a steep slope and high I_{ON}, as shown in Fig. 2(a) [11]. When the gate bias voltage is low, the drain source current is small. This is because the wide energy barrier suppresses the probability of band-to-band tunneling (BTBT), as shown in Fig. 2(b). When the gate voltage is increased, the tunneling barrier is narrowed. As a result, the quantum-mechanical BTBT phenomenon creates an abrupt transition between the *ON* and *OFF* states as shown in Fig. 2(c), achieving a low *SS* at the room temperature as shown in Fig. 2(d).

In addition to the steep-slope switching characteristic, HTFET also exhibits some unique features shown in Fig. 2(e–f) [2, 11, 12, 21]. The first feature is the uni-directional tunneling that makes TFET conducting current almost drain-to-source only in a moderate voltage range. This originates from the asymmetric structure in HTFET. The second feature is the negative differential resistance (NDR), which appears in the negative V_{DS} range. The third feature is about the device capacitance. HTFET has less capacitance than

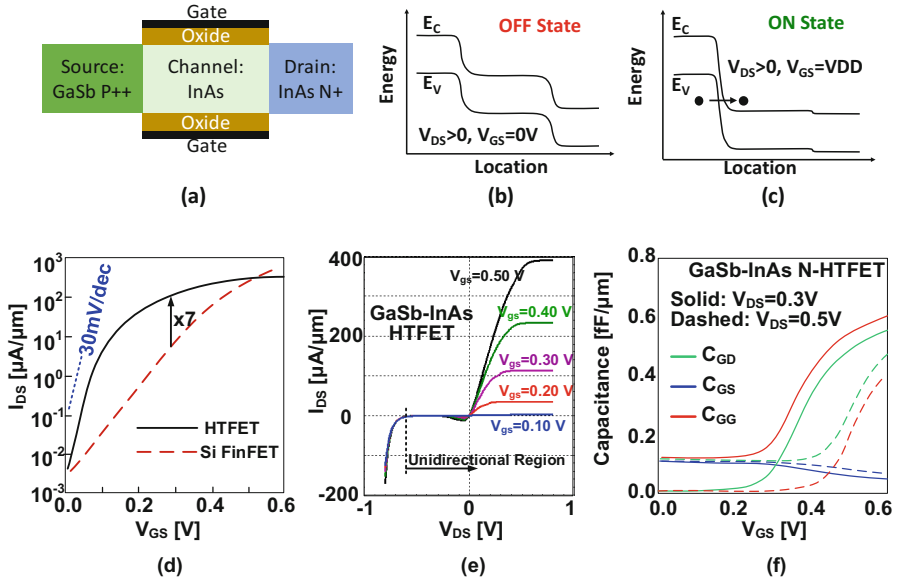

Fig. 2. HTFET: (a) Structure of an N-type HTFET; (b–c) Energy diagrams; (d, e) I_{DS}-V_{GS} comparison; (f) Capacitance [2, 11, 12, 21]

Si FinFET in the low voltage region, and more capacitance in the high voltage region. Table I summarizes some recent TFET experimental results. Device models for TFET are available for circuit SPICE simulations [11, 12, 22–25].

3.2 NCFET

A negative differential capacitor was predicted in 2008 to be stacked at the gate insulator in a MOSFET. By doing this, a small voltage change at the gate could create a larger change in the insulator surface potential, leading to a steeper switching behavior in the I_{DS} versus V_{GS} curves of the transistor [26]. Figure 3(a–b) shows the conceptual device structure and the equivalent gate capacitance network. Recently, there have been advances in both fundamental and experimental results [27–33]. Table 1 shows some recent NCFET results. Due to the challenge of integrating the ferroelectric layer, some early devices were shown with an external ferroelectric capacitor. Recent reported devices are capable of integrating the ferroelectric capacitor around a fin-structure gate.

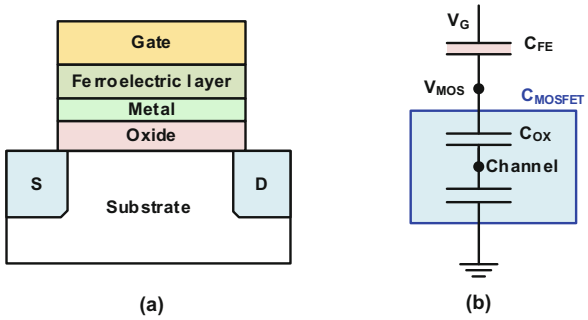

Fig. 3. NCFET: (a) Device structure; (b) Capacitance model [18]

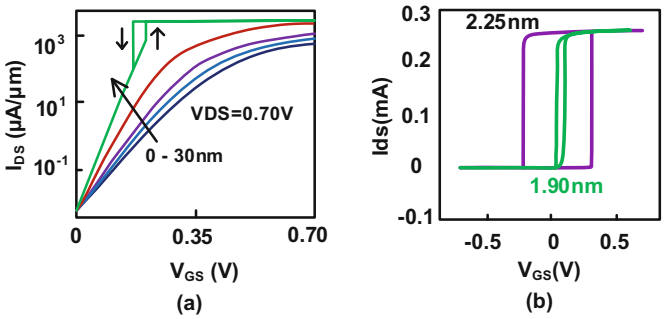

Fig. 4. NCFET simulated switching behavior versus ferroelectric layer thickness [18, 34, 36]

Table 1. Recent advances in TFET, NCFET, and PTD-based PhaseFET

	NCFET			TFET		
Source	[32] IEDM'15	[29] EDL'16	[30] EDL'16	[45] IEDM'14	[44] EDL'15	[43] VLSI'15
Structure	HfZrOFinFET	P(VDF-TrFE)	BiFeO3, FinFET	Si FinFET	III-V vertical	III-V vertical
I_{ON} (A/m)	-	100	1e-4–1e-6	-	8.4	275 N; 30 P
I_{OFF}	-	~5pA/m	1e-12–1e-14	I_{ON}/3e4 N; I_{ON}/2e6 P;	0.1nA/m	0.8nA/m N; 0.3nA/μm P
SS_{min} (mV/dec)	55–87	45–52 (2-4 w/ hysteresis)	8.5–11 P; 16–50 N	56 N;58 P;	64 N	55 N; 115 P;
Hysteresis	Depends	no	yes	no	no	no

Many ferroelectric materials, including PbTiO, BaTiO, Pb(ZrTi)O, HfZrO, etc., could exhibit negative capacitance [30]. The matching of the ferroelectric negative capacitance and the internal MOSFET gate capacitance is the key towards the performance of an NCFET. Thus, a proper capacitance tuning through ferroelectric material layer thickness and area is critical to the success of an NCFET process [30]. Figure 4 shows how the ferroelectric layer thickness affects the switching slope and hysteresis [18, 36]. As the ferroelectric layer thickness increases, *SS* reduces, and a hysteresis window gradually appears and then finally covers both positive and negative V_{GS} range. These characteristics of hysteresis, a steep slope, and their dependence on the ferroelectric material, have been explored in digital logic and memory circuit design [18, 34, 35].

4 New Opportunities Enabled by Emerging Devices, Circuits, and Architectures

This section shows how the IoT system bottlenecks could be mitigated by the opportunities enabled by these emerging devices.

4.1 Energy Harvesters and Sensors with Higher Efficiency

It is intuitive that, by increasing harvested energy from the same ambient environment, the number of performed tasks and functionalities could be increased in an energy-harvesting IoT system. Existing research results have shown that, by making use of the steep switching characteristics, energy harvesters based on these emerging devices could operate better than CMOS transistors in the low-voltage scenarios. Figure 5(a) is a conventional cross-coupled RF rectifier. Figure 5(b) is a conventional DC-DC charge pump. Figure 5(c) is an enhanced TFET DC-DC charge pump topology [11, 12]. The power conversion efficiency (PCE) comparisons in Fig. 6 shows how III-V heterojunction TFET (HTFET) based designs outperform those based on the Si FinFET technology.

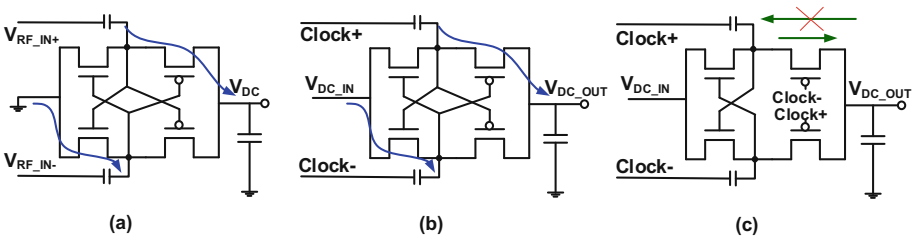

Fig. 5. Rectifier and DC-DC charge pumps: (a) Rectifier; (b) Conventional DC-DC charge pump; (c) Enhanced DC-DC charge pump in III-V HTFET [11, 12]

There are a few factors that lead to the improvement of power conversion efficiency when using HTFETs. The first factor is lower resistive power loss. When the input voltage is low, the resistive power loss limits the overall power conversion efficiency, and the designs in HTFET have less resistive power loss, leading to significant benefits. The second factor is lower capacitive power loss during charge redistribution when the input voltage is low. A combination of these two factors leads to a better transistor sizing strategy for the trade-off between the resistive power loss and switching capacitive loss. The third factor is the uni-directional tunneling conduction which leads to lower reverse power loss in a form of leakage current from the output to the input.

The uni-directional tunneling feature of HTFETs also enables a new circuit topology towards even higher efficiency. For example, in the enhanced HTFET DC-DC converter in Fig. 5, the gate control of the output p-type transistor is now controlled directly by the input clock signal, which enables doubled gate driving voltage and less resistive power loss.

By providing higher power conversion efficiency, HTFET significantly extends the IoT operating applications to lower energy-income scenarios. It is also noted that, from another aspect, an energy harvester itself could be treated as a sensor that senses the input power level. A higher PCE provided by HTFET also improves the sensing sensitivity, such as motion or vibration sensors and radiation sensors. Similar rectifier and DC-DC charge pump designs based on NCFET and PhaseFET, although there is no result reported, a higher PCE will not be a surprise.

4.2 Analog Processing and Communication

For analog processing and transceiver designs, the lowest achievable power consumption is determined by the trade-off between various specifications, including gain, speed and bandwidth, linearity and spectral performance (such as spurious-free dynamic range or SFDR, signal-to-noise + distortion ratio or SNDR, input-referred noise), etc. Figure 7 shows the evaluation results of TFET based designs, including A/D converter, sense amplifier and D/A converter.

Figure 7(a) evaluates a 6-bit 10-MS/s successive-approximate-register (SAR) A/D converter, and Fig. 7(b) shows how HTFET is capable of lowering the energy beyond the limit of CMOS [24]. Such a gain stems from higher current efficiency for both digital logic (lower dynamic power) and the comparator (higher g_m/I_D). Figure 7(c–d)

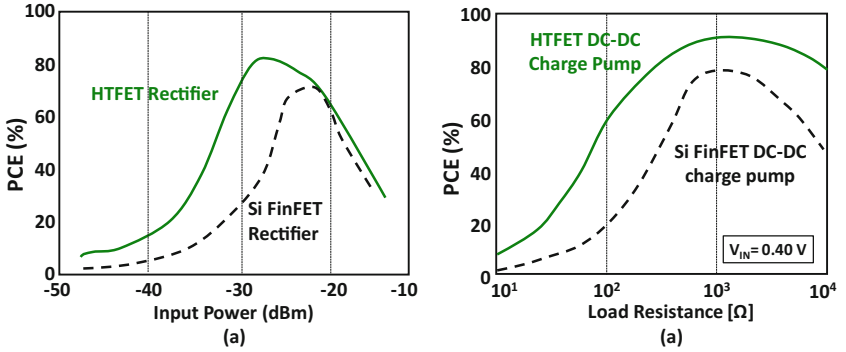

Fig. 6. PCE of rectifier in (a) and DC-DC charge pump in (b) [11, 12]

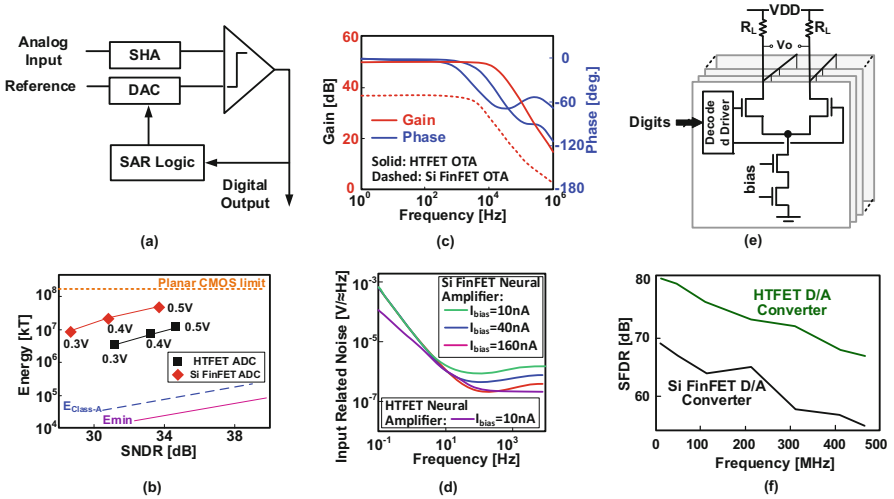

Fig. 7. Comparisons between HTFET and Si FinFET circuits: (a–b) a 6-bit SAR A/D converter and performance; (c–d) bio-signal sensing OTA gain and input referred noise versus frequency; (e–f) Current-steering D/A converter and its SFDR [22, 24, 25]

shows the performance evaluation of a low-noise bio-signal sense amplifier (LNA) [22]. Here HTFET based design also has a higher gain because of higher g_m/I_D. A higher gain also leads to the input referred noise reduction as by definition, the input referred noise is the output noise divided by the gain of the amplifier. Figure 7(d–e) shows the performance evaluation of a current-steering D/A converter [25]. HTFET shows a higher SFDR because of less transistor capacitance at the low voltage region, which leads to less coupled switching glitches and higher output impedance.

TFET based typical RF circuit designs were reviewed in [37], including RF LNA, mixer, frequency doubler, oscillators, etc. Substantial benefits are observed using

HTFET in low-voltage high-frequency circuits, with higher preferred nonlinearity for mixers, and higher transconductance and gain at low power and low current levels.

Considering that the above designs are widely used as a front-end and back-end block in IoT systems, as shown in Fig. 1, significant power saving could be achieved by adopting HTFET.

4.3 Energy-Efficient Volatile Digital Logic

There have been evaluations between TFET and conventional CMOS technologies on digital circuits, including combinational gates and adders, sequential gates like D flip-flops, and SRAM. TFET based designs are shown to outperform conventional CMOS in energy-delay especially with a low supply voltage, as shown in Fig. 8 [38, 39]. It is also noted that, when using TFET for pass-transistor logic, the device feature of uni-directional tunneling conduction affects the functionality and is handled with by either adding another parallel pass transistor for the other opposite direction conduction, or re-designing the circuit topology.

As the technology scales down to smaller dimensions, the parasitics and contact non-idealities play a more important role. Recently, an evaluation work considering parasitics indicates that, similar performance advantage by HTFET is still observed even with higher contact resistance due to a vertical structure [40]. Another work on processor design and evaluation shows that, with less energy per instruction (EPI), TFET based designs extends the design space when considering the thermal limit and the degree of parallelism, leading to higher performance [41].

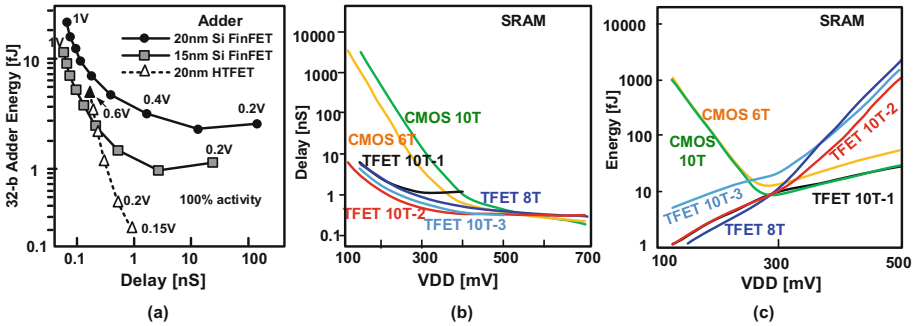

Fig. 8. TFET design examples: (a) a 32-b adder; (b–c) SRAM [38, 39]

Similarly, for NCFET, lower energy-delay has been observed for digital logic in low-voltage scenarios when operating with a moderate-to-high capacitive wire load, as shown in Fig. 9(a) [35]. The hysteresis in the positive V_{GS} region as shown in Fig. 5(c) could significantly improve the input noise margin by an amount of the hysteresis window width [34]. The theory of this could be understood as follows. Considering an NCFET inverter with n-type NCFET transistor and p-type conventional transistor, the n-type NCFET transistor will not turn on until the input voltage increases beyond the

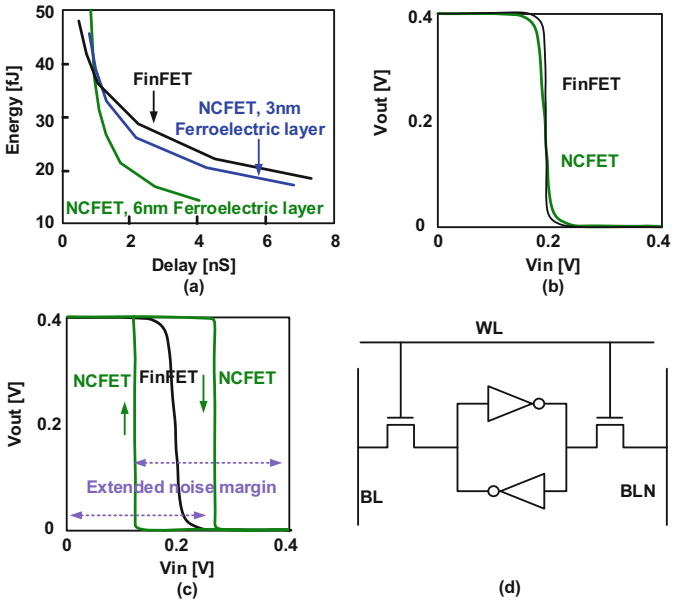

Fig. 9. NCFET evaluation [34, 35]: (a) Energy-delay for a Koggy-Stone adder; (b) Inverter input-output transfer function (NCFET has 16 nm ferroelectric layer thickness); (c) Inverter input-output transfer function (NCFET has 27 nm ferroelectric layer thickness) showing improved input noise margin with NCFET hysteresis; (d) NCFET SRAM with enhanced noise margin with NCFET hysteresis.

rising hysteresis edge, nor will it turn off until the input signal reduces beyond the falling hysteresis edge. This is illustrated in Fig. 9(c). The improved input noise margin of NCFET logic could also be used to build SRAM cells with enhanced noise margin, as shown in Fig. 9(d) [34].

4.4 Energy-Efficient Nonvolatile Logic and Memory Circuits

For IoT energy-harvesting applications where the power supply is intermittent, it is critical to sustain inter-process data during power outages. Therefore, on-chip non-volatile memory (NVM) becomes intriguing because of its non-volatility to avoid refreshing and its immunity to power failures. The possibility of on-chip memory access instead of out-of-chip access also reduces the energy consumption. Meanwhile, power-gating is very useful to further reduce the static leakage power of idle digital circuits, and NVM could be used to store the state of these idle circuits while turning off their power supply.

Furthermore, with on-chip NVM and associated sensing and control, a nonvolatile processor (NVP) could be built to back up the processor states and data, including memory, D flip-flops (DFF), registers, etc., into this NVM during power failures [14, 42, 48–54]. Such on-chip data backup and restore operations reduce the risk of losing computation progress. When compared with out-of-chip nonvolatile backup options,

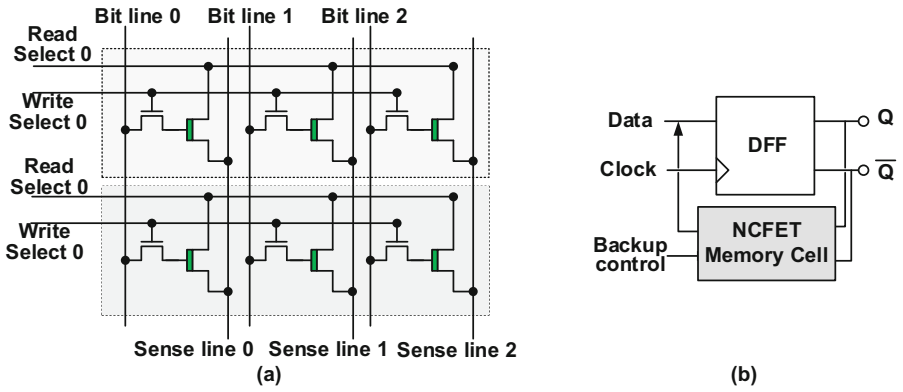

Fig. 10. NCFET circuits [18, 34]. (a) Two-transistor (2T) nonvolatile memory array; (b) Nonvolatile NCFET D flip-flop.

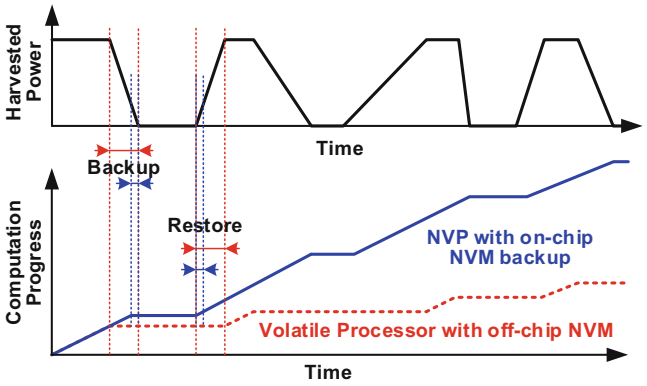

Fig. 11. Comparisons of computation progress between volatile processor with off-chip NVM and nonvolatile processor with on-chip NVM.

this on-chip backup solution has lower power, energy and interface overhead. Such an advantage enables more computational progress in power-supply-intermittent scenarios [13], as illustrated in Fig. 11.

With the tunable hysteresis in NCFETs, energy-efficient nonvolatile memory could be built. Figure 10(a) shows an NCFET NVM design based on an NCFET hysteresis tuned around $V_{GS} = 0$ V (see Fig. 3(d)) [18]. It is reported that this NCFET NVM exhibits improved access energy-delay. Different from existing nonvolatile memory devices such as ReRAM and STT-RAM, the NCFET itself is also a transistor. This provides opportunities of logic-in-memory process.

Attaching an NCFET nonvolatile bit storage to a conventional volatile DFF, a nonvolatile DFF with external backup and reset controls could also be built, as illustrated in Fig. 10(c) [34]. With a local nonvolatile memory cell, the backup and restore

energy becomes lower than that of the clustered nonvolatile memory backup solution in which long-distance data transmission is time and energy consuming.

More aggressively, by exploring the embedded logic and non-volatility in NCFET, an external-control-free intrinsically nonvolatile DFF is possible. Such an intrinsically NV-DFF could be built by replacing the slave latch of a conventional volatile CMOS master-slave DFF with one NCFET nonvolatile latch shown in Fig. 12. Making the NV-DFF intrinsically nonvolatile enables the removal of external controls, and makes fine-grained backup/restore operations in NVP and power-gating applications possible with more energy savings.

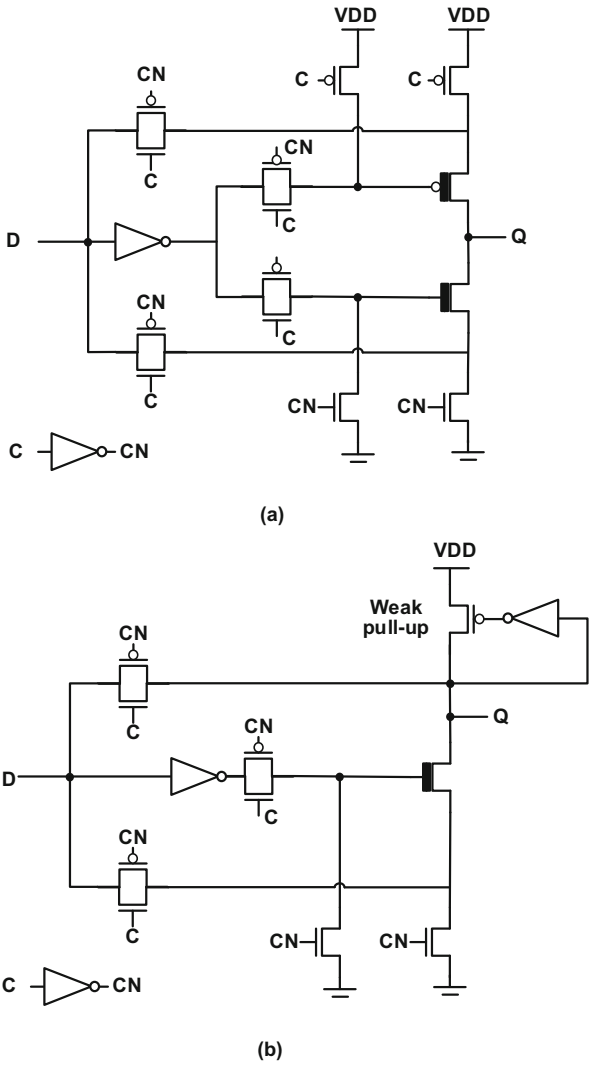

Fig. 12. NCFET nonvolatile latches (NCFET transistors are drawn with thick gates).

With the synergy of the low-voltage NCFET logic [35], NCFET nonvolatile memory array [18], and the NCFET NV-DFF, an energy-efficient NVP is designed, as shown in Fig. 13(b), in comparison with a conventional NVP in Fig. 13(a). As both logic and memory are intrinsically nonvolatile, there is no need for backup and restore controls for the NCFET storage. The baseline design uses conventional CMOS transistors for logic, a clustered FeRAM array as data and instruction memory, and NV-DFF using ferroelectric capacitor for state backup under external control [56].

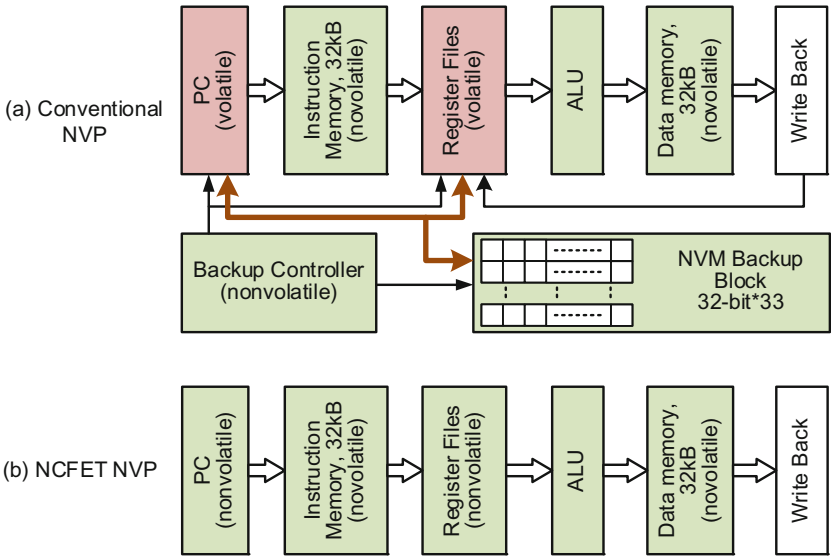

Fig. 13. NVP design using NCFET logic and memory

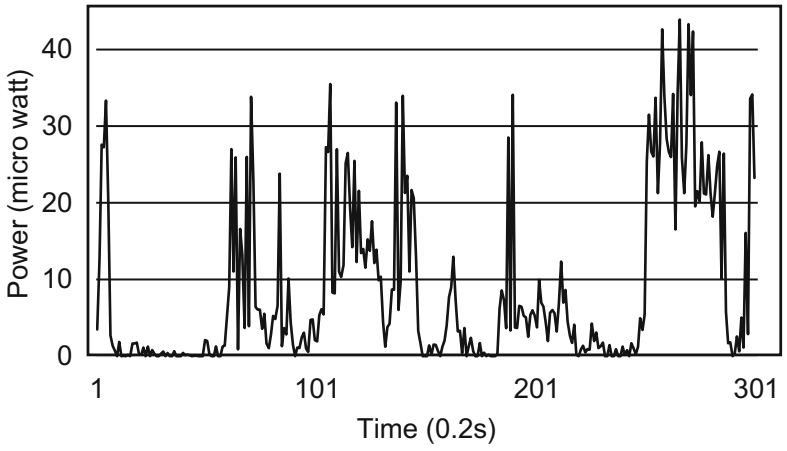

Fig. 14. Input power profile in the test

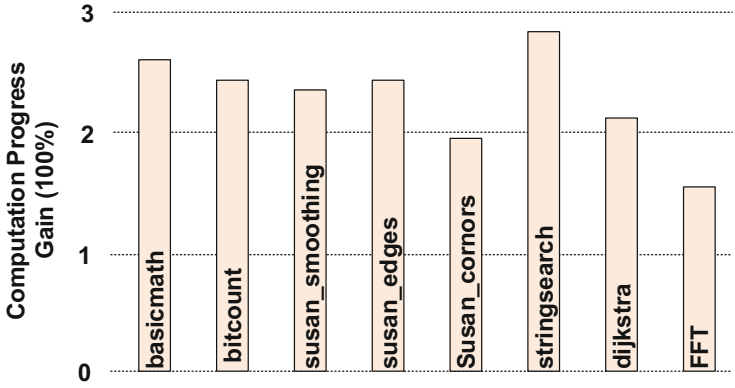

Fig. 15. Computation progress gain for various test benches

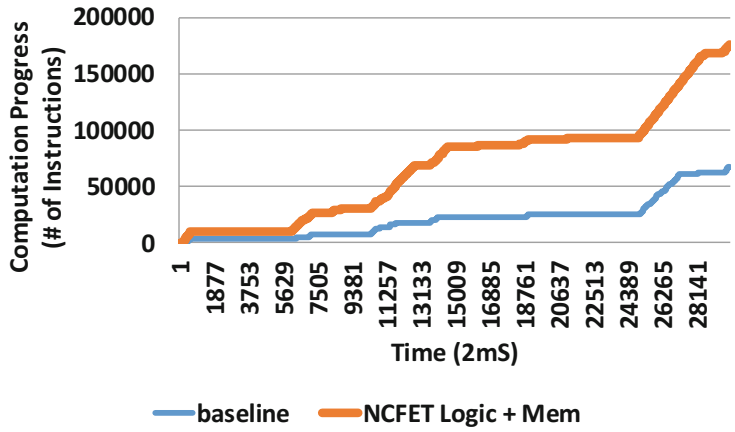

Fig. 16. Comparison between NCFET NVP and the baseline NVP of computation progress versus time (Tesebench: basic math).

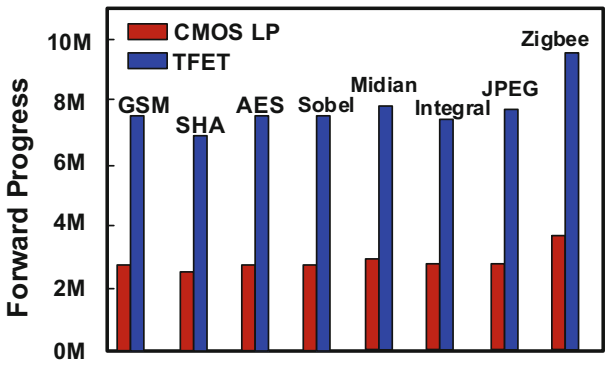

Fig. 17. TFET NVP with more forward progress for various tasks (source: [57]).

Giving the harvested RF power from TV stations, as shown in the power profile sampled per 0.2S in Fig. 14, the average input power is 8.7 μW, with the peak up to ~45 μW and frequent power failures with power lower than nW. The simulations are carried out in various test cases in MiBench [55]. Figure 15 shows the simulation results for these testbenches. Figure 16 shows the comparison of computation progress versus time. The computation progress gain ranges between 1.5× to 2.8×, which confirms the benefit of using NCFET for NVP design.

When only TFET is used to replace CMOS in NVP design, improvement of computation progress is also observed, as shown in Fig. 17 [57]. The improvement comes from the energy savings by low-power digital logic and less number of backup/restore operations.

4.5 Nonvolatile Computing Architectures

In this new NVP design regime, most existing guidance of low-power design techniques are still useful, but there has also been significant difference in the design and optimization methodology.

The first different rule is that "design for low power does not guarantee more computing progress" [13]. This is because, in a battery-less energy-harvesting IoT system, there is no ideal temporary energy storage, and the harvested energy will be wasted in the form of overflowing or leaking if it is not used efficiently in time. In other words, the computing forward progress (CFP) indicated by the number of executed instructions (NI) could be expressed as a function of computation energy (CE) and energy-per-instruction (EPI):

$$\mathrm{CFP} = \mathrm{CE}/\mathrm{EPI}, \tag{2}$$

where CE is a fraction of the total harvested energy, considering the energy loss from backup/restore operations, leakage and overflow in the energy storage capacitor, and leakage in the circuits.

And the fact is that the lowest EPI does not guarantee the highest CE because of the abovementioned energy harvesting and storage non-idealities. For example, an out-of-order processor may contribute to more forward progress than a non-pipelined processor in scenarios when the harvested power is higher. As a result, the power of the processor should adapt to the harvester and energy storage status to find the best trade-off between the lowest EPI and the most CE.

There are various approaches to configuring the processor so as to fit the input power trace. One approach is to dynamically switch between different processing cores which are all embedded on the same chip based on level of harvested power and the store energy [49]. The second approach is to dynamically scale the operating frequency and voltage (DVFS) accordingly [53, 54]. The third approach is to dynamically re-allocate computing and storage resources for the processor which turns out to be a different degree of parallelism [54].

In addition to the trade-off between CE and EPI, there are other optimizations that have significant impact on the overall forward progress.

The first consideration is "what" and "when" to back up the computing states. There are various reasons that make this consideration important. First of all, less amount of backup states needs less backup energy but needs more energy to recover and re-compute; Secondly, a backup operation which is carried out too early may be a complete waste of energy and time as it may not be necessary at all, while a too-late backup may lead to backup failure and progress rolling-backup. Also, there can be a risk to take, on how much energy that could be harvested in the future – which could also be counted into a certain amount of usable energy.

The second consideration is how to understand the feature of the harvested energy, and how to predict its trend. An accurate prediction of the input power will certainly help system configuration for more forward progress. For some energy sources such as ambient RF energy, the harvested power varies radically and is challenging to predict. Meanwhile, for some other energy sources, such as motion and solar energy sources, the harvested power has a certain pattern and could be predicted. Machine learning techniques have been proposed to predict the future energy to assist dynamic system configuration for more forward progress [49, 54].

The third consideration is on-chip NVM optimization. There are a few key factors that must be considered. One factor is what types of on-chip memory to use for backup operations. Different NVM devices, such as ReRAM, FeRAM, STT-RAM, and the emerging NCFET NVM, etc., have different energy-delay performance for read and write operations. Another factor is to use centered (aka clustered) or distributed memory. Distributed memory uses a local nearby NVM bit storage close to each DFF with a copy of access interface circuit. Clustered memory is implemented with arrays of memory and could be dense in area due to shared elements such as sense amplifiers but may consume more energy and delay in access due to longer interconnection lines and limited degree of access parallelism.

5 Future Work for IoT Using Emerging Devices

While emerging devices have shown great potential for future energy-efficient IoT applications, there is still a large gap between what has been experimentally demonstrated and a complete system implementation and application mapping. Significant efforts from all the levels of device, circuits, system and applications are required to speed up the progress [58].

Device understanding, characterization, and integrated fabrication: Continuous optimization of material and process is required for large-scale integration. It is a key to build accurate models of emerging devices that support more aspects of devices features, such as matching, noise, endurance, parasitics, etc., for circuit and higher level simulations;

Circuit and architecture optimizations: It is unlikely for emerging device features to be used as a drop-in replacement for all conventional CMOS techniques. Innovative circuit topology re-design and optimization are sometimes a must to obtain the desired circuit functionality and performance, which also brings additional trade-offs to carry out. Circuit and architecture optimizations to make the most use of pros and mitigate

cons of emerging devices are necessary [13–15, 46]. Meanwhile, device features deviating from conventional CMOS behavior may actually be very useful in some applications, highlighting the necessity of device-circuit-application co-design.

Higher-level considerations: Quality-of-service (QoS) and task scheduling optimization, with support from software design are also an area of key interest [47, 51, 52]. Security, privacy, and communication protocols are core concerns in any IoT deployment. The study of the interaction of quality and security metrics with design and power efficiency optimizations requires further investigations from device to architecture to software ecosystem.

The exploration of emerging devices, circuits, and architectures should be a joint effort. It is impossible to dig into all emerging devices for all different types of applications. Efforts spent for emerging device modeling and benchmarking may not be meaningful if the device finally turns out to be far from satisfactory. Moreover, research on modeling and higher-level design needs strong support from device developing groups and continuous interactions with them are crucial to ensure that each is aware of the newest findings and phenomena understandings in the other's domain.

6 Conclusion

This chapter has discussed new opportunities in Internet-of-Things enabled by emerging devices, circuits and architectures through enhanced and new features to the implementations. The future work for IoT based on emerging technologies is also discussed.

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References

1. Atzori, L., Iera, A., Morabito, G.: The internet of things: a survey. Comput. Networks **54**, 2787–2805 (2010)
2. Li, X., Heo, U.D., Ma, K., Narayanan, V., Liu, H., Datta, S.: Rf-powered systems using steep-slope devices. In: 2014 IEEE 12th International New Circuits and Systems Conference (NEWCAS) (2014)
3. Kim, S., Vyas, R., Bito, J., Niotaki, K., Collado, A., Georgiadis, A., Tentzeris, M.M.: Ambient RF energy-harvesting technologies for self-sustainable standalone wireless sensor platforms. Proc. IEEE **102**, 1649–1666 (2014)
4. Nikonov, D.E., Young, I.A.: Overview of beyond-CMOS devices and a uniform methodology for their benchmarking. Proc. IEEE **101**, 2498–2533 (2013)
5. Lu, L., Li, X., Narayanan, V., Datta, S.: A reconfigurable low-power BDD logic architecture using ferroelectric single-electron transistors. IEEE Trans. Electron Devices **62**(3), 1052–1057 (2015). doi:10.1109/ted.2015.2395252

6. Roy, K., Sharad, M., Fan, D., Yogendra, K.: Computing with spin-transfer-torque devices: prospects and perspectives. In: 2014 IEEE Computer Society Annual Symposium on VLSI (2014)
7. Seabaugh, A.C., Zhang, Q.: Low-voltage tunnel transistors for beyond CMOS logic. Proc. IEEE **98**, 2095–2110 (2010)
8. Khan, A.I., Yeung, C.W., Hu, C., Salahuddin, S.: Ferroelectric negative capacitance MOSFET: capacitance tuning & antiferroelectric operation. In: 2011 International Electron Devices Meeting (2011)
9. Swaminathan, K., Liu, H., Li, X., Kim, M.S., Sampson, J., Narayanan, V.: Steep slope devices: enabling new architectural paradigms. In: Proceedings of the 51st Annual Design Automation Conference on Design Automation Conference - DAC 2014 (2014)
10. Brito, M.A.G.D., Galotto, L., Sampaio, L.P., Melo, G.D.A.E., Canesin, C.A.: Evaluation of the main MPPT techniques for photovoltaic applications. IEEE Trans. Ind. Electron. **60**, 1156–1167 (2013)
11. Liu, H., Li, X., Vaddi, R., Ma, K., Datta, S., Narayanan, V.: Tunnel FET RF rectifier design for energy harvesting applications. IEEE J. Emerg. Sel. Top. Circuits Syst. **4**, 400–411 (2014)
12. Heo, U., Li, X., Liu, H., Gupta, S., Datta, S., Narayanan, V.: A high-efficiency switched-capacitance HTFET charge pump for low-input-voltage applications. In: 2015 28th International Conference on VLSI Design (2015)
13. Ma, K., Zheng, Y., Li, S., Swaminathan, K., Li, X., Liu, Y., Sampson, J., Xie, Y., Narayanan, V.: Architecture exploration for ambient energy harvesting nonvolatile processors. In: 2015 IEEE 21st International Symposium on High Performance Computer Architecture (HPCA) (2015)
14. Ma, K., Li, X., Li, S., Liu, Y., Sampson, J.J., Xie, Y., Narayanan, V.: Nonvolatile processor architecture exploration for energy-harvesting applications. IEEE Micro. **35**, 32–40 (2015)
15. Ma, K., Li, X., Swaminathan, K., Zheng, Y., Li, S., Liu, Y., Xie, Y., Sampson, J.J., Narayanan, V.: Nonvolatile processor architectures: efficient, reliable progress with unstable power. IEEE Micro. **36**, 72–83 (2016)
16. Liu, V., Parks, A., Talla, V., Gollakota, S., Wetherall, D., Smith, J.R.: Ambient backscatter. In: Proceedings of the ACM SIGCOMM 2013 Conference on SIGCOMM - SIGCOMM 2013 (2013)
17. Ueki, M., Takeuchi, K., Yamamoto, T., Tanabe, A., Ikarashi, N., Saitoh, M., Nagumo, T., Sunamura, H., Narihiro, M., Uejima, K., Masuzaki, K., Furutake, N., Saito, S., Yabe, Y., Mitsuiki, A., Takeda, K., Hase, T., Hayashi, Y.: Low-power embedded ReRAM technology for IoT applications. In: 2015 Symposium on VLSI Technology (VLSI Technology) (2015)
18. George, S., Gupta, S., Narayanan, V., Ma, K., Aziz, A., Li, X., Khan, A., Salahuddin, S., Chang, M.-F., Datta, S., Sampson, J.: Nonvolatile memory design based on ferroelectric FETs. In: Proceedings of the 53rd Annual Design Automation Conference on - DAC 2016 (2016)
19. Chi, P., Li, S., Xu, C., Zhang, T., Zhao, J., Liu, Y., Wang, Y., Xie, Y.: PRIME: a novel processing-in-memory architecture for neural network computation in ReRAM-based main memory. In: 2016 ACM/IEEE 43rd Annual International Symposium on Computer Architecture (ISCA) (2016)
20. Roman, R., Najera, P., Lopez, J.: Securing the internet of things. Computer **44**, 51–58 (2011)
21. Kim, M.S., Liu, H., Swaminathan, K., Li, X., Datta, S., Narayanan, V.: Enabling power-efficient designs with III-V tunnel FETs. In: 2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS) (2014)

22. Liu, H., Shoaran, M., Li, X., Datta, S., Schmid, A., Narayanan, V.: Tunnel FET-based ultra-low power, low-noise amplifier design for bio-signal acquisition. In: Proceedings of the 2014 International Symposium on Low Power Electronics and Design - ISLPED 2014 (2014)
23. Tsai, W.-Y., Liu, H., Li, X., Narayanan, V.: Low-power high-speed current mode logic using Tunnel-FETs. In: 2014 22nd International Conference on Very Large Scale Integration (VLSI-SoC) (2014)
24. Kim, M.S., Liu, H., Li, X., Datta, S., Narayanan, V.: A steep-slope tunnel FET based SAR analog-to-digital converter. IEEE Trans. Electron Devices **61**, 3661–3667 (2014)
25. Kim, M.S., Li, X., Liu, H., Sampson, J., Datta, S., Narayanan, V.: Exploration of low-power High-SFDR current-steering D/A converter design using steep-slope heterojunction tunnel FETs. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **24**(6), 2299–2309 (2016)
26. Salahuddin, S., Datta, S.: Use of negative capacitance to provide voltage amplification for low power nanoscale devices. Nano Lett. **8**, 405–410 (2008)
27. Hu, C., Salahuddin, S., Lin, C.-I., Khan, A.: 0.2 V adiabatic NC-FinFET with 0.6 mA/μm ION and 0.1nA/μm IOFF. In: 2015 73rd Annual Device Research Conference (DRC) (2015)
28. Lee, M.H., Wei, Y.-T., Chu, K.-Y., Huang, J.-J., Chen, C.-W., Cheng, C.-C., Chen, M.-J., Lee, H.-Y., Chen, Y.-S., Lee, L.-H., Tsai, M.-J.: Steep slope and near non-hysteresis of FETs With antiferroelectric-like HfZrO for low-power electronics. IEEE Electron Device Lett. **36**, 294–296 (2015)
29. Jo, J., Choi, W.Y., Park, J.-D., Shim, J.W., Yu, H.-Y., Shin, C.: Negative capacitance in organic/ferroelectric capacitor to implement steep switching MOS devices. Nano Lett. **15**, 4553–4556 (2015)
30. Khan, A.I., Chatterjee, K., Duarte, J.P., Lu, Z., Sachid, A., Khandelwal, S., Ramesh, R., Hu, C., Salahuddin, S.: Negative capacitance in short-channel FinFETs externally connected to an epitaxial ferroelectric capacitor. IEEE Electron Device Lett. **37**, 111–114 (2016)
31. Jo, J., Shin, C.: Negative capacitance field effect transistor with hysteresis-free Sub-60-mV/Decade switching. IEEE Electron Device Lett. **37**, 245–248 (2016)
32. Li, K.-S., Chen, P.-G., Lai, T.-Y., Lin, C.-H., Cheng, C.-C., Chen, C.-C., Wei, Y.-J., Hou, Y.-F., Liao, M.-H., Lee, M.-H., Chen, M.-C., Sheih, J.-M., Yeh, W.-K., Yang, F.-L., Salahuddin, S., Hu, C.: Sub-60 mV-swing negative-capacitance FinFET without hysteresis. In: 2015 IEEE International Electron Devices Meeting (IEDM) (2015)
33. Lee, M.H., Chen, P.-G., Liu, C., Chu, K.-Y., Cheng, C.-C., Xie, M.-J., Liu, S.-N., Lee, J.-W., Huang, S.-J., Liao, M.-H., Tang, M., Li, K.-S., Chen, M.-C.: Prospects for ferroelectric HfZrOx FETs with experimentally CET = 0.98 nm, SSfor = 42 mV/dec, SSrev = 28 mV/dec, switch-off 0.2 V, and hysteresis-free strategies. In: 2015 IEEE International Electron Devices Meeting (IEDM) (2015)
34. George, S., Aziz, A., Li, X., Datta, S., Sampson, J., Gupta, S., Narayanan, V.: NCFET based logic for energy harvesting systems. In: SRC TECHCON 2015 (2015)
35. George, S., Aziz, A., Li, X., Kim, M.S., Datta, S., Sampson, J., Gupta, S., Narayanan, V.: Device circuit co design of FEFET based logic for low voltage processors. In: 2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI) (2016)
36. Aziz, A., Ghosh, S., Datta, S., Gupta, S.: Physics-based circuit-compatible SPICE model for ferroelectric transistors. IEEE Electron Device Lett. **37**, 1 (2016)
37. Asbeck, P.M., Lee, K., Min, J.: Projected performance of heterostructure tunneling FETs in low power microwave and mm-wave applications. IEEE J. Electron Devices Soc. **3**, 122–134 (2015)
38. Datta, S., Bijesh, R., Liu, H., Mohata, D., Narayanan, V.: Tunnel transistors for energy efficient computing. In: 2013 IEEE International Reliability Physics Symposium (IRPS) (2013)

39. Saripalli, V., Datta, S., Narayanan, V., Kulkarni, J.P.: Variation-tolerant ultra low-power heterojunction tunnel FET SRAM design. In: 2011 IEEE/ACM International Symposium on Nanoscale Architectures (2011)
40. Kim, M.S., Cane-Wissing, W., Li, X., Sampson, J., Datta, S., Gupta, S.K., Narayanan, V.: Comparative area and parasitics analysis in FinFET and heterojunction vertical TFET standard cells. ACM J. Emerg. Technol. Comput. Syst. **12**, 1–23 (2016)
41. Swaminathan, K., Liu, H., Sampson, J., Narayanan, V.: An examination of the architecture and system-level tradeoffs of employing steep slope devices in 3D CMPs. ACM SIGARCH Comput. Archit. News. **42**, 241–252 (2014)
42. Wang, Y., Liu, Y., Li, S., Zhang, D., Zhao, B., Chiang, M.-F., Yan, Y., Sai, B., Yang, H.: A 3us wake-up time nonvolatile processor based on ferroelectric flip-flops. In: 2012 Proceedings of the ESSCIRC (ESSCIRC) (2012)
43. Pandey, R., Madan, H., Liu, H., Chobpattana, V., Barth, M., Rajamohanan, B., Hollander, M.J., Clark, T., Wang, K., Kim, J.- H., Gundlach, D., Cheung, K.P., Suehle, J., Engel-Herbert, R., Stemmer, S., Datta, S.: Demonstration of p-type In0.7Ga0.3As/-GaAs0.35Sb0.65 and n-type GaAs0.4Sb0.6/In0.65Ga0.35As complimentary Heterojunction Vertical Tunnel FETs for ultra-low power logic. In: 2015 Symposium on VLSI Technology (VLSI Technology) (2015)
44. Rajamohanan, B., Pandey, R., Chobpattana, V., Vaz, C., Gundlach, D., Cheung, K.P., Suehle, J., Stemmer, S., Datta, S.: 0.5 V supply voltage operation of In0.65Ga0.35As/GaAs0.4Sb0.6Tunnel FET. IEEE Electron Device Lett. **36**, 20–22 (2015)
45. Morita, Y., Mori, T., Fukuda, K., Mizubayashi, W., Migita, S., Matsukawa, T., Endo, K., O'uchi, S., Liu, Y., Masahara, M., Ota, H.: Experimental realization of complementary p- and n- tunnel FinFETs with subthreshold slopes of less than 60 mV/decade and very low (pA/μm) off-current on a Si CMOS platform. In: 2014 IEEE International Electron Devices Meeting (2014)
46. Liu, Y., Yang, H., Wang, Y., Wang, C., Sheng, X., Li, S., Zhang, D., Sun, Y.: Power system design and task scheduling for photovoltaic energy harvesting based nonvolatile sensor nodes. In: Lin, Y.-L., et al. (eds.) Smart Sensors and Systems, pp. 243–277. Springer, Cham (2015)
47. Zhang, D., Liu, Y., Li, J., Xue, C.J., Li, X., Wang, Y., Yang, H.: Solar power prediction assisted intra-task scheduling for nonvolatile sensor nodes. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. **35**, 724–737 (2016)
48. Liu, Y., Wang, Z., Lee, A., Su, F., Lo, C.-P., Yuan, Z., Lin, C.-C., Wei, Q., Wang, Y., King, Y.-C., Lin, C.-J., Khalili, P., Wang, K.-L., Chang, M.-F., Yang, H.: 4.7 A 65 nm ReRAM-enabled nonvolatile processor with 6 × reduction in restore time and 4 × higher clock frequency using adaptive data retention and self-write-termination nonvolatile logic. In: 2016 IEEE International Solid-State Circuits Conference (ISSCC) (2016)
49. Ma, K., Li, X., Liu, Y., Sampson, J., Xie, Y., Narayanan, V.: Dynamic machine learning based matching of nonvolatile processor microarchitecture to harvested energy profile. In: 2015 IEEE/ACM International Conference on Computer-Aided Design (ICCAD) (2015)
50. Li, Q., Zhao, M., Hu, J., Liu, Y., He, Y., Xue, C.J.: Compiler directed automatic stack trimming for efficient non-volatile processors. In: Proceedings of the 52nd Annual Design Automation Conference on - DAC 2015 (2015)
51. Xie, M., Pan, C., Hu, J., Yang, C., Chen, Y.: Checkpoint-aware instruction scheduling for nonvolatile processor with multiple functional units. In: The 20th Asia and South Pacific Design Automation Conference (2015)

52. Wang, Y., Liu, Y., Wang, C., Li, Z., Sheng, X., Lee, H.G., Chang, N., Yang, H.: Storage-Less and Converter-Less Photovoltaic Energy Harvesting with Maximum Power Point Tracking for Internet of Things. IEEE Trans. Comput. Aided Design Integr. Circuits Syst. **35**, 173–186 (2016)
53. Ma, K., Li, X., et al.: Dynamic power and energy management for energy harvesting nonvolatile processor systems. ACM Trans. Embed. Comput. Syst. (TECS) **16**(4), 107:1–107:23 (2017)
54. Ma, K., Li, X., et al.: Spendthrift: machine learning based resource and frequency scaling for ambient energy harvesting nonvolatile processors. In: ASP-DAC (2017)
55. Guthaus, M.R., Ringenberg, J.S., Ernst, D., Austin, T.M., Mudge, T., Brown, R.B.: MiBench: a free, commercially representative embedded benchmark suite. In: Proceedings of the Fourth Annual IEEE International Workshop on Workload Characterization. WWC-4 (Cat. No.01EX538), pp. 3–14 (2001)
56. Kimura, H., Fuchikami, T., Marumoto, K., Fujimori, Y., Izumi, S., Kawaguchi, H., Yoshimoto, M.: A 2.4 pJ ferroelectric-based non-volatile flip-flop with 10-year data retention capability. In: 2014 IEEE Asian Solid-State Circuits Conference (A-SSCC), KaoHsiung, pp. 21–24 (2014)
57. Ma, K., Li, X., Sampson, J., Xie, Y., Liu, Y., Narayanan, V.: Nonvolatile processor optimization for ambient energy harvesting scenarios. In: The 15th Non-volatile Memory Technology Symposium (NVMTS), pp. 1–3 (2015)
58. Li, X., Ma, K., George, S., Sampson, J., Narayanan, V.: Enabling Internet-of-Things: Opportunities brought by emerging devices, circuits, and architectures. In: 2016 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Tallinn, pp. 1–6 (2016)