A 14 Bit 500 MS/s CMOS DAC Using Complementary Switched Current Sources and Time-Relaxed Interleaving DRRZ

Xueqing Li, Qi Wei, Zhen Xu, Jianan Liu, Hui Wang, and Huazhong Yang, *Senior Member, IEEE*

***Abstract*—A 14 bit 500 MS/s current-steering digital-to-analog converter (DAC) was designed and fabricated in 0.13 μm CMOS process. For traditional wide-band current-steering DACs, the spurious-free dynamic range (SFDR) is limited by nonlinear distortions from the code-dependent load variations and the code-dependent switching glitches. They are analyzed in this paper and mitigated by the proposed complementary switched current sources (CSCS) and time-relaxed interleaving digital-random-return-to-zero (TRI-DRRZ), respectively. The proposed techniques are fabricated and measured, with an SFDR of 84.8 dB at 11 MHz signal frequency and 73.5 dB at 244 MHz. The DAC consumes 299 mW from a mixed power supply of 1.2 V and 2.5 V with an active area of 1.85×0.65 mm^2.**

***Index Terms*—Digital-to-analog converter (DAC), interleaving, return-to-zero (RZ), spurious-free dynamic range (SFDR).**

I. Introduction

FAST current-steering digital-to-analog converters (DACs) have been widely used in wide band transmitters, arbitrary waveform generators, and direct digital frequency synthesizers because of their intrinsic high speed, moderate accuracy, and ability to drive resistive loads directly [1]–[10]. Fig. 1 shows a simplified diagram of a traditional current-steering DAC. In such a DAC, a series of weighted current sources are switched either to the positive or negative output node, forming a differential voltage output on the equivalent resistive loads.

For fast DACs, spurious-free dynamic range (SFDR) is a key parameter for describing the required linearity. To achieve a high SFDR, non-ideal effects, such as current source mismatches [8]–[15], timing errors [16], code-dependent load variations [1], [3], [17], and code-dependent switching glitches [1], [4]–[6], [18]–[23], need mitigation. Among these effects, code-dependent load variations and switching glitches have become two bottlenecks in recently published wide-band high-dynamic-range CMOS DAC designs [1]–[4], [8].

Manuscript received July 08, 2013; revised November 05, 2013, January 06, 2014, and February 22, 2014; accepted March 05, 2014. Date of publication July 08, 2014; date of current version July 24, 2014. This work was sponsored in part by the 863 program of China under Contract 2013AA014103 and the National Science Foundation for Young Scientists of China under Grant 61306029. This paper was recommended by Associate Editor K. Doris.

X. Li was with the Department of Electronic Engineering, Tsinghua University, Beijing, 100084, China. He is now with the Department of Computer Science and Engineering, Pennsylvania State University, State College, PA 16802 USA (e-mail: lixueq@gmail.com).

Q. Wei, Z. Xu, J. Liu, H. Wang and H. Yang are with the Department of Electronic Engineering, Tsinghua University, Beijing, 100084, China (e-mail: weiqi@tsinghua.edu.cn; quakexz@163.com; liujn156@163.com; wangh@tsinghua.edu.cn; yanghz@tsinghua.edu.cn).

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Digital Object Identifier 10.1109/TCSI.2014.2332248

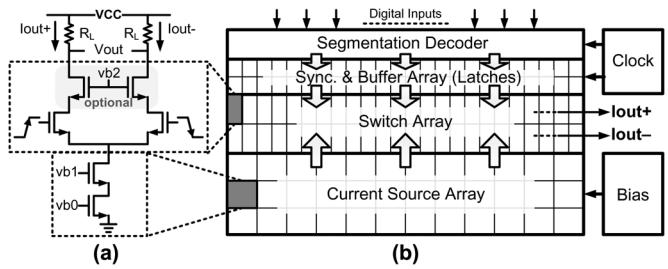

Fig. 1. Diagram of a traditional current-steering DAC with typical current source and switch units in (a) and a typical layout floorplan in (b).

The main contributions of this paper include two aspects:

(i) A complementary switched current source (CSCS) is proposed to mitigate the effect of code-dependent load variations. Different from traditional methods of simply increasing the output impedance of switched-on current routes, this approach improves the SFDR by reducing the output impedance mismatch of switched-on and switched-off current routes. Meanwhile, the SFDR degradation by the mismatch between the output impedances of switched-on and switched-off current routes is also analyzed in detail, which could be a design criterion for wide-band DACs.

(ii) Time-relaxed interleaving digital-random-return-to-zero (TRI-DRRZ) [24] is employed to suppress nonlinear distortions in the code-dependent switching glitches. In this paper, we provide detailed analysis and comparisons between TRI-DRRZ, non-return-to-zero (NRZ), and return-to-zero (RZ) techniques, showing the advancement of TRI-DRRZ in nonlinear harmonics suppression without tightening the settling-time requirement or attenuating the signal power.

To verify the proposed techniques, an experimental 14 bit 500 MS/s CMOS DAC was fabricated, with measured SFDR of 84.8 dB with an 11 MHz input signal and 73.5 dB at 244 MHz.

The rest of this paper is organized as follows. Section II and Section III describe the proposed CSCS and TRI-DRRZ approaches, respectively. The experimental 14 bit 500 MS/s DAC design is introduced in Section IV, and the measured results are shown and discussed in Section V. Finally, Section VI draws the conclusions.

II. Proposed CSCS

In this section, the proposed CSCS approach and comparisons with other recent techniques are presented, after a brief discussion of the output impedance requirements.

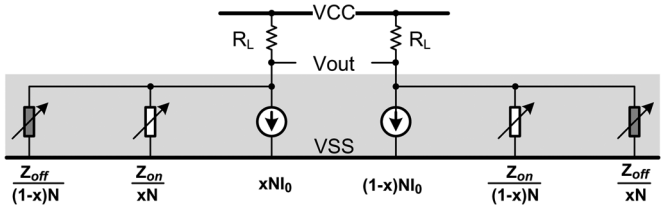

Fig. 2. Simplified model of the DAC with finite output impedance.

A. Theoretical Analysis of Output Impedance Requirements

As illustrated in Fig. 2, R_L is the external resistive load at each output of the DAC. N is the total number of current sources for a thermometer-decoded DAC. x $(0 < x < 1)$ is the full-range digital input code. I_0 is the current of the least significant bit (LSB). Z_{on} is the output impedance of a switched-on current route, and Z_{off} is that of a switched-off current route ($Z_{off} \gg Z_{on}$). As observed in Fig. 2, the finite output impedance of "on" and "off" current routes forms a code-dependent load in parallel with R_L to the DAC's current output. Such a code-dependent load behaves like a nonlinear current attenuator to the resistive load R_L. Assuming $Z_{on} \gg NR_L$, [34], [35] and later [2] give the SFDR of the differential output:

$$\text{SFDR} \approx \left(\frac{4Z_{eff}}{NR_L}\right)^2, \text{ with } Z_{eff} = \left(Z_{on}^{-1} - Z_{off}^{-1}\right)^{-1}. \quad (1)$$

To prevent SFDR deterioration caused by code-dependent load variations, most traditional techniques focus on increasing Z_{on} [1]–[3], [17]. For digital-to-analog conversions with SFDR >70 dB up to Giga-hertz, satisfying the output impedance requirement in (1) is challenging, even with elaborate circuits and layout designs [2], [17], [27].

B. Proposed CSCS Approach

The CSCS approach is proposed to make the mismatch between Z_{on} and Z_{off} towards zero, which is one effective way to increase Z_{eff} and SFDR. As shown in (1), Z_{eff} and $SFDR$ will increase if Z_{off} is lowered towards Z_{on}. In other words, CSCS makes the DAC's output impedance independent of the input code, so that the current to R_L is not attenuated code-dependently, leading to the harmonics suppression and SFDR increase. Making the output impedance independent of the input code is not a new idea: it was introduced in [36] for less integral nonlinearity (INL), and then discussed in [2], [34] on the on/off capacitive difference compensation for higher SFDR.

Our previous work in [25] focuses on this point, arriving at a conclusion illustrated in Fig. 3, where the SFDR versus Z_{on} with different mismatches between Z_{off} and Z_{on} are given. The curves in Fig. 3 confirm the effectiveness of making Z_{on} and Z_{off} equal. As an example, to achieve 80 dB SFDR, the Z_{on} requirement reduces from 10 MΩ under 100% mismatch to only 1.0 MΩ under 5% mismatch. This is of great significance for wide-bandwidth DAC design, because increasing the output impedance becomes challenging at high frequencies.

This paper proposes the CSCS unit to equalize Z_{off} and Z_{on}, as illustrated in Fig. 4. Compared with the traditional unit shown in Fig. 1, the difference is the additional complementary current branch composed of a cascode current source labeled as M0b and M1b, and two switches labeled as M2b and M3b. The sizes of M0b and M1b, are scaled from M0a and M1a according to

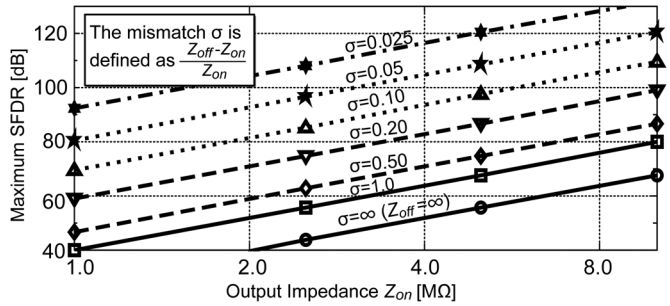

Fig. 3. SFDR versus LSB Z_{on} and mismatch σ for a 14 bit DAC with $R_L = 50\ \Omega$.

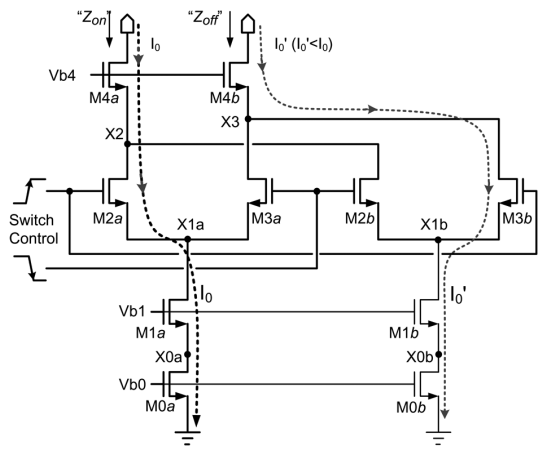

Fig. 4. Proposed CSCS unit.

the current ratio between the complementary current I_0' and the main current I_0. The sizes of M2a, M3a, M2b and M3b satisfy:

$$W_{2a} = W_{3a},\ W_{2b} = W_{3b},\ L_{2a} = L_{3a} = L_{2b} = L_{3b}. \quad (2)$$

All transistors work in the saturation region, except the two turned-off switches in the cut-off region. With the co-existence of I_0 and I_0' inside each CSCS unit, there is always one current path from each output node to the ground through a switch and a current source, no matter what the control signals are. Therefore, the two transistors M4a/M4b can always be biased in the saturation region, resulting in nearly the same capacitance at nodes X2 and X3, which is nearly independent of the switch control signals. As a result, the mismatch between Z_{on} and Z_{off} is reduced, and the SFDR increases with higher Z_{eff}.

It should be noted that Z_{eff} also depends on (a) the intrinsic gains of the transistors in the current routes, and (b) the complementary switch sizes. Therefore, further optimizations of the CSCS unit are indispensable for an optimum Z_{eff}.

C. CSCS Unit Optimizations

In the following discussions, it is assumed that M2a and M3b in Fig. 4 are switched on while M2b and M3a are switched off. Z_{on} and Z_{off} at high frequencies can be derived:

$$Z_{on}^{-1} \approx j\omega\left(C_{gd4a} + \frac{C_{X0a}}{A_{1a}A_{2a}A_{4a}} + \frac{C_{X1a}}{A_{2a}A_{4a}} + \frac{C_{X2}}{A_{4a}}\right), \quad (3)$$

$$Z_{off}^{-1} \approx j\omega\left(C_{gd4b} + \frac{C_{X0b}}{A_{1b}A_{2b}A_{4b}} + \frac{C_{X1b}}{A_{2b}A_{4b}} + \frac{C_{X3}}{A_{4b}}\right), \quad (4)$$

where A_{1a}, A_{2a} and A_{4a} are the intrinsic saturation gains, i.e., $g_m r_{ds}$, of M1a, M2a, and M4a, respectively; $C_{X0a}, C_{X1a}, \ldots$

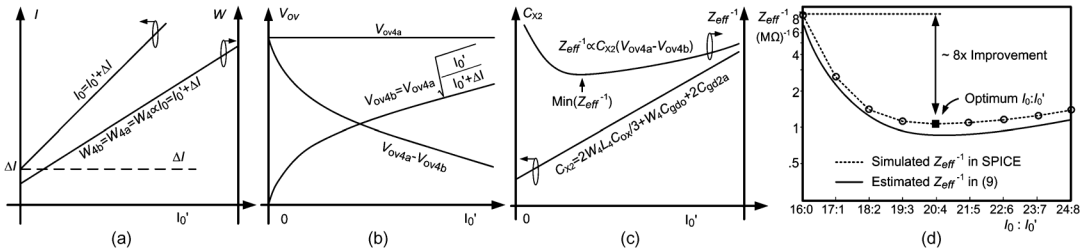

Fig. 5. I_0' optimizations of the proposed CSCS in Fig. 4 to maximize Z_{eff} with fixed L_4, V_{ov4a}, and ΔI ($\Delta I = I_0 - I_0'$). (a) Estimated linear relationships between I_0', I_0, and W_4. (b) Estimated relationships between I_0' and V_{ov4a}, V_{ov4b}, and $V_{ov4a} - V_{ov4b}$. (c) Estimated relationships between I_0' and C_{X2}, Z_{eff}^{-1}. (d) Z_{eff}^{-1} versus I_0'.

represent the capacitance at nodes $\mathrm{X0}a, \mathrm{X1}a, \ldots$, respectively. Z_{eff} turns out to be:

$$(j\omega Z_{eff})^{-1} \approx \underbrace{\left(\frac{C_{X0a}}{A_{1a}A_{2a}A_{4a}} - \frac{C_{X0b}}{A_{1b}A_{2b}A_{4b}}\right)}_{\Delta T1} + \underbrace{\left(\frac{C_{X1a}}{A_{2a}A_{4a}} - \frac{C_{X1b}}{A_{2b}A_{4b}}\right)}_{\Delta T2} + \underbrace{\left(\frac{C_{X2}}{A_{4a}} - \frac{C_{X3}}{A_{4b}}\right)}_{\Delta T3}. \quad (5)$$

C_{X0a} and C_{X1a} are usually larger than C_{X2} because of the large current source transistors for static current matching and long interconnection lines [2]. However, compared with $\Delta T3$, the capacitance effect of $\Delta T1$ and $\Delta T2$ in (5) is further suppressed by intrinsic gains of M1 and M2, i.e., $A_{1a}A_{2a}$ and $A_{1b}A_{2b}$, in a typical range of $10^2 \sim 10^3$. Thus, $\Delta T3$ usually dominates the output impedance at high frequencies.

In the proposed CSCS unit, C_{X2} is nearly the same as C_{X3}, and (5) could be simplified:

$$(j\omega Z_{eff})^{-1} \approx \frac{C_{X2}(V_{ov4a} - V_{ov4b})}{2V_E L_4}, \quad (6)$$

where V_E is the Early voltage, and V_{ov} is the over-drive voltage. A smaller transistor size is usually helpful for less capacitance and a larger Z_{eff} at high frequencies, as shown in (6). To obtain the largest Z_{eff}, the amount of I_0' and the complementary switch size also need further optimizations.

(i) Optimizations of I_0'.

In the CSCS unit, the effective current output is the difference between I_0 and I_0', i.e. $\Delta I = I_0 - I_0'$. Given ΔI fixed, I_0 and W_4 each has a linear relationship with I_0', as shown in Fig. 5(a), as does C_{X2} plotted in Fig. 5(c). As for $V_{ov4a} - V_{ov4b}$, the relationship with I_0' is more complex:

$$V_{ov4a} - V_{ov4b} = V_{ov4a} - V_{ov4a}\sqrt{\frac{I_0'}{I_0}} = V_{ov4a}\left(1 - \sqrt{\frac{I_0'}{I_0' + \Delta I}}\right). \quad (7)$$

As a result, the relationship between Z_{eff} and I_0' is derived:

$$(j\omega Z_{eff})^{-1} \propto (kI_0' + b)\left(1 - \sqrt{\frac{I_0'}{I_0' + \Delta I}}\right), \quad (8)$$

where k and b are constants. The curves of V_{ov4a}, V_{ov4b}, and $V_{ov4a} - V_{ov4b}$ are illustrated in Fig. 5(b). In Fig. 5(c), the minimum Z_{eff}^{-1} is presented. It should be noted that the optimum I_0' in (8) varies with both transistor operating points and the process characterizations. A simulated curve Z_{eff}^{-1} at 500 MHz is plotted in Fig. 5(d), which proves the above conclusions. The simulation results also demonstrate $\sim 8\times$ improvement of Z_{eff} after using the CSCS approach.

(ii) Optimizations of the complementary switch size.

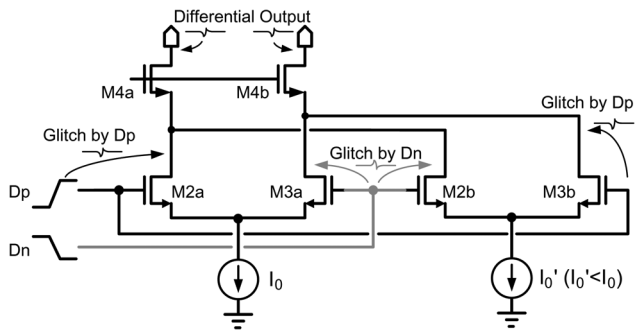

Fig. 6. Differential cancellation of the glitches by the CSCS unit.

In typical designs, the capacitance effect of $\Delta T1$ and $\Delta T2$ in (5) is suppressed significantly by the intrinsic gains of M1–M2. In designs using a low supply voltage or deep sub-micron CMOS technologies, the intrinsic gain is lowered [27], so the proportion of $\Delta T1$ and $\Delta T2$ in Z_{eff}^{-1} increases. Similar to the derivations of $\Delta T3$, $\Delta T2$ can be derived:

$$\Delta T2 \approx \frac{C_{X1a}V_{ov2a}V_{ov4a} - C_{X1b}V_{ov3b}V_{ov4b}}{4V_E^2 L_{2a}L_4}. \quad (9)$$

For a smaller $\Delta T2$, the switch size should be small for less capacitance. More importantly, the ratio between W_{2a} and W_{2b} can also be optimized. If W_{2a}/W_{2b} equals I_0/I_0', i.e., $W_{2a}/W_{2b} = I_0/I_0' = C_{X1a}/C_{X1b}$, then $C_{X1a}V_{ov2a}V_{ov4a}$ is larger than $C_{X1b}V_{ov3b}V_{ov4b}$ in (10), resulting in a non-zero $\Delta T2$, ($V_{ov2a} = V_{ov3b}$, in this case). If W_{2b} increases, the difference between $C_{X1a}V_{ov2a}V_{ov4a}$ and $C_{X1b}V_{ov3b}V_{ov4b}$ can be reduced, resulting in a smaller $\Delta T2$.

Another feature of CSCS is the capability of canceling the glitches due to switch coupling. As illustrated in Fig. 6, the switching by the control signals at the complementary current route forms a glitch at the output, just opposite to the glitch induced by the main current route. For symmetrical control signals, the best glitch cancellation tends to use complementary switches (M2b and M3b in Fig. 6) with the same size as the main switches (M2a and M3a in Fig. 6).

D. Comparisons With Other Techniques and Summary

Previous work of a current source and switch unit was proposed in [25], where the optimizations of I_0' and the complementary switch size were not mentioned. Another type of CSCS unit without M4a/M4b was also proposed in [26], yielding a smaller Z_{eff} and lower SFDR; in this case, it is the same as the unit proposed by [25]. In this paper, further optimizations of the design strategy in CSCS units are proposed for the first time for a higher Z_{eff}.

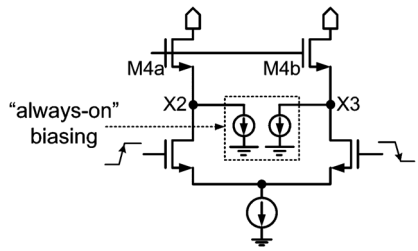

Fig. 7. "Always-on" biasing [2], [39].

Another technique in a similar configuration (without $\mathrm{M}4a$ and $\mathrm{M}4b$) is proposed in [28], using an auxiliary current path with dummy capacitance in each current unit. Its purpose is high power-supply rejection. Neither theory nor simulation on the distortions caused by finite output impedance is provided. In fact, the auxiliary current might also help to increase Z_{eff}, using the same optimizations in this paper.

It should also be noted that the "always-on" biasing was proposed in [2], [39], as illustrated in Fig. 7. By adding two constant current sources with a value of 1%∼2% of the main current source to keep $\mathrm{M}4a$ and $\mathrm{M}4b$ in saturation, the capacitance at the nodes X2 and X3 in Fig. 7 is nearly the same. However, it was not revealed by [2], [39] but clarified in this paper, that the intrinsic gain difference of $\mathrm{M}4a$ and $\mathrm{M}4b$ also significantly affects the SFDR through the terms A_{4a} and A_{4b} in (5–7). Additional constant biasing current of only 1%∼2% of the main current inevitably results in a significant intrinsic gain difference between $\mathrm{M}4a$ and $\mathrm{M}4b$. Therefore, the method aiming only at the equal capacitance at nodes X2 and X3 without optimizations of I_0' and the complementary switch size, does not yield the highest Z_{eff} for the DAC. This conclusion has been confirmed by theoretical and simulated results of the proposed CSCS technique in this section.

From another point of view, if the "always-on" biasing employs the CSCS design optimizations, it will yield the same Z_{eff}. However, it should be noted that the "always-on" biasing is not able to suppress the glitches at the output, which is another inherent feature of the proposed CSCS approach (see Fig. 6).

The cost of the proposed CSCS includes more power and silicon area. The power increase comes from the additional static current to the DAC's output and the extra power to drive additional switches. Taking $I_0 : I_0' = 5 : 1$ as an example, such power and area increase is as high as 50%. It has been revealed that the INL due to random matching errors is roughly proportional to the root of the total number of current sources [31]. Such increased number and silicon area of the CSCS current source array yields larger random and linear systematic matching errors by roughly $(1+50\%)^{0.5}-1 \approx 23\%$ and ∼50%, respectively [13]–[15], [31]. If the current amplitude matching requirement is essential, calibration techniques [10], [37] are a viable choice for higher static accuracy in collaboration with the CSCS approach. At last, more switches to drive tends to increase the timing errors [16], [30], [35].

The complementary CSCS current forms a common-mode DC current in the DAC output. In typical transformer-coupled differential-to-single conversion for the DAC output, this common-mode DC current flows through the transformer and consumes no voltage headroom. Fig. 8 gives such a typical conversion diagram [1], [8], [18].

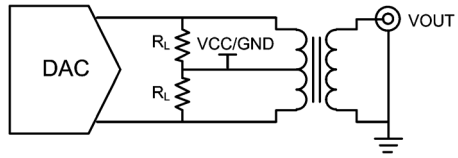

Fig. 8. Transformer-coupled differential-to-single conversion diagram.

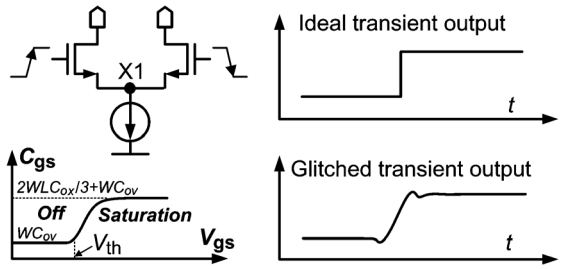

Fig. 9. Nonlinear code-dependent switching in the current routes.

Despite of more power, area, current matching errors and timing errors, the CSCS approach is still effective for higher output impedance. In wide-bandwidth high-dynamic-range DAC designs, where finite output impedance due to high frequency becomes the bottleneck, the CSCS approach exhibits the potential for wider bandwidth and higher SFDR, fitting well with the CMOS technologies scaling and lower supply trend.

III. Proposed TRI-DRRZ

To achieve a high SFDR, special measures have to be taken to suppress nonlinear distortions in code-dependent switching glitches. This section describes the proposed TRI-DRRZ approach in detail and compares it with traditional solutions.

A. Nonlinear Code-Dependent Switching Glitches

In current-steering DACs, the change of switch control causes glitches in the current route, as shown in Fig. 9. The mechanism of the glitches is rather complex and determined by many factors [1], [5], [16], [29], [30]. One such factor is the charge transfer of node X1 in Fig. 9 caused by the mismatch between the tail current and the total current of the switches when switching. Another factor is the timing mismatches of the switching activities, mainly due to switching load mismatches, switch driving ability mismatches, and clock distribution timing skews. These factors cause code-dependent glitches in the current and nonlinear harmonics in the spectrum, deteriorating the SFDR significantly at high frequencies.

B. Traditional Solutions to Nonlinear Switching Glitches

Traditional solutions mainly include two types. One type focuses on reducing the glitch energy, through lowering the control signal swing [6], [10], RZ to isolate the output when switching [7], [20]–[22], adjusting the crossover point of the control signals [5], and reducing timing mismatch between parallel current routes [16], [30], [33], [35]. Dynamic-mismatch mapping in [30], [33] optimizes the cell-selecting sequence to minimize both amplitude and timing mismatch errors without increasing the noise floor, yielding SFDR $>$78 dB and noise spectral density (NSD) $<$ −163 dB across the Nyquist band at 200 MS/s [30]. The other type tries to turn the glitches due to switching timing errors and amplitude mismatch errors to

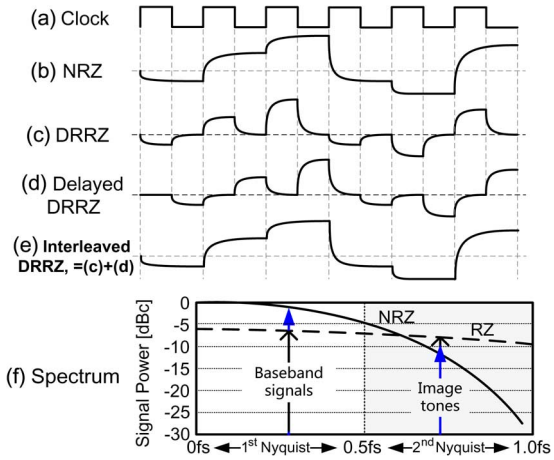

Fig. 10. NRZ, DRRZ, and interleaved DRRZ transient waveforms comparisons in (a)–(e) and output spectrum comparisons in (f).

be code-independent, through ways of random switching techniques [8], or quad-switching techniques for constant switching in each clock cycle [4], [5], [19], [23].

DRRZ in [1] and DMRZ in [8], utilize both dynamic random switching and RZ techniques to be the first CMOS DAC with $>$70 dB SFDR up to 500 MHz and 800 MHz, respectively. Fig. 10 illustrates the DRRZ output waveforms. When the clock goes high, the DAC gives NRZ output under the control of traditional segmentation decoder; when the clock goes low, DRRZ resets the switch control signals, so that the DAC's output current is divided equally, and randomly, to the positive and negative ports. An equal current division results in differential return-to-zero behavior, and the random division makes the current switching code-independent. In other words, the switching glitches result in noises instead of large distortions in the spectrum. As for DMRZ, the randomization is not inserted into the RZ operations, but into the NRZ operations in high clock phases through dynamic random switching.

DRRZ and DMRZ need not change analog blocks while suppressing nonlinear distortions, but have serious problems:

(i) The tight timing diagram in RZ operations requires that the switching settles within half a clock period, rather than one clock period in NRZ DACs. This effect makes a high-speed DAC much more difficult to design.

(ii) As illustrated in Fig. 10(f), compared with NRZ DACs, the extra signal energy loss due to the RZ operations is 6 dB at DC and 3 dB at the Nyquist fs/2 [20], [21], where fs is the sampling frequency. More importantly, the lowpass filter of the DAC's output is more challenging to design because of higher image tones in the 2nd Nyquist zone [21]. Lower signal power and higher image tones limit the baseband applications [22].

The problems in (ii) can be compensated by interleaving two RZ schemes connected in parallel, as illustrated in Fig. 10(e), each operating in an opposite clock phase [22], [23]. The cost is doubled power and chip area. However, the settling-time is not relaxed because each parallel path remains unchanged.

C. Proposed TRI-DRRZ Approach

In order to solve the problems of DRRZ/DMRZ and further improve the nonlinear harmonics suppression, TRI-DRRZ is proposed, as illustrated in Fig. 11. It uses a pseudo random

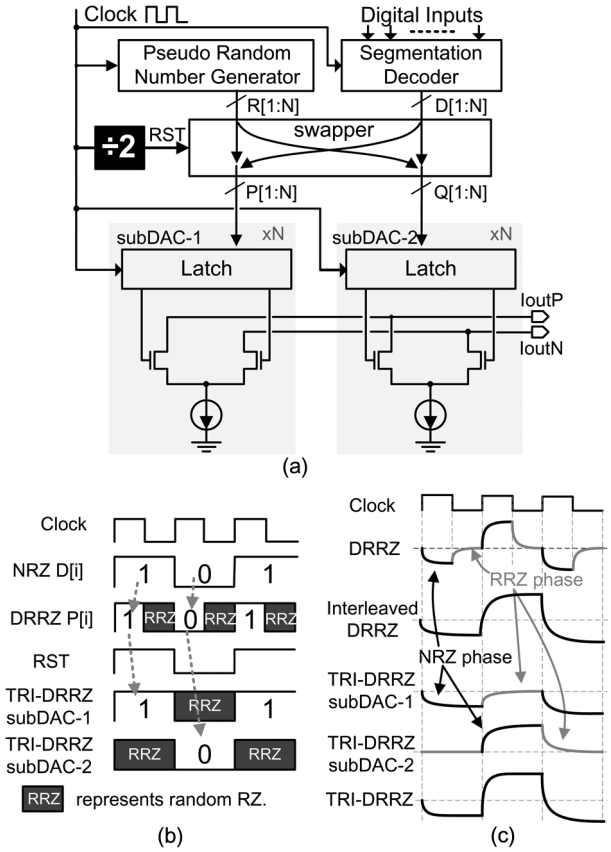

Fig. 11. Proposed TRI-DRRZ approach. (a) TRI-DRRZ function diagram. (b) Control signals inside the TRI-DRRZ diagram. (c) Output of TRI-DRRZ compared with DRRZ, and interleaved DRRZ.

number generator (PRNG) and two sub DACs, i.e. subDAC-1 and subDAC-2, controlled by the swapper indicator RST ($\mathrm{RST} = \mathrm{CLK} \div 2$). When RST is high, subDAC-1 gives an NRZ output under the control of the segmentation decoder, and subDAC-2 returns to zero through random and equal current division as DRRZ. When RST goes low, subDAC-1 and subDAC-2 interchange actions. Fig. 11 also compares the waveforms of DRRZ, interleaved DRRZ, and TRI-DRRZ.

The TRI-DRRZ evolves from DRRZ, but has essential advantages after the evolvement, including the relaxation of settling-time requirements, the increase of signal energy, more suppression of image tones, and higher SFDR.

First, the settling-time problem is relaxed. As shown in Fig. 11, the switching of a current route in DRRZ and dual RZ schemes in [22], [23] changes twice in a clock cycle; In TRI-DRRZ, it reduces to once a clock cycle, allowing twice the time for signal settling. As a result, the settling-time design of a high-speed RZ DAC becomes much easier in TRI-DRRZ. The term "relaxed" in TRI-DRRZ comes from this phenomenon.

Second, the signal energy loss and image tone suppression problem in the 2nd Nyquist spectrum region due to the RZ operations in DRRZ is also mitigated. The differential output range of TRI-DRRZ is the same as NRZ. In this case, it is also the same as the interleaved DRRZ in Fig. 10(e) and other dual RZ schemes in [22], [23].

Third, the SFDR is higher. As illustrated in Fig. 11(b), (c), the total times of randomized switching and corresponding switching glitches in TRI-DRRZ are the same as DRRZ, but the signal power of TRI-DRRZ is higher. Therefore, TRI-DRRZ

TABLE I
COMPARISONS BETWEEN THE PROPOSED TRI-DRRZ AND OTHERS

Specifications	NRZ	DRRZ /DMRZ	Interleaved DRRZ/DMRZ	**TRI-DRRZ**
Settling-time requirement	low	high	high	**low**
Output signal power	large	small	large	**large**
Image suppression [a]	high	low	high	**high**
Switch driving power	small	medium	large	**medium**
Power efficiency [b]	high	low	low	**medium**
SFDR [c]	low	medium	high	**high**
Chip area	small	small	large	**large**

[a] The image represents the signal image in the 2nd Nyquist spectrum region;
[b] Power efficiency = {signal power}/{DAC power};
[c] SFDR here is subject to the signal power and nonlinear switching distortions.

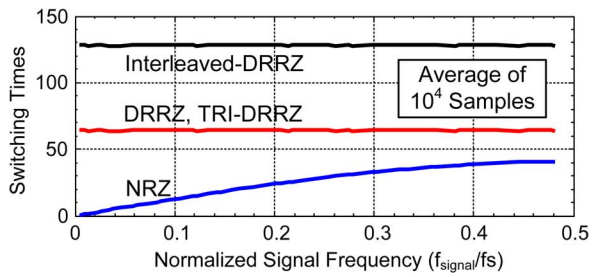

Fig. 12. Switching times per cycle in a 6-bit fully thermometer-decoded DAC.

yields a higher SFDR than DRRZ by increasing the signal power of DRRZ without increasing noise floor or distortions. It is also important to note that the extra switches required by TRI-DRRZ operations result in a larger timing error of the sampling clock edge [16], [30], [35]. Therefore, careful sample timing design is required to satisfy the timing requirements.

The idea of time-relaxed interleaving could also be applied to other RZ DACs in [8], [21]–[23], for relaxed settling-time requirement, larger signal power, and higher SFDR. Table I summarizes the performance comparison between NRZ, DRRZ/DMRZ, the interleaved DRRZ/DMRZ, and TRI-DRRZ. It is important to note that the conclusions in Table I are valid only based on the same DAC prototype, i.e. with the same design architecture and specifications like resolution, segmentation, sampling rate, process, latch, switch and current source biasing, etc. The settling-time requirement, output signal power, and the image signal suppression of these techniques have been discussed above.

In Table I, the DAC switch driving power is generally proportional to the times of switching activities inside the DAC, depending on the number of switches and the possibility of ON-OFF state interchanging. Fig. 12 shows the average times of switching per clock cycle in a 6-bit thermometer-decoded DAC in different schemes. The average switching times in TRI-DRRZ and DRRZ are the same, and are 60% larger than NRZ at frequencies near fs/2. As the signal frequency drops, the switching activity of NRZ significantly cools down, but TRI-DRRZ and DRRZ maintain unchanged. The interleaved—DRRZ has twice switching times of DRRZ/TRI-DRRZ, and thus consumes the highest switch driving power.

In Table I, the power efficiency is defined as the ratio of the output signal power to the entire DAC power. TRI-DRRZ has lower power efficiency than NRZ because of the same signal power but larger DAC power due to heavier switch driving and the additional PRNG block. However, TRI-DRRZ outperforms DRRZ and the interleaved DRRZ in power efficiency because of larger signal power than DRRZ, and less switch driving power than the interleaved DRRZ, respectively.

In Table I, the SFDR comparisons between NRZ, DRRZ, and TRI-DRRZ have been discussed above. In terms of the comparison between TRI-DRRZ and the interleaved DRRZ, their SFDR is equivalent because the output signal power is the same, and the code-dependent switching glitches are both randomized so as not to limit the SFDR (under the condition that both DACs settle). However, it is noted that TRI-DRRZ potentially has less impact on the noise floor than the interleaved-DRRZ due to halved number of sample activities.

Table I also shows that the interleaved DRRZ and TRI-DRRZ occupy the largest chip area due to a second sub DAC. The increased area of the current sources yields larger random and systematic gradient mismatches [13]–[15]. In the proposed DAC implementations, current source unit sizing to control the random mismatch and a biasing technique to minimize the gradient mismatch will be applied in Section IV.

IV. CHIP IMPLEMENTATION

To verify the proposed CSCS and TRI-DRRZ solution, a 14 bit 500 MS/s DAC in 0.13 μm CMOS process is implemented. This section gives the design details, including the DAC architecture, the CSCS realizations, the TRI-DRRZ realizations, a new fast latch, and layout details.

A. DAC Architecture

The DAC has a power supply of 1.2 V(digital)/2.5 V(analog). The full-scale current output is 16 mA, and the differential load is 50 Ω. The DAC architecture is shown in Fig. 13, containing a current source and switch unit array, a latch array, a clock generation block, and a TRI-DRRZ decoder. The TRI-DRRZ decoder integrates the segmentation decoder, RZ decoder, and the swapper together. The 14 bit DAC is segmented into 6 unary-weighted most significant bits (MSB), 4 unary-weighted upper-significant bits (USB), and 4 binary-weighted LSB. Such segmentation is mainly based on the trade-off between the dynamic linearity and the power and area of the digital decoder: A large MSB segment helps for high dynamic linearity but also introduces larger power and chip area of the binary-to-thermometer decoder [31].

B. CSCS Unit Realizations

The current source and switch units of MSB and USB are the same as Fig. 4, using cascoded NMOS current sources. For an MSB current source, the main current I_0 is 320 μA (consisting of 20 parallel 16 μA current units), and the complementary current I_0' is 64 μA (consisting of 4 parallel 16 μA current units), forming a differential current output of 256 μA. The ratio of $I_0 : I_0' = 5$ is for the purpose of a large Z_{eff}, as shown in the simulation results in Fig. 5(d). For a USB current source, the main and complementary current is 32 μA and 16 μA, respectively, forming a differential current of 16 μA. The ratio $I_0 : I_0'$ of USB current sources is not 5:1 for the purpose of directly reusing the same 16 μA current unit in MSB current sources for better matching. One such 16 μA current unit is divided into 5 independent currents: 8 μA, 4 μA, 2 μA, 1 μA, and 1 μA for four LSB and one dummy current sources in the LSB segment

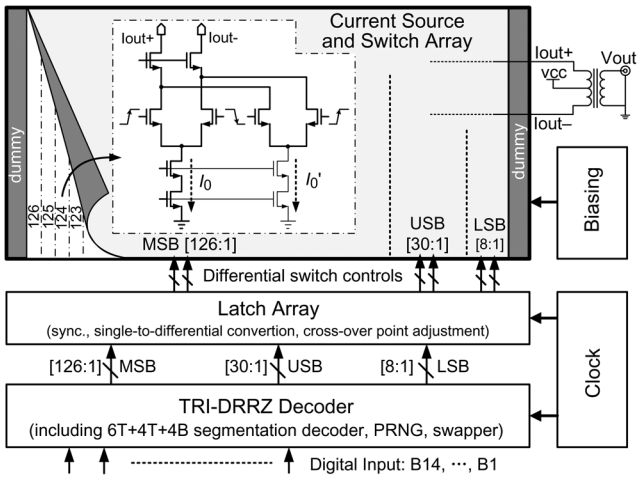

Fig. 13. Architecture of the 14 bit 500 MS/s DAC.

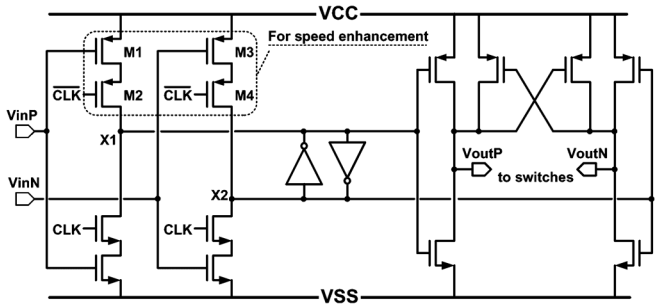

Fig. 14. High-speed latch.

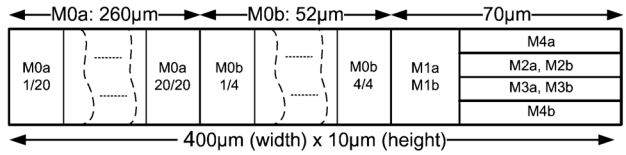

Fig. 15. Floorplan of the current source and switch unit in Fig. 4 in a strip.

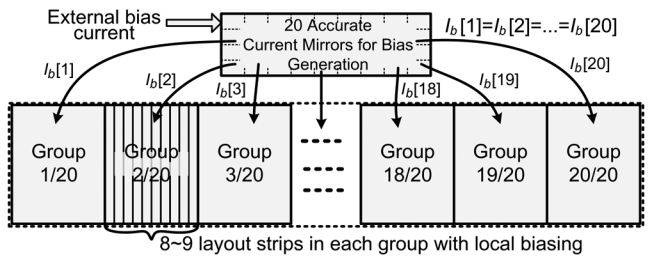

Fig. 16. Biasing scheme to mitigate gradient matching errors.

for current matching. The CSCS approach is not applied to the LSB current sources because the finite output impedance of one LSB current source contributes to only a small part of nonlinear distortions.

Considering both CSCS and TRI-DRRZ introduce more number of current sources, sizing of the current sources is important for keeping INL due to the random mismatches under control. The yield model in [40] is adopted to determine the required sigma(I)/I of a current source for a targeted INL yield of 90%. The unit current source area is then derived based on the matching model from [11].

C. TRI-DRRZ Realizations

The two identical sub DACs in Fig. 11(a) are realized with the same circuit and layout, resulting in twice the number of latches, switches, and current sources. When one sub DAC enters the RZ phase, the PRNG randomly selects 32 MSB current sources to be switched to the DAC's positive output port, while the left current sources are switched to the DAC's negative output port. Such configuration produces an almost zero differential output, with one LSB DC offset. This constant slight offset has very little effect on the dynamic performance.

D. Fast Latch

Fig. 14 shows the high-speed latch in the DAC. Its differential outputs, i.e., VoutP and VoutN, are used directly to control the switches of the current routes. It is revealed in [2] that fast transitions of switch control signals reduce the effects of the switch driving mismatch and the clock jitter. By adding transistors M1–M4, the low-to-high transition of the voltage at the nodes X1 and X2 in Fig. 14 is significantly accelerated. All MSB, USB, and LSB employ the same latch for the same driving ability, and dummy switches are added to USB and LSB current routes for the same driving load to the latch.

E. Layout Implementations

Fig. 15 shows the layout of the current source and switch unit for an MSB unit. It has an outline of $\sim 400\ \mu\text{m} \times \sim 10\ \mu\text{m}$. In the MSB segment of one sub DAC, there are $2^6 - 1 = 63$ such strips. For the entire DAC, the total number is 164, including the USB and LSB segments. As explained in Section II, reducing the parasitic capacitance in the layout is critical to increase the output impedance and reduce the effect of the code-dependent load variations. As a result, in Fig. 15, the current source and the switch are placed closely in every strip for minimum parasitic capacitance of the interconnection lines. Therefore, all the current source and switch units are placed in parallel in one direction, forming a $450\ \mu\text{m} \times 1700\ \mu\text{m}$ array. This layout pattern is similar to [2] and different from other traditional two-dimensional matrix-style placements.

The disadvantage of this floorplan is the emerging problem of gradient matching errors in the current source array, especially when TRI-DRRZ is applied. Gradient matching errors are mainly a result of fabrication technology non-idealities, such as doping gradients and oxide thickness gradients [13]–[15]. Temperature gradients, package stress, and the IR-drop also contribute to some gradient matching errors [13]–[15]. The biasing technique in [31] is applied to solve the gradient matching errors between distant current sources. As illustrated in Fig. 16, the current source array is partitioned into 20 groups. The size of a group is about $85\ \mu\text{m} \times 400\ \mu\text{m}$. All the current sources in a group share the same biasing gate voltages generated locally inside the group from an accurate biasing current $I_b[i]$, $i = 1, 2, \ldots 20$. Because the maximum distance between any two current sources in a group is less than 80 μm, the gradient error is tightly constrained. Outside the current source array, 20 current mirrors generate the required accurate biasing currents $I_b[i]$, $i = 1, 2, \ldots 20$, for the 20 groups. Because the biasing currents for all the groups are well matched, and all the current sources inside a local group are also well matched, the current sources of the entire array are well matched.

Fig. 17 shows the chip photograph of the fabricated DAC in 0.13 μm 1P8M CMOS process. The DAC layout is designed

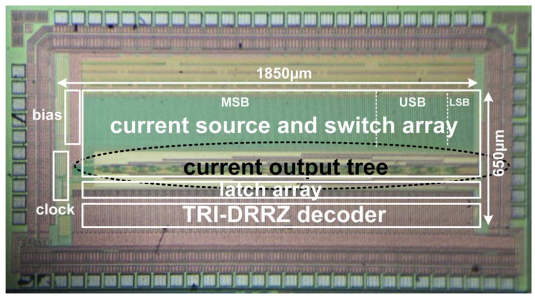

Fig. 17. Micrograph of the fabricated DAC.

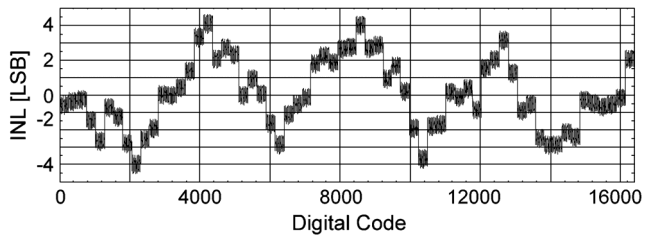

Fig. 18. Measured INL performance of the 14 bit DAC.

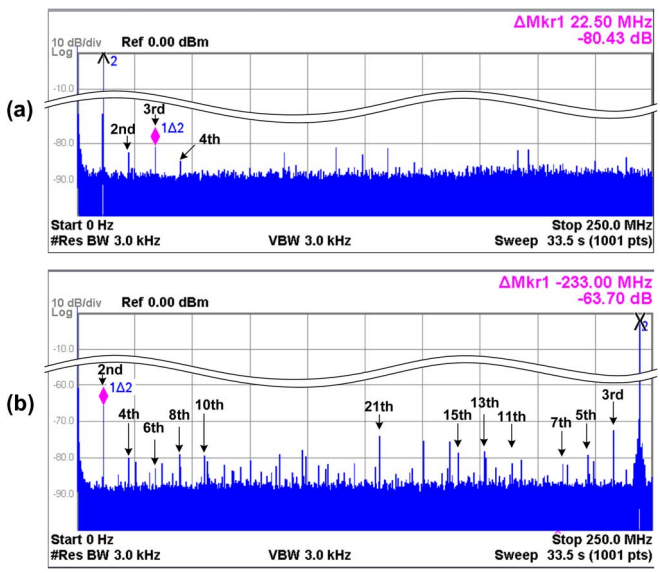

Fig. 19. Measured spectrum with CSCS on and TRI-DRRZ off at (a) 11 MHz and (b) 244 MHz input.

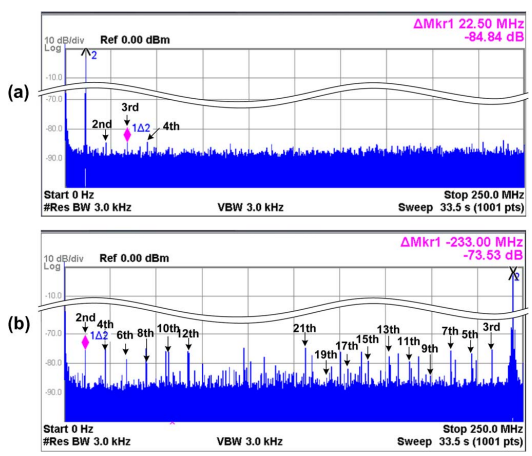

Fig. 20. Measured spectrum with CSCS and TRI-DRRZ on at (a) 11 MHz and (b) 244 MHz input.

manually. The core occupies an area of $1.85 \times 0.65\ \mathrm{mm}^2$, and the entire chip size is $2.3 \times 1.4\ \mathrm{mm}^2$.

V. Experimental Results

The fabricated DAC is mounted directly on the copper surface of the testing board. The dynamic measurement setup is similar to Fig. 8, with the two $\mathrm{R_L}$ resistors removed for higher signal power. The clock and parallel digital inputs of the DAC are generated by Agilent Parbert 81250. The analog output of the DAC is synthesized by Agilent N9020 spectrum analyzer after differential-to-single conversion by a transformer. This transformer has an impedance ratio of 1:1, and its center tap is connected to a 2.5 V power supply. Because the full-scale current output of the DAC is 16 mA and the load is 50 Ω by the spectrum analyzer, the DAC's output has a $0.8\mathrm{V_{ppd}}$ swing.

Fig. 18 shows the measured INL curve of the 14 bit DAC after correcting the offset and gain error using linear least-squares estimation techniques. The INL measurement is carried out with CSCS on and TRI-DRRZ off. The yielded INL/DNL is 4.5/2.5 LSB, respectively, which is far from the 14 bit resolution accuracy. Several chip samples have been tested and their INL performance is similar. The dominating factors that limit the INL performance are probably the systematic matching errors, because all three tested chip samples have similar INL curve shapes. As discussed in Section II and III, both CSCS and TRI-DRRZ techniques require more current source area, leading to a $3\times$ total area, and consequently, larger INL due to the systematic gradient errors even if the biasing technique in [31] is employed. Therefore, a more appropriate way to higher accuracy might be calibration [10], [37].

Fig. 19 gives the measured SFDR with a signal-tone output from the DAC at 500 MS/s sampling rate with CSCS on and TRI-DRRZ off. An 11 MHz signal spectrum is shown in Fig. 19 with 80.4 dB SFDR dominated by the 3rd order harmonic, and 244 MHz signal with 63.7 dB SFDR dominated by the 2nd order harmonic. As the frequency increases to the Nyquist, the SFDR degrades. Due to the compact layout for less parasitics, no CSCS disable option is provided in this design. As a result, it is implied that CSCS is on for all measurements. Considering the current source array area is much larger than [1], [2], [8], more parasitic capacitances exist in this design, leading to a lower output impedance. The decreasing slope of SFDR in 100∼250 MHz, however, is far away from the -40 dB/decade slope by (1). To some extent, this could be explained by the mitigation function of CSCS on the finite output impedance effect.

After enabling TRI-DRRZ, the measured signal-tone spectra are demonstrated in Fig. 20, with SFDR increases from 80.4 dB to 84.8 dB at 11 MHz signal frequency, and 63.7 dB to 73.5 dB at 244 MHz signal frequency. The 2nd and 3rd order harmonics are still dominating the SFDR, but lower in energy than those in Fig. 19 without TRI-DRRZ. The SFDR improvement by TRI-DRRZ is 4.4 dB at 11 MHz and around 10 dB for signal frequencies higher than 100 MHz. Fig. 21 shows the measured SFDR at 500 MS/s versus the signal frequency. At low frequencies, the switching activity is infrequent, leading to less distortion and less significant SFDR improvement by TRI-DRRZ. After enabling TRI-DRRZ, the SFDR increases to $>$73.5 dB across the entire Nyquist band.

It is also noticed that, compared with the 11 MHz signal spectrum, more tones above the noise floor appear in the 244 MHz signal spectrum. Some tones could be recognized as harmonic tones, as labeled in Fig. 19 and Fig. 20, while others are obscure to identify. In post-layout simulations, in which the digital

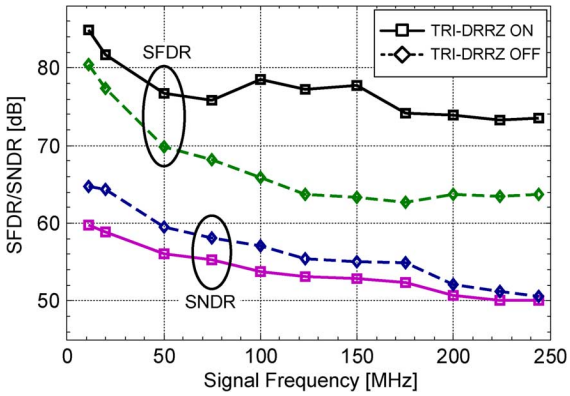

Fig. 21. Measured SFDR and SNDR versus the signal frequency.

input signal is ideal and no noise is applied, harmonics with an order higher than 4 are nearly unobservable. It is possible that the DAC core generates such tones, and a more probable course is the signal integrity problem of the single-ended full-swing CMOS parallel digital input codes of the DAC, which inevitably increases the bit error rate at higher signal frequencies. One phenomenon supporting this speculation is that when slightly delaying the sampling time of the digital input code by 0.1∼0.2 ns in the measurements, the energy of those tones change significantly (while harmonics are still dominating the SFDR). If those tones are generated inside the DAC core with correctly sampled digital input codes, the energy of those tones tend not to change. Another indirect proof is one inherent property of TRI-DRRZ that the total switching times in one clock cycle does not increase at higher signal frequencies, as discussed in Section III. Such a property suggests that those tones at high frequency are probably due to peripheral factors. Thus, it is recommended to employ low-error-rate I/O like low-voltage differential-signaling (LVDS) for high-speed DACs [38].

Signal-to-noise-and-distortion ratio (SNDR) is another key parameter to describe the dynamic performance of a DAC. It is determined by total harmonic distortion (THD) energy and NSD. For DACs employing techniques like TRI-DRRZ with frequent random switching activities, extra noise appears in the output spectrum, which lowers SNDR. Fig. 21 also shows the measured SNDR at 500 MS/s versus the signal frequency. Because NSD does not take harmonic performance into account, and that some tones in the high frequency output spectra are hard to identify as harmonics or noise tones, SNDR is measured instead of NSD. After enabling TRI-DRRZ, the measured SNDR drops significantly by ∼5 dB at low signal frequencies, and less significantly at high frequencies. A smaller difference observed at high signal frequencies may be the result of (a) less difference of switching activities between TRI-DRRZ and NRZ, as shown in Fig. 12, and (b) large power of various tones above the noise floor, as discussed above.

Third order intermodulation distortions (IMD3) are also measured. Fig. 22 shows the measured two-tone spectrum near 180 MHz sampled at 500 MS/s, with an IMD3 of −77.0 dB. The IMD3 of different signal frequencies at 500 MS/s are plotted in Fig. 23, better than −77.0 dB in the Nyquist band.

Fig. 24 plots the SFDR curves of this DAC and recently published CMOS DACs with ≥400 MS/s sampling rate and ≥12 bit resolution. Meanwhile, Table II shows the comparisons of these DACs. Although the sampling rate of this design is lower than

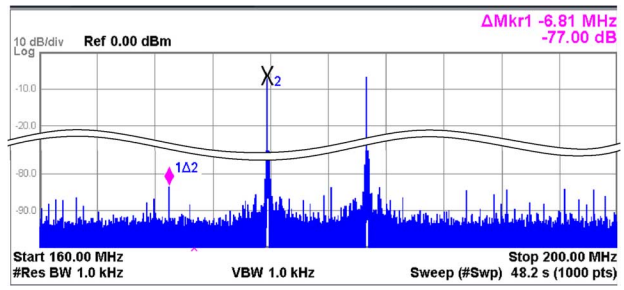

Fig. 22. Two-tone measurement centered around 180 MHz.

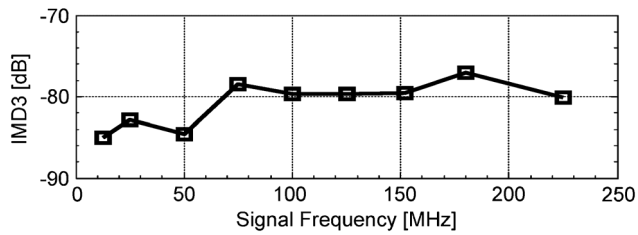

Fig. 23. Two-tone measurement IMD3 versus the signal frequency.

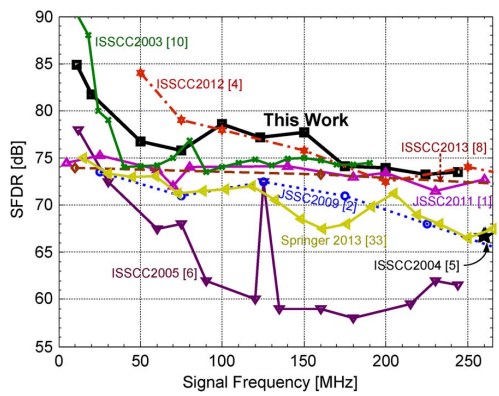

Fig. 24. SFDR performance comparisons.

[1], [2], [4], [8], [33], the SFDR of this work is higher than [1], [2], [6], [8], [33] within the entire Nyquist band. Considering the third-order distortion is generally proportional to the square of the signal amplitude [2], the SFDR of this work is more pronounced than [1], [8]. Compared with [4] which uses a mixed −1.5/1.8 V power supply, this work needs no negative power supply and occupies much less chip area. Compared with the calibrated DAC in [10], the SFDR performance of this work is similar, with the exception under low-frequency input where the SFDR is limited by the static matching linearity.

There are several types of figure of merit (FOM) for comprehensively evaluating a fast DAC, as summarized in [8], [29]. Considering the sampling rate fs, SFDR at a low signal frequency $SFDR_{LF}$, SFDR near the Nyquist $SFDR_{fs/2}$, the signal power P_{sig}, and the DAC power consumption P_{DAC}, [1], [8], [29], [32] give the FOM as

$$\text{FOM} = 2^{\frac{SFDR_{LF}-1.76}{6.02}} \times 2^{\frac{SFDR_{fs/2}-1.76}{6.02}} \times fs \Big/ (P_{DAC} - P_{sig}). \tag{10}$$

A higher FOM in (10) implies higher power efficiency. Note that such FOM comparisons with widely-varied sampling rate might not be fair for high sampling rate DACs, since $SFDR_{fs/2}$ tends to deteriorate with low output impedance. The FOM of this design is 9.23×10^4 Hz/mW, higher than [1], [2], [4], [6], [33].

TABLE II
COMPARISONS BETWEEN RECENTLY PUBLISHED $\geq$400 Ms/S, $\geq$12 BIT CMOS DACs

Specifications	This work	[1] JSSC2011	[2] JSSC2009	[4] ISSCC2012	[6] ISSCC2005	[8] ISSCC2013	[10] ISSCC2003	[33] Springer2013
Technology (nm)	**130**	90	65	180	180	40	250	140
Core area (mm^2)	**1.20**	0.825	0.31	4.0	1.13	0.016	~1.95	1.10
Supply (V)	**1.2/2.5**	1.2/2.5	1.0/2.5	-1.5/1.8	1.0/1.8	1.2	2.5/3.3	1.2/1.8
DAC power (mW)	**299**	128	188	600	216	40	400	260
Sampling rate (GS/s)	**0.50**	1.25	2.9	3~6	0.50	1.6	0.40	0.65
Resolution (bits)	**14**	12	12	14	12	12	16	14
INL/DNL (LSB)	**4.5/2.5**	1.2/0.51	0.5/0.3	–	1.0/0.6	–	0.65/0.25	2.4/1.7
Calibration	**No**	Yes	No	–	No	No	Yes	No
Full-scale current (mA)	**16**	16	50	20	15	16	–	20
$SFDR_{LF}$ (dB)	**84.8**	75	74	84.5	80	74.0	98	>73
$SFDR_{fs/2}$ (dB)	**73.5**	66	52	52	60	70.3	73	>65
SNDR (dB)	**>50**	–	–	–	–	–	–	–
NSD (dBm/Hz)	–	–	–	–	–	-151 @0.8GHz	<-160	–
THD	–	–	–	–	–	–	–	<-63dB
IMD3 (dB)	**<-77.0**	–	-60 @1GHz	-70 @0.5GHz	–	-70 @0.8GHz	<-80	–
FOM in (11) (10^4Hz/mw)	**9.23**	7.32	2.09	4.48	1.56	46	38	2.24

VI. CONCLUSION

A 14 bit 500 MS/s current-steering CMOS DAC has been presented with $>$73.5 dB SFDR and ≤ -77.0 dB IMD3 in the entire Nyquist band. The measured results were obtained while driving a 50 Ω spectrum analyzer with a signal amplitude of 0.8 V_{ppd}. The performance has verified the effectiveness of the proposed CSCS and TRI-DRRZ approaches for mitigating the nonlinear distortions caused by code-dependent load variations and code-dependent switching glitches. The current source biasing technique and the high-speed latch also play an important role in static linearity and fast conversion, respectively, in the DAC.

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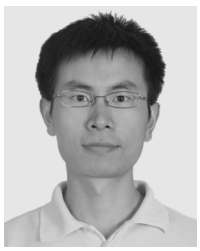
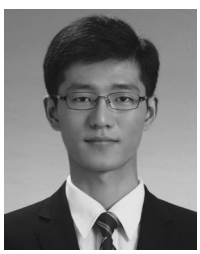


Xueqing Li received the B.S. and Ph.D. degrees in electronics engineering from Tsinghua University, Beijing, China, in 2007 and 2013, respectively.

Since 2013, he has been a Postdoctoral Researcher in the Department of Computer Science and Engineering, Penn State University, State College, PA, USA. His current interests include wideband high-dynamic-range DACs, RF-powered systems, wireless sensor networks, and other low-power high-performance RF and mixed-signal IC designs using both CMOS and emerging devices like steep-slope tunnel FETs.

Qi Wei received the Ph.D. degree from Tsinghua University,Beijing, China, in 2010.

He is now an Assistant Professor in the Department of Electronics Engineering, Tsinghua University. His research interests are analog IC design and high performance data converters, including high performance operational amplifier, pipeline ADC, SAR ADC, current DACs.



Zhen Xu was born in Fuyang, Anhui Province, in 1989. He received the B.S. degree in 2011 and the M.S. degree in March, 2014, from the Electronic and Information Engineering Department, Beijing Jiaotong University, Beijing, China.

He is a Research Assistant in the Department of Electronics Engineering, Tsinghua University, Beijing, China, since 2011. His current interest is high-resolution current-steering DACs.

Jianan Liu received the B.S. degree from the Department of Electronic Engineering from Tsinghua University, Beijing, China, in 2012. He is currently a Masters degree candidate in the Department of Electronic Engineering in Tsinghua University.

His research interest is high-resolution and high-speed DACs.

Hui Wang received the B.S. degree in radio electronics from Tsinghua University, Beijing, China, in 1970.

She served as Vice Director of Electronics Engineering Department, Tsinghua University, from 1996 to 1999, Deputy Dean of Academic Affairs Office from 1999 to 2005, and the Vice Dean of School of Information Science and Technology from 2005 to 2012. She was a Visiting Scholar at Stanford University, Stanford, CA, from 1991 to 1992. She participated in many projects from the Natural Science Foundation of China (NSFC), "863" program and some key programs of fundamental research.

Prof. Wang was a recipient of awards including the Science and Technology Progress Award (I) from Chinese Ministry of Electronics, the National Science and Technology Progress Award (III) from National Science and Technology Communication and Teaching Achievement Award (I) from Chinese Ministry of Education.

Huazhong Yang (M'97–SM'00) was born in Ziyang, Sichuan Province, China, on August 18, 1967. He received the B.S. degree in microelectronics in 1989, the M.S. and Ph.D. degrees in electronic engineering in 1993 and 1998, respectively, all from Tsinghua University, Beijing.

In 1993, he joined the Department of Electronic Engineering, Tsinghua University, Beijing, where he has been a Full Professor since 1998. He has been in charge of several projects, including projects sponsored by the national science and technology major project, 863 program, NSFC, 9th five-year national program and several international research projects. Dr. Yang has authored and co-authored over 300 technical papers, seven books, and over 70 granted Chinese patents. His current research interests include wireless sensor networks, data converters, energy-harvesting circuits, parallel circuit simulation algorithms and nonvolatile computing.

Dr. Yang was awarded the Distinguished Young Researcher by NSFC in 2000 and Cheung Kong Scholar by Ministry of Education of China in 2012. He has also served as the chair of Northern China ACM SIGDA Chapter.