A Reconfigurable Low-Power BDD Logic Architecture Using Ferroelectric Single-Electron Transistors

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***Abstract*— This paper presents ferroelectric single-electron transistors (SETs) with tunable tunnel barriers and their application in a reconfigurable binary decision diagram (BDD) logic architecture. In this experimental demonstration, the SETs can be programmed into short, open, and Coulomb blockade modes to construct the BDD fabric. We experimentally demonstrate the decision node, consisting of two SETs, with robust path switching characteristics. Harnessing such programmability and path switching features, a nonvolatile reconfigurable low-power BDD logic is achieved. A ferroelectric dielectric-based split gate configuration and a differential biasing scheme are utilized to share the programming resources and reduce the energy consumption. Peripheral interface circuits are designed to recover the output signal swing for cascaded BDD logic demonstration and to provide noise immunity. The simulation shows that with sufficient circuitry complexity or a latched dynamic CMOS interface, the proposed BDD architecture achieves higher power efficiency than CMOS at the same throughput delay.**

***Index Terms*— Binary decision diagram (BDD), Coulomb blockade, ferroelectric, nonvolatile, sense amplifier, single-electron transistor (SET).**

I. Introduction

TECHNOLOGY scaling predicted by Moore's law has successfully led to integration of billions of transistors on a single chip with reduced cost per function. Yet, the energy consumption and device-to-device variation remain a bottleneck in future scaling [1]. FinFETs and gate-all-around transistors with an ultrathin body are being pursued to address the transistor scaling issues for the 10-nm node and beyond [2]. In the limit of the ultimate transistor dimension scaling, we expect it to evolve into nonclassical single/few-electron transistors even at room temperature.

In this paper, we explore experimentally and theoretically single-electron transistors (SETs) that utilize the Coulomb blockade effect in a gated 0-D quantum dot as a device candidate for ultralow-power logic applications [3]. Fig. 1(a) shows the trend of switching energy as a function of transistor scaling [4]. Due to the markedly reduced electron count in the OFF/ON switching operation, the energy per operation of an SET potentially approaches the theoretical limit $k_BT \times \ln 2$, which is much less than that of classical MOSFETs. However, few-electron devices exhibit much worse ON/OFF switching characteristics compared with their MOSFET counterpart [5]. Fig. 1(b) shows the voltage transfer characteristic of an SET inverter [5]. Nanoscale devices in the single- or few-electron regime suffer from low transconductance, degraded output resistance, and, often, a lack of complementary (n and p-channel) solution, making it essential to coexplore the device design in conjunction with a non-CMOS logic architecture [6].

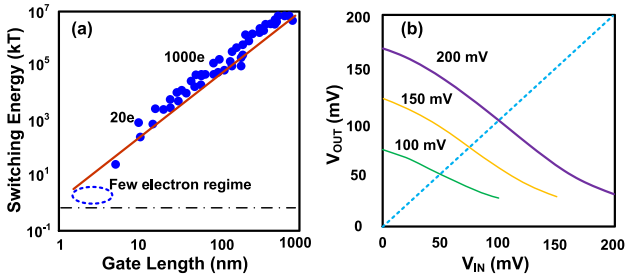

Fig. 1. (a) Silicon nMOS switching energy scales with the gate length and the number of channel electrons. (b) Voltage transfer characteristic of an SET inverter.

The binary decision diagram (BDD) logic has been proposed as a suitable logic architecture for implementing logic with SETs [7]. Recently, BDD architecture optimizations using the mapping algorithm to achieve the minimum area and number of layers have attracted much attention [8]–[11]. BDD stacks are capable of building any combinational logic as an alternate representation of the logic truth table. In the BDD logic, the logic input to the decision node determines the conducting path. Fig. 2(a) shows a BDD diagram for a three-input OR logic. The messenger electrons are routed into the left or right path according to the logic input at each decision node and detected at the 0/1 terminal. On the other hand, the potentially high defect rate and variability in the devices operating close to the scaling limit makes the reconfigurability and tunability of the device characteristics vital to SET BDD architecture implementations. The reconfigurable

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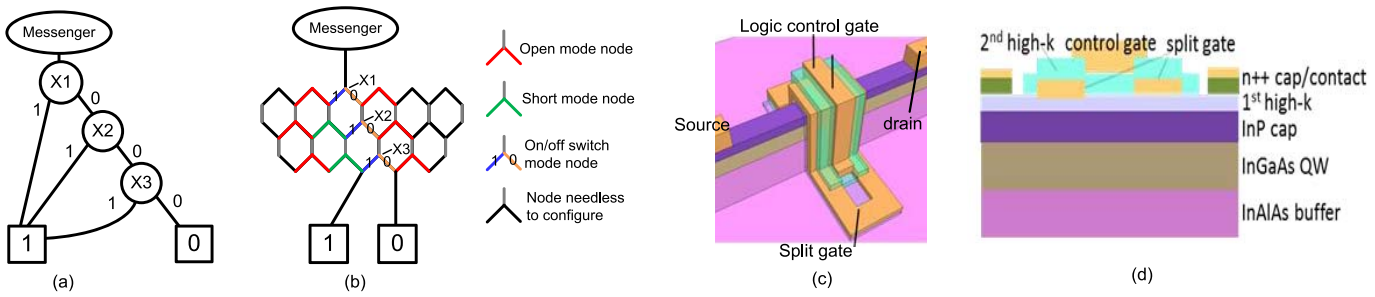


Fig. 2. (a) BDD diagram representative of three-input OR logic function. (b) Mapping of three-input OR logic function to a hexagonal BDD fabric. (c) Schematic of the reconfigurable device with a split gate for programming and a control gate for logic input. (d) Schematic of the cross section of the device.

BDD logic architecture requires the SET to be programmed not only to perform as a decision node edge and execute the path switching function, but also to act as a short or an open path along certain edges of the 2-D hexagonal fabric. Fig. 2(b) shows an example of mapping a three-input OR logic onto a hexagonal BDD fabric. Such a scenario avoids certain device failures, as well as maps different logic functions in the same BDD fabric.

There are several reported experimental demonstrations of SETs [12]–[15]. In [12] and [13], gated nanoparticles with a thin insulator film as a barrier are used to isolate the Coulomb island from the source/drain Fermi reservoir. The barriers are not tunable once the film material and thickness are selected. Other reports [14], [15] construct the Coulomb island confined by several Schottky gates in the GaAs/AlGaAs 2DEG system. The advantage of the electrostatically controlled barriers is that the coupling strength between the source/drain and the Coulomb island is tunable. Yet the disadvantages are: 1) low device density due to several complicated Schottky gates aligned in 2-D; 2) large parasitic capacitance of the Coulomb island to the substrate due to lack of physical isolations; and 3) continuous Schottky gate biasing during device operations. In [3], 1-D nanowire and two Schottky split wrapped gates are used to overcome the device density and dot-to-substrate capacitance problems. However, the lack of independent gate control makes the barriers electrically unstable when modulating the Coulomb island potential. None of these satisfy the device requirement of reconfigurable BDD fabric.

In this paper, we present a programmable SET with tunable barriers and independent logic gate that is applicable to reconfigurable BDD logic. The device schematic is shown in Fig. 2(c). The split gate tunes the electrostatic barriers within the 1-D nanowire while the control gate modulates the potential of the Coulomb island. We also demonstrate path switching operation in a BDD decision node consisting of two SETs. Further, we demonstrate the integration of ferroelectric dielectric into the split gate-stack and achieve nonvolatile programming functionality which leads to energy savings.

The rest of this paper is organized as follows. Section II introduces the proposed single-electron device fabrication and characterization. Section III describes the device programming strategy in terms of nonvolatility and local reference. Section IV benchmarks the performance of the proposed BDD logic against the conventional CMOS logic implementation. Finally, the conclusion is given in Section V.

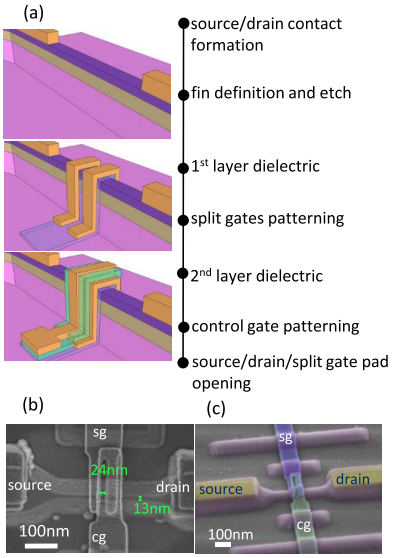


Fig. 3. (a) Device fabrication flow of a programmable SET. (b) Scanning electron microscope image (top view). (c) Tilted scanning electron microscope image (false colored) of fabricated device.

II. Device Fabrication and Characterization

The programmable SETs are fabricated on a strained $In_{0.7}Ga_{0.3}As$ quantum well (QW). The layer structure consists of InP substrate/$In_{0.52}Al_{0.48}As$ (300 nm) buffer/ 2×10^{12} cm^{-2} n-type Si modulation doping/$In_{0.52}Al_{0.48}As$ (3 nm) spacer layer/$In_{0.7}Ga_{0.3}As$ (14 nm) QW/InP (2 nm)/ n+ $In_{0.53}Ga_{0.47}As$ cap layer (20 nm). The electrons are confined in the QW channel by the high bandgap $In_{0.52}Al_{0.48}As$ bottom barrier and the InP top barrier. The high electron mobility in the system provides an opportunity for the integration of high-performance classical QW FETs for peripheral circuits on the same chip with the BDD stacks. The low effective mass leads to strong quantization and increased separation of the bound states in the QW, thereby facilitating room temperature quantum device operation.

The device fabrication process is shown in Fig. 3(a). Evaporated Ti/Au source/drain contacts and alignment markers were defined by e-beam lithography and formed by the liftoff process. The Ti/Au forms ohmic contact with the n+ cap layer. Then the active device region for the gate-stack was defined and we etched the n+ cap layer using citric acid/H_2O_2/H_2O solution. The wet etch process stops selectively on the InP barrier. The 1-D narrow fin pattern

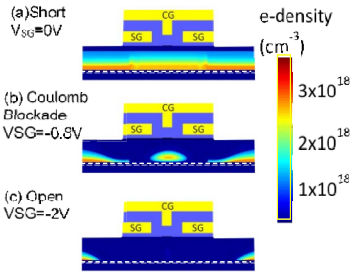


Fig. 4. Self-consistent Schrodinger–Poisson simulation of electron density of short, open, and Coulomb blockade modes with $V_{SG} = 0$, -0.8, and -2 V.

was carefully defined with the optimal dose level using an electron beam with high-resolution resist. A BCl_3/Ar plasma etch process was used to etch the fins. The nominal widths of the etched fins are around 10 nm. Afterward, the first dielectric of 10-nm Al_2O_3 was formed using atomic layer deposition (ALD). Then the split gate region was defined using electron beam lithography. The Pd/Au metal stack was deposited using the evaporation and lift-off process. The split gate finger width is around 60 nm, and the separation between the split gate fingers can be as small as 30 nm. The second dielectric of 10-nm Al_2O_3 was deposited using ALD and the top control gate (Pd/Au) was aligned and deposited spanning the gap between the split gates. The top control gate width was designed to be larger than the gap for sufficient tolerance of possible alignment errors. Fig. 3(b) and (c) shows the scanning electron microscope image of the fabricated device with a ~13-nm fin width and a ~25-nm split gate separation.

The quantum dot device dimensions can be estimated from the fin width, split gate separation, and QW thickness T_{QW} ($T_{QW} \approx (13 \times 25 \times 12)^{1/3} \approx 15$ nm). The split gate determines the coupling strength between the source/drain and the Coulomb island. The corresponding charging energy of ~60 meV is much smaller than 260 meV ($10k_BT$@300 K). This energy scale is not likely to exhibit Coulomb blockade at room temperature. Therefore, the fabricated programmable SET was electrically characterized at 77 K using a Lakeshore cryogenic probe station and an HP 4155 semiconductor parameter analyzer. Fig. 4 shows the self-consistent Schrodinger–Poisson simulation of the electron density. Fig. 5(a) shows the corresponding transfer characteristics of the device under bias conditions $V_{SG} = 0$, -0.8, and -2 V. When $V_{SG} = 0$ V, this device is in a depletion mode QW FET modulated by the control gate. The device is in ON state if V_{CG} is greater than the threshold voltage -1 V. If the V_{CG} window is always greater than -1 V, this device is in a short mode. When $V_{SG} = -0.8$ V, the split gate creates depletion regions serving as barriers to isolate the channel between source/drain. When the tunneling resistance resulting from the depletion region is greater than h/q^2, where h and q represent the Planck constant and the charge of a single electron, respectively, the channel is considered as an isolated Coulomb island with electron wave confined inside. In this scenario, the energy levels in the Coulomb island are discretized. The addition energy E_A, which is required to transfer one more electron to the Coulomb island, arises from both the Coulomb charging energy related to

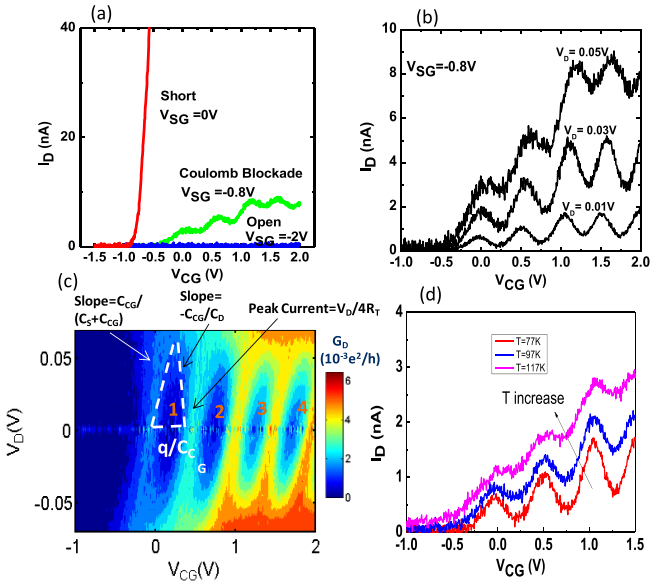


Fig. 5. (a) I_D–V_{CG} characteristics of a programmable SET in short, Coulomb blockade, and open modes at 77 K. (b) I_D–V_{CG} characteristics under various drain bias conditions in the Coulomb blockade mode. (c) Drain conductance is plotted as a function of V_{CG} and V_D in Coulomb blockade mode. The device parameters extracted from this contour are listed in Table I. (d) I_D–V_{CG} characteristics at different temperatures.

TABLE I
EXTRACTED DEVICE PARAMETERS

No.	C_S (aF)	C_D (aF)	C_{CG} (aF)	R_T (MΩ)
1	1.38	0.93	0.241	4.6
2	1.44	0.96	0.256	2.64
3	1.45	0.95	0.263	1.67
4	1.49	0.99	0.275	1.64

electron-to-electron interaction and the size quantization effect. When the control gate modulates the Coulomb potential with a small drain bias, the conductance peaks occur when one of the energy levels periodically aligns with the source/drain Fermi level.

The oscillations I_D–V_{CG} under $V_{SG} = -0.8$ V are clearly shown in Fig. 5(a) and (b). At $V_{SG} = -2$ V, the strong depletion effect results in a very large tunnel resistance and depletes the entire Coulomb island region. Thus, only the background leakage current can be observed as shown in Fig. 5(a). In Fig. 5(b), the I_D–V_{CG} characteristics for various drain bias conditions are shown. Clearly, the higher drain bias results in a smaller peak-to-valley current ratio. As the drain potential is larger than E_A/q, the oscillation tends to disappear since at least one transmission state can always be aligned within the gap between the Fermi levels of the source and the drain contact. Fig. 5(c) shows the drain conductance (I_D/V_D) contour as a function of the control gate voltage and the drain voltage. The device capacitance and the resistance parameters can be calculated from the shape of the Coulomb diamonds and the peak drain conductance. The extracted parameters are listed in Table I. From the extracted parameters, the addition energy can be estimated as $q2/C_\Sigma = 63$ meV, which is around $10k_BT$ for 77 K. The gate coupling ratio is $C_G/C_\Sigma = 10\%$. Fig. 5(d) shows the temperature effect

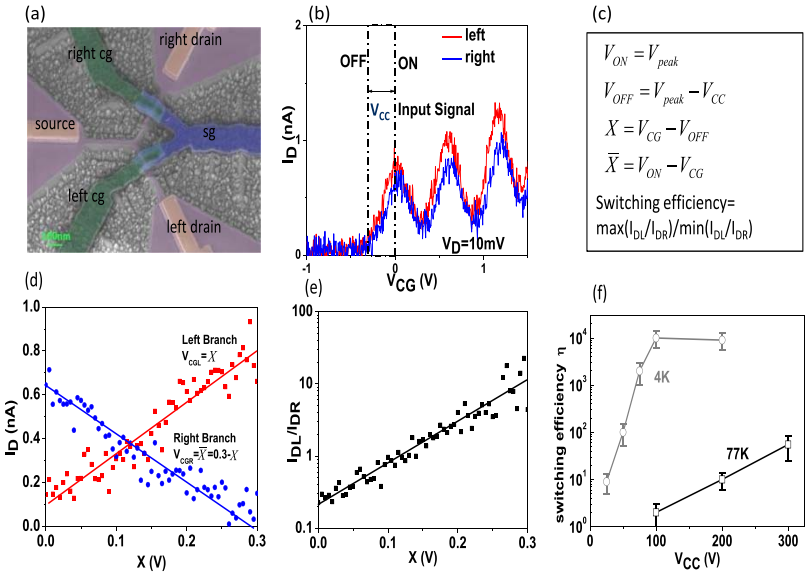


Fig. 6. (a) Scanning electron microscope image of fabricated BDD decision node. (b) I_D–V_{CG} characteristics of devices in the left and right branches. (c) Logic input transform to variable X after defining low and high states. (d) I_D–X characteristics for the left and right branches. (e) Current ratio versus logic input. (f) Switching efficiency as a function of the width of the logic input voltage window V_{CC}.

TABLE II
PROJECTED ROOM-TEMPERATURE SET FOR SILICON AND $In_{0.7}Ga_{0.3}As$

Material	Size (nm)	E_C (meV)	E_Q (meV)	E_Σ(meV)
silicon	2	170	90	260
$In_{0.7}Ga_{0.3}As$	5	60	200	260

on Coulomb oscillations. As the thermal energy increases with temperature rising from 77 to 117 K, the oscillation characteristics are suppressed. To enable higher temperature operation, further device dimension scaling is required to provide higher Coulomb charging energy. The quantization effect, which is also sensitive to device scaling, can effectively increase the addition energy in sub-10-nm III–V systems, leading to reasonable values of device dimensions necessary in this system to achieve room temperature device operations. Assuming that the dot has a spherical shape, Table II shows the estimated dimension, Coulomb charging energy, and quantization energy for SETs working at room temperature for both $In_{0.7}Ga_{0.3}As$ and silicon.

Based on the oscillation characteristics, logic switching can be experimentally demonstrated in a BDD decision node consisting of programmable SETs. Fig. 6(a) shows a fabricated BDD decision node. The decision node has logic input X to the left control gate and $\overline{X}$ to the right control gate. In the device test, the common source node is grounded and the drains are biased at 10 mV. The split gate bias is set at −0.8 V to program the device into the Coulomb blockade mode. Fig. 6(b) shows the I_D–V_{CG} characteristics for the left and right branches. The ON state is defined as the peak position. V_{peak} and the OFF state are determined by V_{peak}–V_{CC}, where V_{CC} is the chosen V_{CG} window width. Therefore, the logic input should be defined as V_{CG}–V_{OFF} and V_{ON}–V_{CG}. After performing the voltage transformation indicated in Fig. 6(c), the current in the left and right drain nodes as a function of the input X is plotted in Fig. 6(d). Fig. 6(e) shows the current ratio I_{DL}/I_{DR} and the path switching efficiency. The maximum and minimum current ratio indicates the switching efficiency. If the two SETs are identical, the minimum current ratio should be the inverse of the maximum ratio. We use $(I_{DL}/I_{DR})_{max}/(I_{DL}/I_{DR})_{min}$ to characterize the worst case switching efficiency since device variations always exist in practical implementations. Fig. 6(f) shows the switching efficiency for different V_{CC}s. A larger V_{CC} provides higher switching efficiency if the OFF state has not reached the minimum current level. When V_{CC} is sufficiently large to reach the minimum current (background leakage current) in the OFF state, the switching efficiency saturates as shown in the 4-K curve. The experimentally achieved switching efficiency is 80 at 77 K and over 10^4 at 4 K.

III. DEVICE PROGRAMMING STRATEGY: NONVOLATILITY AND LOCAL REFERENCE

As discussed in the previous section, the devices can be programmed into short, Coulomb blockade, and open modes according to the split gate voltage. It is straightforward to realize the BDD hexagonal fabric programming as shown in Fig. 7(d). Fig. 7(a) shows the cross section schematic of the split gate wrapping around the fin. This strategy requires individual split gate voltage supply for each nonvertical edge. In addition, the split gate has to be always biased to maintain the device mode, which is not preferable in a low-power design. Nonvolatile gate-stack using ferroelectric dielectric has been proposed to reduce the energy consumption and share programming resources [6], [16]. The ferroelectric split gate structure is shown in Fig. 7(b).

Fig. 8 shows the experimental result of the ferroelectric SET reported in [16]. Once a programming pulse initiates polarizations in the ferroelectric, the remnant polarizations are able to create the depletion barriers. The barrier resistance depends on the amount of remnant polarizations, which corresponds to the amplitude of the programming pulse before reaching the

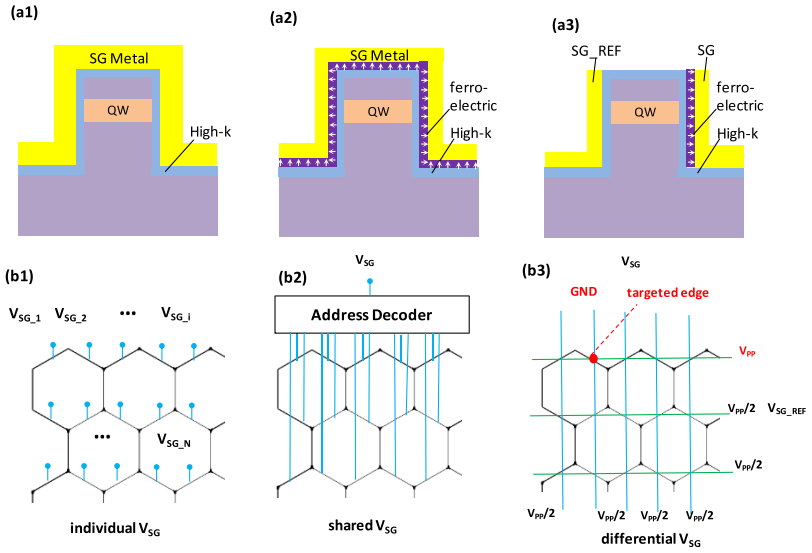
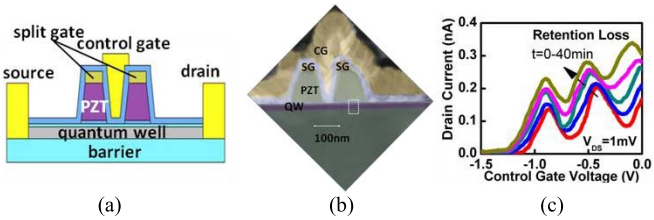


Fig. 7. (a)–(c) Cross section schematics for nonferroelectric, ferroelectric, and differential input split gate. (d)–(f) BDD fabric programming strategy using gate-stacks in (a)–(c).



(a) (b) (c)

Fig. 8. Nonvolatile ferroelectric SET using ferroelectric gate in [16]. (a) and (b) Cross section schematic and TEM image along the transport direction. (c) Retention measurement of Coulomb blockade device mode.

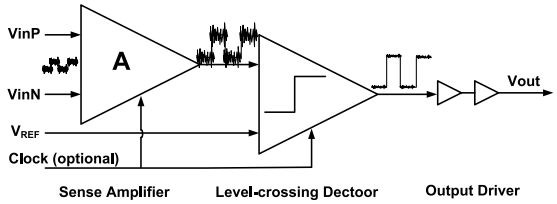


Fig. 9. CMOS interface circuit between the BDD logic blocks.

saturation point. A retention time of more than 40-min Coulomb oscillation has been demonstrated. With the ferroelectric gate-stack, the fabric can be programmed sequentially using the shared split gate voltage supply in Fig. 7(e). On the other hand, the differential V_{SG} input has been proposed to further reduce the number of split gate wire [6]. The differential V_{SG} can be realized by the device structure shown in Fig. 7(c) with ferroelectric gate-stack for V_{SG} and nonferroelectric gate-stack for local reference $V_{SG_{Ref}}$. The polarization is set by the differential voltage $V_{SG}-V_{SG_{Ref}}$ with source/drain floating in the programming stage. After removing V_{SG} and $V_{SG_{Ref}}$, the remnant polarization creates an electric field to deplete the fin. Fig. 7(f) shows this antifuse-like schematic to program the targeted edge with $V_{SG} = V_{PP}$ and $V_{SG_{Ref}} = 0$. All the deselected V_{SG} and $V_{SG_{Ref}}$ are kept at $V_{PP}/2$. The effective programming voltage at the targeted edge is V_{PP}, and 0 or $V_{PP}/2$ at the other deselected edges. The challenge still remains as how to avoid the $V_{PP}/2$ perturbation to the existing device state.

IV. Peripheral Interface Circuits and Energy Delay Benchmarking

Ideally, the output voltage level of the SET BDD fabric is either V_{CC} as logic 1 or ground as logic 0. A voltage too close to $V_{CC}/2$ should be avoided to prevent unpredictable output. As discussed earlier with Fig. 6, the output amplitude swing is lower than the input swing to the control gate, mainly because of the finite OFF- and ON-state resistance ratio R_{OFF}/R_{ON}. The amplitude degrades if more selected (deselected) branches are connected in series (parallel). Fig. 10(a) shows the worst amplitude for logic 1 versus the BDD depth, which demands an interface between BDD blocks to recover the degraded voltage swing. Fig. 9 shows such an interface, consisting of a sense amplifier to recover the signal swing, a level crossing detector to filter possible noise due to switching, and a driver for sufficient fanout driving ability.

The necessity of using the interface circuitry brings area and energy overhead. Such overhead depends on the required gain of the sense amplifier to recover degraded amplitude swing related to the BDD depth, and the driving capability for the next BDD block with a certain fanout factor. As for the SET BDD fabric, the area is mainly determined by the number of SET transistors. As shown in Fig. 10(b), the worst case area overhead percentage by the BDD interface reduces as the BDD depth increases, and contributes to the area outperformance over the CMOS logic solution. Meanwhile, a higher R_{OFF}/R_{ON} at the same BDD depth also reduces this area overhead.

For the energy-delay evaluation, the BDD simulation is conducted in a commercial Monte Carlo simulator SIMON [17] using the experimentally extracted parameters presented in Table I. The CMOS circuits are simulated using Cadence Spectre based on a calibrated 22-nm node silicon FinFET model generated by commercial simulator TCAD Sentaurus [18]. Fig. 11 compares the simulated energy-delay of a three-input NAND gate and a full adder using CMOS technology and the BDD logic architecture with a CMOS

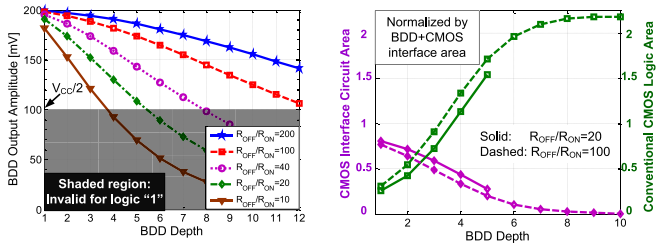


Fig. 10. (a) Worst logic 1 output amplitude versus the BDD depth with $V_{CC} = 0.20$ V. (b) Worst case area comparisons for fanout = 4 driving capability with $R_{OFF}/R_{ON} = 20$ and 100. Assumptions—a BDD SET has the same area as the smallest MOSFET; the conventional CMOS logic is implemented using the NOR and NAND gates; the BDD fabric occupies a rectangular outline.

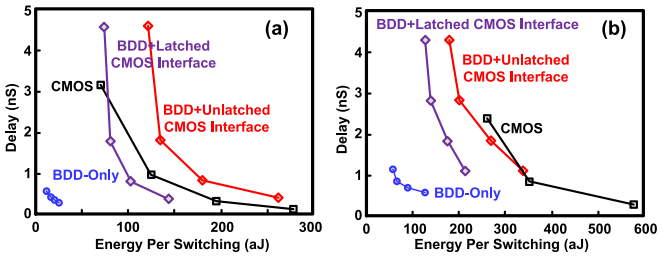


Fig. 11. Energy-delay comparison between CMOS logic and BDD logic with a fanout = 4 CMOS interface circuit. (a) Three-input NAND. (b) Full adder. The supply voltage changes from 300 to 150 mV.

interface. The BDD energy consumption is minimized due to the single-electron switching operation and is mainly consumed in the CMOS interface circuit.

For nonpipelined logic designs, the sense amplifier and level-crossing detector in the BDD interface are not latched by a clock signal and have constant biasing power consumption. In this case, for the three-input NAND gate, the SET BDD with CMOS interface solution consumes ∼30% more energy than the CMOS solution at the same speed, as shown in Fig. 11(a). For the more complex full adder, the BDD architecture consumes less energy per operation, as shown in Fig. 11(b).

For a pipelined BDD logic design, the sense amplifier and the level-crossing detector are latched by the clock, functioning as dynamic amplifier and comparator with almost no dc power consumption [19]. In this case, as shown in Fig. 11(b), the BDD + CMOS interface solution has higher power efficiency than the CMOS solution in almost all energy-delay corners.

From the SET device aspect, future research on the process scaling capability to fabricate a smaller Coulomb island is helpful for a larger OFF/ON resistance ratio for a larger BDD depth, and thus less power and area overhead by both the BDD fabric and the CMOS interface circuit, which makes the BDD architecture more promising. Further, although beyond the scope of this paper, the level-crossing detector could be eliminated for more power saving, when the signal amplitude is sufficiently large to tolerate the noise in high-V_{CC} or low-BDD-depth designs.

V. Conclusion

The III–V QW-based ferroelectric SETs experimentally show the robust programmability among short, open, and Coulomb blockade operation modes using split gate bias. This enables us to build reconfigurable BDD logic circuits with compatible integration of a CMOS interface circuit between the SET BDD blocks. The energy-delay benchmark indicates that with sufficient circuitry complexity or a latched dynamic CMOS interface, the SET BDD + CMOS interface architecture outperforms the conventional CMOS logic circuit in energy efficiency. Future noise study, BDD mapping algorithm for area and depth optimization, as well as the device fabrication techniques are of significance.

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Authors' photographs and biographies not available at the time of publication.