Correlated Material Enhanced SRAMs With Robust Low Power Operation

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***Abstract*— We propose a novel static random access memory (SRAM) cell employing correlated material (CM) films in conjunction with the transistors to achieve higher read stability, write ability, and energy efficiency. The design of the proposed SRAM cell utilizes orders of magnitude difference in the resistance of the insulating and metallic phases of the CM to mitigate the design conflicts. By appropriately controlling the phase transitions in the CM films during SRAM operation through device–circuit codesign, we achieve 30% higher read static noise margin and 36% increase in the write margin over standard SRAM. The proposed design also leads to a 50% reduction in the leakage current due to high insulating state of the CM. This is achieved at 28% read time penalty. We also discuss the layout implications of our technique and present techniques to sustain no area overhead.**

***Index Terms*— Correlated materials (CMs), insulator to metal transition (IMT), metal to insulator transition (MIT), static noise margin (SNM), static random access memory (SRAM).**

I. Introduction

TECHNOLOGY scaling has been the driving force for the improvement in performance, energy efficiency, and integration density of electronic systems [1]. However, the benefits of scaling are accompanied by several design issues, such as increase in leakage, exacerbation of short channel effects, and aggravation in design conflicts between speed, power, and robustness. With a looming uncertainty on the future of standard transistors due to such issues, a strong need has arisen to explore alternate technologies. Devices based on alternate materials, such as GaAs and germanium [2], are being investigated for high performance computing. Technologies which beat the 60 mV/decade subthreshold swing limit exhibited by standard transistors have garnered interest for low power applications. In particular, tunnel FET (TFETs) and negative capacitance FETs have shown an immense promise. Recently, steep-switching transistors based on correlated materials (CM) exhibiting abrupt insulator metal transitions (IMTs) have been proposed [3]. These devices, known as hybrid phase transition FETs (HyperFETs), show unique characteristics, such as hysteretic behaviour and abrupt increase in current at certain gate and drain voltages. Such distinct properties offer new opportunities for mitigating the design conflicts and alleviating the limitations of standard transistor-based circuits in deeply scaled technologies. One class of circuits, which is severely affected by the issues associated with the scaling of conventional transistors and therefore, strongly needs novel design techniques, is static random access memory (SRAM). Due to self-conflicting requirements for optimizing the read and write operations, which are aggravated by increasing short channel effects and process variations, the design space for SRAMs dwindles with technology scaling. Moreover, advanced transistors, such as FinFETs suffer from width quantization [4], which aggravates the read–write conflict in SRAMs. In addition, increasing transistor leakage has a strong impact on the power efficiency of a memory macro. This is because the energy dissipation is dominated by leakage due to a low activity in a large memory array. These issues need to be addressed by employing new technologies that are inherently better than standard transistors. Several previous works have explored such technology-aware design approaches for SRAMs. In [5], independent gate control in FinFETs was utilized to increase the stability of SRAMs. In [6], asymmetry was introduced in the devices to mitigate the read–write conflicts. New SRAM cells based on TFETs have been widely explored in [7]. All these approaches point to the importance of device–circuit codesign in optimizing SRAMs in advanced technologies.

In this paper, we propose a novel SRAM cell, which utilizes the unique properties of CMs and HyperFETs to achieve simultaneous increase in the read stability and write ability, thus mitigating the read–write conflict. In addition, significant leakage reduction and enhancement in the hold stability is attained. The proposed SRAM cell requires judicious device–circuit codesign to trigger data-dependent and operation-driven IMTs in the CM. In addition, we follow layout-driven codesign of the cell and the CM to achieve the aforementioned benefits at no area cost. The contributions of this paper are summarized as follows.

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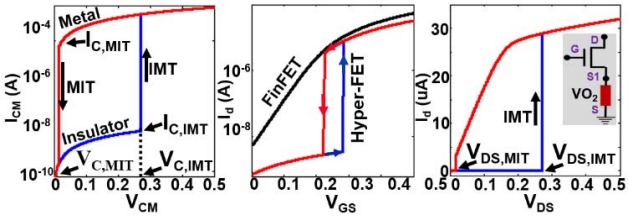

Fig. 1. (a) I–V Characteristic of a CM. (b) I_d–V_{gs} characteristic of HyperFET compared with I_d–V_{GS} of FinFet. (c) I_d–V_{ds} characteristic of a HyperFET with HyperFET structure having VO_2 connected to the source of the transistor.

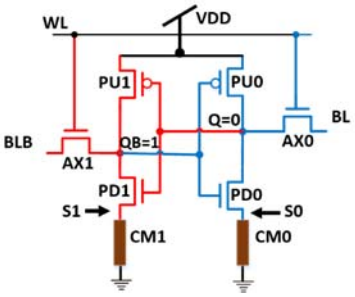

Fig. 2. IMT material connected to the source of "PD0" and "PD1."

1) We propose a novel SRAM cell employing CMs in conjunction with the transistors to achieve higher stability, write ability, and energy efficiency.
2) We present the layout implications of the proposed SRAM by analysing the impact of introducing a CM in the cell.
3) We present a layout-aware device–circuit codesign methodology for the proposed SRAM, which utilizes the distinct properties of CMs and HyperFETs to mitigate the design conflicts.
4) We quantify the stability, leakage, performance, and area of the CM augmented SRAM, and perform a comparison with standard SRAMs.

II. Correlated Materials and HyperFET

Functional oxides, such as VO_2 and NbO_2, are a class of CMs, which exist in two phases (metallic and insulating) due to collective carrier dynamics. CMs exhibit abrupt IMTs, which may be triggered by strain [8], thermal excitation [9], or electrical current/voltage [10]. The IMTs and metal-to-insulator transition (MITs) driven by voltage/current have been experimentally demonstrated in materials, such as VO_2 and V_2O_3, at room temperature [11]. Such CMs operate in the insulating phase in the absence of the voltage/current stimulus. As the applied voltage (V_{CM}) or current (I_{CM}) is increased, CMs remain in the insulating state as long as $I_{CM} < I_{C,IMT}$ (critical current for IMT) and $V_{CM} < V_{C,IMT}$ (the corresponding critical voltage). Increase in voltage/current beyond the critical values triggers IMT and the CM transitions into the metallic phase. CM remains in the metallic state as long as $I_{CM} > I_{C,MIT}$ (i.e., $V_{CM} > V_{C,MIT}$). (Here, $I_{C,MIT}$ and $V_{C,MIT}$ are the critical current and voltage, respectively, for MIT). The current–voltage characteristics of CMs show orders of magnitude difference in the resistance of the metallic (R_{metal}) and insulating phases ($R_{insulator}$). In typical CMs, $I_{C,IMT} < I_{C,MIT}$ and $V_{C,IMT} > V_{C,MIT}$, which leads to hysteresis in the current-voltage (I–V) characteristics. Several CMs show such behavior with a wide range of resistivity ratios and critical current densities. Therefore, application-driven downselection of suitable CMs and tailoring of their properties can lead to intriguing possibilities of novel devices.

HyperFET [3] is one such device, in which a VO_2 is integrated with source of an FET [Fig. 1(c) (inset)]. HyperFETs exhibit abrupt change in the drain current if its gate voltage or drain voltage increases beyond a critical value [Fig. 1(b) and (c)]. This critical value corresponds to the point at which the transistor current is equal to I_{CIMT} and the voltage across CM ($V_{S'S}$) is equal to $V_{C,IMT}$. The abrupt change in current is induced by IMT in the CM resulting in subthreshold swing much smaller than 60 mV per decade [3]. Similarly, as the gate or drain voltage is decreased, the CM undergoes MIT and drain current abruptly decreases when the voltage across CM goes below $V_{C,MIT}$. Like CMs, HyperFETs show hysteretic characteristics. Due to a large resistivity in the insulating state, the FET gets strongly source-degenerated, which leads to a significant reduction in the OFF current. In the ON-state, the CM operates in the metallic state, as a result of which, the reduction in the ON-current is mild. Because of the large resistivity ratio, HyperFETs exhibit a boost in the ratio of ON and OFF currents. In this paper, we utilize these unique features of CMs and HyperFETs to enhance the stability, write ability, and energy efficiency of the SRAM cell.

III. Correlated Material-Enhanced SRAM

The proposed SRAM cell is shown in Fig. 2. Two CM films (CM0 and CM1) are incorporated in the design by electrically integrating them in series with the pull-down n-channel FETs PD0 and PD1, forming the HyperFET structure mentioned in Section II. The role of the CMs in the proposed cell is to selectively change the resistance of the pull-down path during the read and write operations, depending on the voltage of the respective storage nodes, with an objective to enhance the stability. Additionally, since HyperFETs have lower OFF current compared with the standard transistors [Fig. 1(b)], reduction in cell leakage is achieved. Next, we describe the cell operation and how the unique characteristics of the CM are utilized in the proposed design. Without any loss of generality, let us assume node "Q" stores "0" and node "QB" stores "1."

A. Hold/Standby Mode

The cell is so designed that during the hold state, CM0 and CM1 operate in the insulating phase i.e., voltages at S0 and S1 (V_{S0} and V_{S1}, respectively) $< V_{CIMT}$. With the wordline (WL) voltage at 0 and the access transistors in the OFF-state, the voltage at the storage nodes is determined by the relative resistance of the pull-up pMOSFETs and pull-down HyperFETs. With $Q =$ "0" and QB = "1," PU1 is ON, which charges QB to V_{DD}. The voltage at Q (V_Q) is determined by the resistive division between PU0 (in the OFF-state) and the CM0 (in the insulating phase). (Note that the resistance of PD0 in the ON-state is much smaller than PU0 and CM0 and thus, may be neglected.) The insulating resistance

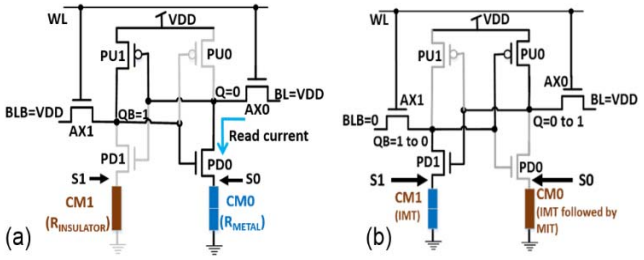

Fig. 3. (a) Circuit representation during read operation. (b) Circuit representation during write operation.

of CM0 is designed to be significantly smaller than the OFF-state resistance of the pMOS and nMOS, so that V_Q and V_{S0} are sufficiently close to 0. This also leads to small voltage at S1, which is determined by the resistive division between PD1 (in the OFF-state) and S1 in the insulating phase. Despite Q being close to 0, it (Fig. 2) is not directly connected to the GND, since the insulating state resistance is reasonably large. Hence, node Q is a high-impedance node with its voltage very close to 0. There is a possibility of node Q being elevated above "0 V" because of the high impedance, which affects the hold static noise margin (SNM). However, this effect on the hold SNM is mild. This is because an increase in noise voltage at node Q beyond a certain value (such that voltage at S0 $> V_{C,IMT}$) triggers IMT in CM0, which establishes the connection of storage node Q to ground, pulling it down to 0, thereby retaining the data. As mentioned before, the node QB is always driven to V_{DD} by PU1 in the hold state. This tends to have a positive effect on the hold stability, since the logic threshold voltage (V_M) of the inverter formed by PU1, PD1, and CM1 increases significantly. Therefore, cell design must be such that the latter effect offsets or even dominates the effect of floating node. This requirement is in synergy with the read stability needs, which we will discussion in Section III-B. Thus, despite the operation of the CMs in the insulating state, a properly designed cell exhibits comparable or higher hold stability with respect to the standard SRAM (quantified later) due to: 1) the selective use of the CM (i.e., in series with the pull-down transistors only); 2) the dynamic reduction in the resistance of the CM [in response to the increasing V_{DS}—see Fig. 1(c)]; and 3) increase the trip point of the inverter storing "1." Under normal hold conditions, the CMs operate in the insulating state, as mentioned before. This leads to reduction in the cell leakage due to lower OFF current in the HyperFETs compared with the standard transistors [Fig. 1(b)]. Note that, V_{S0} and V_{S1} are close to 0 but still greater than 0, which leads to lower V_{GS} of PD0 and PD1, resulting in lower leakage. Even though the insulating state resistance of the CM is lesser than the OFF-state resistance of the transistor, this is sufficient to strongly source degenerate the FET and to achieve a smaller leakage.

B. Read Operation

During the read mode, bit lines are precharged to V_{DD} and the assertion of the word-line turns ON the access transistors [Fig. 3(a)]. Recall from the discussion in Section III-A that before the commencement of the read operation, CM0 and CM1 operate in the insulating phase with V_Q, V_{S0}, and V_{S1} close to 0 and $V_{QB} = V_{DD}$ (by design). As AX0 turns ON, read current starts to flow through AX0 and PD0 to charge S0. At the same time, V_Q rises, which increases the current though PD1 and slowly starts charging S1 through AX1 and PD1. The time constant associated with the charging of S0 is lower compared with S1, since the ON-state resistance of AX0 and PD0 is much smaller than the resistance of PD1. As a result, S0 reaches V_{CIMT} faster than S1, which triggers IMT in CM0, pulling down V_{S0} and V_Q. This, in turn, slows down the charging of S1 so that V_{S1} remains less than V_{CIMT}, and CM1 continues to operate in the insulating phase. Metallic CM0 also establishes the discharge path for BL, which enables the sense amplifier to resolve to correct read value. With CM0 operating in the metallic phase and CM1 in the insulating phase, enhancement in the read stability is achieved compared with 6T SRAMs. This is because node QB is strongly driven to V_{DD} by PU1. Since insulating phase of CM1 significantly lowers the strength of the pull down HyperFET PD1, a large increase in V_M is observed. The rise in V_Q is slightly larger than that in standard SRAM. However, the former effect is much more dominant, which enhances the read stability. The additional metallic resistance of CM0 in the read path, although small, leads to a degradation in the read performance. This penalty can be mitigated by judicious selection of the CM, with low resistance in the metallic state and sufficiently large resistance in the insulating state. Such a material would also enhance the stability benefits of the proposed SRAM by reducing the rise in V_Q.

C. Write Operation

During the write operation, BL and BLB are driven to V_{DD} and 0, respectively and on asserting WL, V_Q rises (like the read operation) and V_{QB} falls [Fig. 3(b)]. The cell design for read tends to trigger IMT in CM0 by charging the terminal S0. However, at the same time, reduction in V_{QB} during write tends to increase the charging time of S0. As a result, two scenarios may occur, depending on the design. First, CM0 may remain in the insulating state as V_{QB} may not be sufficient to drive current $> I_{CIMT}$. Second, CM0 may undergo IMT as S0 charges beyond V_{CIMT} followed by the MIT as V_{QB} reduces and current reduces below I_{CMIT}. In both the scenarios, V_Q is higher compared with the standard SRAM. This reduces the strength of PU1, which leads to further reduction in V_{QB}. Discharge of QB turns PU0 ON, which charges Q to V_{DD} (virtually unopposed by PD0, since CM0 is in the insulating state). As V_Q increases, PU1 turns OFF and AX1 discharges QB to "0." Depending on the design of the cell, increase in V_Q may trigger IMT in CM1, which further helps in the discharge of QB. Whether or not CM1 undergoes IMT, QB is driven to GND by the access transistor AX1. Due to the high insulating resistance of CM, which leads to higher V_Q and a more effective feedback action as described before, the write ability is enhanced.

IV. Cell Area and Layout-Aware Array Design

A. Layout Analysis

It is critical to evaluate the impact of CMs on the layout of the cell and consider design strategies to minimize the area

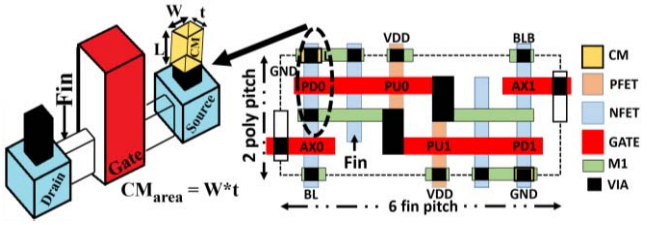

Fig. 4. Layout of the proposed SRAM cell.

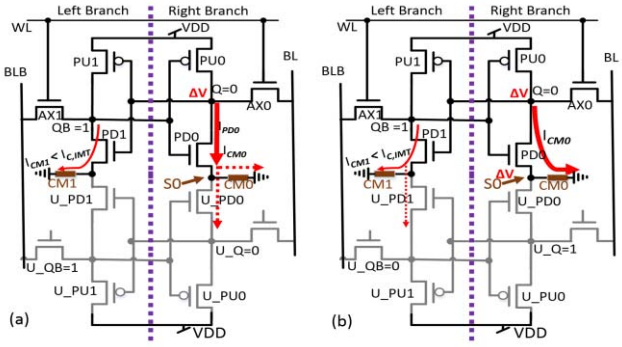

Fig. 5. (a) When unaccessed cell is storing "0," where additional current path causes delayed IMT. (b) When unaccessed cell storing "1." No current path to unaccessed cell, with ΔV voltage across S0, faster IMT.

penalty. The layout of the SRAM is shown in Fig. 4. A 3-D illustration of the pull-down HyperFET with CM displays the length (L) and the area. The vertical dimension of the layout is a function of the poly pitch, lateral dimension is a function of device width (or number of fins in FinFETs) and contact sizes. If exclusive CMs are used for each cell, sharing of the source of the pull-down transistors will be infeasible, leading to an increase in the vertical dimension. This will also lead to an increase in bitline capacitance per cell. In order to avert this area penalty and maintain the same layout footprint as the standard 6T SRAM, we propose to share the CMs amongst the neighbouring cells in the same column (Fig. 4). However, once the CMs are shared with unaccessed cells, there may be an additional current paths bypassing the CM during its high-resistivity state. These current paths are extensively studied and explained in Section IV-B.

B. Design Considerations With Unaccessed Cell

Additional current paths due to CM sharing between neighbouring cells affect the cell current in the accessed cell, leading to an unwanted current in the unaccessed cell (Fig. 5). The design must take into account this effect to ensure that: 1) the accessed cell operates as per the design requirements described in Section III and 2) the current through the unaccessed cell has minimal effect on the array stability. The current through the accessed and the unaccessed cells are dependent on the data stored in both the cells. To explain this, we consider two scenarios: 1) accessed and unaccessed cells have the same data [i.e., Q and U_Q in Fig. 5(a) store the same logic value] and 2) the accessed cell stores the opposite data as the unaccessed cell [Fig. 5(b)].

Let us first consider the read operation. Before the read operation commences, CM0 is in the insulating state, and voltage across the node S0 is less than V_{CIMT}. When the word line is asserted, read current prompts an increase in V_Q, resulting in a current flow through S0 to CM0. If the unaccessed cell stores the same data as the accessed cell [Fig. 5(a)], U_PD0 is ON, which leads to an additional current path through S0 to node U_Q. This reduces the current through CM0 and leads to an additional delay in charging S0 to $V_{\mathrm{C,IMT}}$, thereby delaying the IMT in CM0. The cell must be designed considering this worst case. In other words, the design should be such that: 1) CM0 undergoes IMT in the presence of the current through the unaccessed cell and 2) the data in the accessed cell does not flip even with the additional delay in phase transition due to the unaccessed cell. With the initiation of the IMT in CM0, both Q and U_Q are discharged. Note, transistors PD1 and U_PD1 are OFF, eliminating any current flow through them. Thus, QB and U_QB remain at V_{DD}. When the unaccessed cell stores the opposite data as the accessed cell (U_Q at "1" and Q at ""0"), there is no current path through U_PD0 [see Fig. 5(b)] as it is OFF the entire time during the read operation. Thus, the phase transition time in CM0 is lower compared with the previous case. The other branch of the accessed cell storing "1" has its pull-down transistor OFF, thereby keeping the corresponding CM in its insulating state and allowing no current to flow through the unaccessed cell.

Let us now discuss the effect of CM sharing on the write operation. Since writing into the SRAM is primarily initiated by the current flow from pull-up via access transistor, the pull-down transistor plays an auxiliary role. Hence, the additional current paths do not have a significant effect on the write ability of the accessed transistor. It may be noted that the additional current paths through the unaccessed cell are similar to those in the read operation, as shown in Fig. 5. Thus, if the initial data in the accessed cell is the same as the unaccessed cell, there is a current path in the branch of the unaccessed cell storing "0" (U_PD0). Once the opposite data is written into the accessed cell, the current ceases to flow as PD0 turns OFF. If the initial data in the accessed cell is opposite to that in the unaccessed cell, there is no additional current path in the initial phase of the write. Once the data is written, the bitline voltage at 0 reinforces the voltage at the node U_Q, as long as WL is asserted, thus maintaining the stability of the unaccessed cell.

However, the current through the unaccessed cell during read and write when the data in the accessed and unaccessed cells is the same affects the stability of the unaccessed cell. The voltage at node U_Q storing "0" rises, as a result of which, the data may be flipped. But, it is reassuring to note that the rise in the voltage at U_Q cannot be greater than the rise in the voltage at Q, since the current direction is from Q to U_Q. Hence, the stability of the unaccessed cell cannot be worse than that of the accessed cell during read. In other words, the bottleneck for array stability will be the accessed cell. We will quantify this important aspect of the proposed design comparing the stability of the accessed and unaccessed cells in Section VI.

TABLE I
CM MODEL PARAMETERS USED IN SIMULATIONS

Parameter	Value
Thickness (nm)	20
Width (nm)	30
Length (nm)	55
J_{CMIT} (A/cm^2)	5.31x10^9
J_{CIMT} (A/cm^2)	5.3 x10^6
$\rho_{INSULATOR}$ (Ω·cm)	0.85
ρ_{METAL} (Ω·cm)	3.7 x10^{-5}
IMT time (ps)	50
MIT time (ps)	50
Capacitance (fF)	2

V. DEVICE-CIRCUIT CODESIGN

In this section, we discuss the design methodology, considering the sharing of the CM amongst the neighbouring cells. To quantitatively evaluate the impact on cell stability and write ability, we perform simulations employing 20-nm predictive technology models for FinFETs [12] and an in-house SPICE model for the CMs. The resistivities in the metallic and insulating states (ρ_{METAL} and $\rho_{INSULATOR}$), the critical current densities for IMT and MIT (J_{CIMT} and J_{CMIT}), and the geometry of the CM (length L and cross sectional area A) serve as the model inputs. It triggers phase transitions by constantly monitoring the current flow in the CM during circuit operation and comparing it with $I_{C,IMT}$ and $I_{C,MIT}$. For the successful read operation, there is a charging delay involved to charge capacitance at the node S0 to V_{CIMT}. This is the combination of CM and the transistor capacitances. After the voltage at node S0 reaches V_{CIMT}, CM0 will take a finite time to completely transition to a metallic state. Hence, the read delay is a function of both IMT switching time and RC charging delay. Table I shows the CM capacitance used in the model. The model has been validated by comparing the predicted current–voltage (I–V) characteristics to our experimental measurements. We design the SRAM cell with 1, 1, and 2 fins in the access, pull-up, and pull-down transistors. The resistivity ratio of the CM ($\rho_{INSULATOR}/\rho_{METAL}$) is chosen to be $\sim 10^4$, as per our experimental observations and other literature on CMs like VO_2 [3]. Since the CMs exhibit a wide range of critical current densities ($J_{C,IMT}$ and $J_{C,MIT}$), we obtain a range of these values to trigger the selective phase transitions in CMs during the read and write operations. To bring in the array context into simulation, we calculated the BL/BLB capacitance for an SRAM array of 256 cells in the column including the routing capacitance. This is done by adding the gate to drain capacitance of 256 access transistors. In addition, the bitline routing is calculated to be $\sim$100 μm for connecting all the 256 cells of the column based on the layout. The capacitance per unit length is estimated from [13] and appropriately scaled for 20-nm technology. Similarly, the wordline capacitance was estimated by considering the gate capacitance of 256 cells in a row and the interconnect capacitance based on the wordline length obtained from the layout. The results are obtained considering these parasitics. For this paper, the cross-sectional area of the CM is fixed to be equal to the contact size. (If the CM is grown in a backend layer, a larger area may be used as per the design requirements). We identify the range of length of CM (L) for which IMT is triggered in CM0 but not in CM1 during read. L affects the resistance as well V_{CIMT} ($= \rho^*_{INSULATOR} J^*_{CIMT} L$), and therefore, is a critical factor determining how fast the nodes S0 and S1 are charged to $V_{C,IMT}$. Very large values of L lead to slower charging of S0, which delays the IMT in CM0 and deteriorates the access time and stability. On the other hand, if L is too small, low value of $V_{C,IMT}$ may trigger IMT in both the CMs and not achieve the benefits of read stability as discussed before. We design the cell by sweeping L and monitoring the state of CM0 and CM1 during the read operation, thus identifying the feasible range of L. Fig. 6 shows the time to achieve IMT from the time WL is asserted. It can be observed that time to IMT for CM1 is always larger than that for CM0, since the resistance of PD0 (in the ON-state) is less than PD1 (in the OFF-state), as discussed before. We categorize Fig. 6 into three regions to determine the ideal length of CM for a robust operation. When the length of the CM is between 30 and 42 nm, we see that both CM0 and CM1 will undergo transition when the wordline is kept high for a longer duration. For the cell to operate in this region, the read wordline pulse must be greater than the time to IMT for CM0 and less than that for CM1. When L is greater than 42 nm, CM1 practically ceases to transition into the metallic phase. Hence, for 42 nm $<$ L $<$ 60 nm, the design is not constrained by an upper bound on the read pulse width and offers a larger design flexibility for determining the array organization. When the length is greater than 60 nm, even though IMT is observed in CM0 and read operation is possible, time to IMT grows exponentially. This will directly affect the read time of the cell and it may not be beneficial to operate in this region. Table I summarizes the CM parameters with the length obtained from the codesign approach presented before. These values are used for the rest of the analysis.

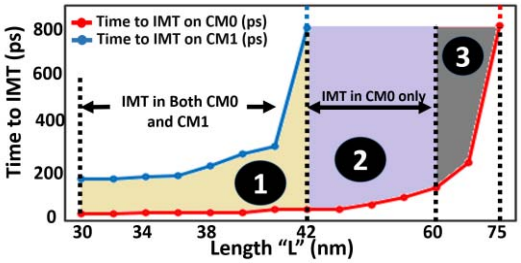

Fig. 6. Length selection for selective phase switching.

VI. ANALYSIS AND RESULTS

A. Read Analysis

To evaluate the read operation, we perform static and dynamic analyses. Read SNM analysis shows a 30% increase in the read stability compared with standard SRAMs [Fig. 7(a)], which is explained as follows. As the voltage V_Q is increased from 0, the output voltage at QB (V_{QB}) remains at V_{DD} till the CM undergoes IMT. This is due to

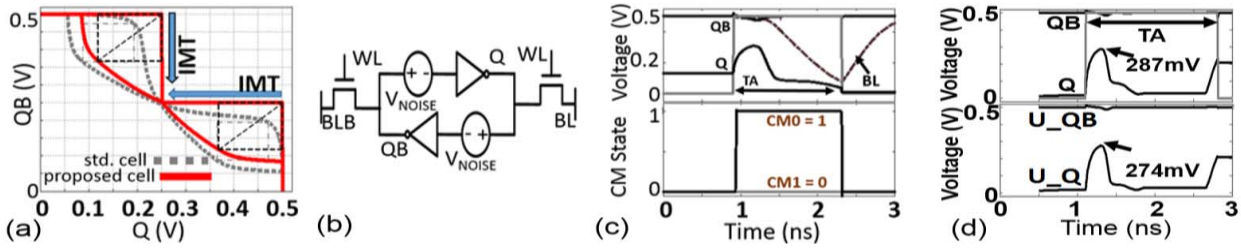

Fig. 7. (a) Read SNM compared against standard 6T SRAM (standard). (b) Circuit representation with noise sources attached for dynamic noise analysis. (c) Waveforms corresponding to successful read operation. (d) Behaviour of unaccessed cell sharing the CM during read operation.

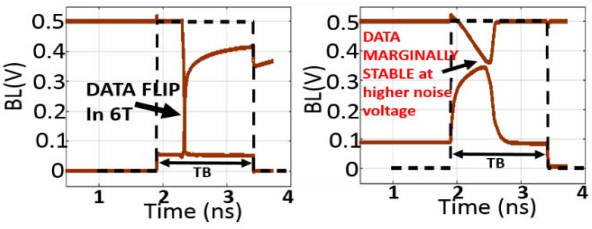

Fig. 8. (a) Data flip in the presence of the noise source (beyond 185 mV) with standard 6T SRAM. (b) Showing minimum point of stability with the proposed design.

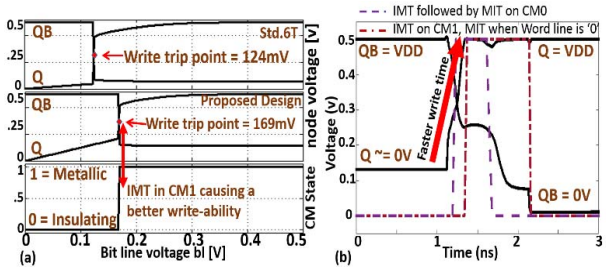

Fig. 9. (a) Write margin. (b) Transient analysis of write with CM0 undergoing IMT followed by MIT.

high insulating state resistivity of the CM, due to which the pull-up pMOS holds the data virtually unopposed by the pull-down path. This increases V_M of the inverter formed by PU1, PD1, CM1, and AX1, making the node QB more immune to noise compared with standard SRAMs. Only when V_Q is sufficiently large and the current exceeds I_{CIMT}, we notice an abrupt change in the VTC. After IMT, the butterfly curve is similar to that of standard SRAM, except for an increase in V_{QB} for $V_Q = V_{\text{DD}}$, which is due to a finite metallic state resistance of the CM. Note from Fig. 7 that the CM operates in the insulating phase for the corresponding output voltage in the logic "1" state, while it is in the metallic phase for logic "0" output, as per the design requirements (see Section III-B). Fig. 7(a) clearly shows a larger lobe in the SNM curve, representing the enhanced read stability.

Since proposed cell operation is based on the phase transitions of the CM and the relative time constants associated with charging of S0 and S1, it is critical to perform the dynamic read analysis for proper evaluation of the cell. The dynamic read operation shown in Fig. 7(c) illustrates that the transient increase in the internal node voltage (V_Q) does not flip the data as IMT is initiated on CM0. CM1 stays in the insulating phase during the entire read operation. To evaluate the read stability, noise sources of appropriate polarity (opposite to the internal node voltages) are introduced as shown in Fig. 7(c) and transient read operation is simulated to measure the noise voltage (V_N), which flips the data in the cell. The immunity of standard 6T SRAM cell to this noise is up to $V_N = 185$ mV, above which the voltages at nodes "Q" and "QB" are flipped [see Fig. 8(b)]. The corresponding immunity to the noise voltage for the proposed design is up to 220 mV. Thus, the proposed design achieves 30% improvement in read stability. However, selective IMT on the CMs to enhance the read stability adversely affects the read time. Given the fact that the precharged bitline voltage does not discharge until IMT occurs in CM0, time to IMT along with the internal node discharge increases the read time by 28%. This can be controlled by judiciously choosing the CM with a smaller time associated with IMT and smaller $J_{\text{C,IMT}}$ values.

B. Write Analysis

To evaluate the write operation, we perform direct current (dc) and transient analysis for comprehensive comparison. Write margin (WM) is obtained by sweeping the BLB voltage [14] from V_{DD} to 0 (with BL at V_{DD}). WM is defined as the BLB voltage value at the point when Q and QB flip [Fig. 9(a)]. Our proposed design has 36% more write margin compared with 6T cell. This analysis concludes that the proposed design suppresses the conflicting read and write design requirements. We also perform dynamic write analysis in the presence of the unaccessed cells. Fig. 9(b) shows the write operation. CM0 undergoes IMT as S0 charges beyond V_{CIMT} followed by MIT as V_{QB} reduces which lowers the current below I_{CMIT}. As explained in Section III and Section IV, V_Q increases due to the combined effect of the insulating state resistance of CM0 and the increased resistance of PD0 as V_{QB} reduces. Increase in V_Q triggers IMT in CM1, which further helps in the discharge of QB and improves write ability. We observe 29% improvement in the write time of the proposed SRAM cell compared with the standard SRAM.

C. Hold Analysis

To demonstrate the hold stability of this cell and to capture the effect of phase transition of CMs, a surge of noise voltage is introduced during the standby mode at the internal node

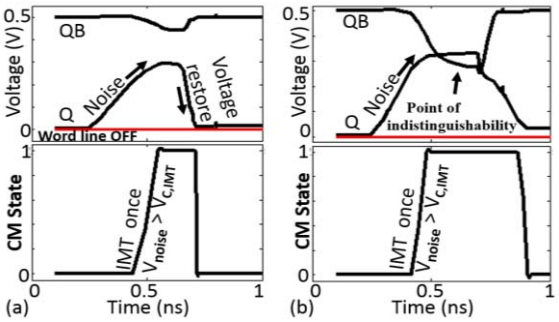

Fig. 10. (a) Data retention during hold mode in the presence of noise. (b) Node data indistinguishable or flipped beyond certain voltage value.

storing "0." When the noise voltage is sufficiently less than $V_{C,IMT}$ of the CM, node voltage V_Q rises but this is not sufficient to turn ON PD1 and upset the hold stability. When the noise voltage becomes equal to $V_{C,IMT}$ of the CM, phase transition occurs and node voltage is restored back to zero (Fig. 10) with a low resistance discharge path to GND, thereby maintaining the hold stability. As per our simulation results, dynamic hold stability is maintained for a maximum noise voltage of 320 mV, while the standard 6T hold stability is affected by any noise voltage beyond 200 mV. As discussed in Section III-A, an improvement in hold stability is attributed to the increase in the V_M of the inverter formed by PU1, PD1, and CM1 due to insulating state resistance of CM1 (similar to read stability). Thus, even if the node storing 0 rises due to noise, it is not sufficient to flip the data. Moreover, IMT in CM0 for $V_{S0} > V_{CIMT}$ pulls down Q to 0, thus maintaining high hold stability. During standby mode, FET ON-state resistance (in series with the CM0) is sufficiently low, and we have designed the relative resistance ratio of the FET to the CM to be smaller than the particular value above which oscillations can be observed in the CM because of change in V_Q [15].

D. Stability of the Unaccessed Cells

To analyze the effect of CM sharing on the stability of the unaccessed cell (discussed in Section IV-B), we carefully monitored the node voltage fluctuations [U_Q and U_QB in Fig. 7(d)] during the read and write operations on the accessed cell. Fig. 7(d) shows the worst case scenario (read operation when the accessed and unaccessed cells have the same data) in which there is a maximum current flow to the unaccessed cell (see Section IV-B). The voltage across the node storing zero (U_Q), rises similar to Q (of the accessed cell) but by a smaller magnitude. Since the V_M of this inverter formed by PU1, PD1, and CM1 is significantly increased, the rise in U_Q is not sufficient to disturb the data in the cell. Once the voltage across the CM reaches $V_{C,IMT}$, Q and U_Q are discharged and stability of both accessed and the unaccessed cell is reestablished. Similar to the read stability analysis, we introduce noise sources in the unaccessed cell while the read and write operations are performed. Data instability is observed for noise voltage >260 mV, which is greater than that observed for the accessed cell. Hence, the unaccessed cell does not serve as the bottleneck for stability, as discussed in Section IV-B. Note, the array stability of the proposed technique is larger than that for the standard SRAM, as per the results in Section VI-A.

TABLE II
COMPARISON WITH STANDARD 6T ($V_{DD} = 0.5$ V)

	6T cell	Proposed Design	Improvement
Read SNM (mV)	103	134	30%
Write margin (mV)	124	169	36%
Leakage Power (nW)	2.49	1.245	50.1%
Read Time (ps)	63.4	88	-28%
Write Time (ps)	46.6	33	29.18%
Layout Area	6 Fins X 2 poly pitch	6 Fins X 2 poly pitch	0%

E. Leakage

Another advantage of the proposed cell is leakage reduction, which is attributed to lower OFF current in HyperFETs compared with standard transistors [see. Fig. 1(b)]. Our analysis shows that our design achieves 50% reduction in the cell leakage compared with 6T SRAM cell.

Table II summarizes analysis results and the comparison against the standard 6T SRAM cell. All the analyses presented in this section have been done in the presence of unaccessed cell sharing the CMs with the accessed cells.

F. Cell Sizing Considerations

In this paper, our objective is to quantitatively address the read–write conflicting design requirement of an SRAM cell by using the CM. For this, we chose the bitcell with 1, 1, 2 (pull-up, access, pull-down) sizing, which is by design itself favors read stability. Since one of the key benefits of our technique is the improvement in read stability, we chose 1, 1, 2 sizing to have the reference/standard cell optimized for large SNM. However, we have performed the analysis for a high-dense and compact SRAM cell with 1, 1, 1 sizing. we get 20% improvement in write margin and 25.5% improvement in read SNM, 26% smaller write time, and 32% read time penalty (as compared with the standard 6T with 1, 1, 1 sizing).

G. Process Variations

Similar to conventional SRAM design, our proposed design also shows the degradation with worst case transistor threshold voltage (V_{TH}) mismatch. However, in addition to V_{TH} mismatch of the host transistor, the CMs will introduce an additional source of variation as their length and area may show variation, which will change the hysteresis/resistance of the CM. In addition, the IMT/MIT switching times may show variations. To analyze this effect, we have performed an analysis with ±50 mV worst case V_{TH} deviation in each transistor, ±5% worst case variation in the length and area of the CMs and ±10% worst case deviation in the switching times. Considering these variations simultaneously, we compare the 6T SRAM and the proposed technique. We still see an enhancement in the design metrics, but reduced in magnitude

TABLE III
VARIATION ANALYSIS

	6T cell	Proposed Design	Improvement	6T cell (50mv Vth variation)	Proposed design (50mv Vth variation + 5% CM geometry variation + 10% switching time variation)	Improvement
Read SNM (mV)	103	134	30%	83	98.3	18.43%
Write margin (mV)	124	169	36%	110	128	16.36%
Read Time (ps)	63.4	88	-28%	88	134	-52.2%
Write Time (ps)	46.6	33	29.18%	41.4	34.6	16.42%

compared with the proposed design not accounting for any variations. Table III summarizes the metrics with and without variations.

VII. CM RELIABILITY AND OTHER DESIGN ASPECTS

The novel SRAM design discussed in Section III, IV, V and VI is meticulously coupled to the properties of the CM. A wide variety of CMs, with a wide range of resistivity ratios and hysteresis, have been reported so far [11], and a large research effort is directed toward further exploration of new materials. In addition, the inherent properties of a CM can be tailored through ingenious use of strain [8]. Hence, there is ample flexibility in choosing the best set of material properties to maximize benefit of the proposed SRAM. However, it is vital to choose materials with IMT/MIT switching time, which is sufficiently smaller than the target read/write delays. Based on our experimental data on VO_2 and simulation-based projections, switching time of $\sim$50 ps is estimated for scaled CM films (which are used in our analysis before). We focused on low-voltage operation (0.5 V) of SRAMs and at such low voltages, the inherent delay of the transistor is larger than the CM switching time. Despite that, we observed a penalty in read access time, which can be reduced by choosing a CM with better switching characteristics. In any case, the proposed SRAM is suitable for ultralow power applications, such as implantable or wearable devices, in which SRAM stability (and not performance) limits low voltage operation.

In addition to the switching speed, CMs must also exhibit proper thermal stability within the operating range. Materials such as NbO_2 show stability up till temperatures as large as 1080 K. For reliability of the design, the CM must have satisfactory endurance. HyperFET is an emerging device and yet to be evaluated in terms of reliability. Although data for reliability is not available so far for the compound HyperFET (transistor and CM), the endurance has been reported in the literature. The prototypical demonstrations [3] and [16] of HyperFET were made using VO_2 as CM having a reliability of $>10^9$ cycles [17], and still in its nascent stage of development. Prior to selecting a material for the proposed SRAM structure, consideration of such aspects is also critical.

VIII. CONCLUSION

In this paper, we propose a novel technique of designing an SRAM by employing CMs in the pull-down path of the cell. This paper utilizes the phase transitions of CMs to achieve enhancement in the read stability, write ability, hold stability, and leakage power reduction. Proper codesign of the cell discussed in this paper enables selective phase transitions in the CM depending on the data stored in the cell, which mitigates the read–write conflict. Layout analysis of the cell showed that the design can be realized with no additional layout penalty, if the CMs are shared amongst the neighbouring cells in a column. We performed an extensive analysis of the impact of CM shared by the accessed and unaccessed cells and analysed their stability. We discussed the role of the phase transitions in the CMs in enhancing read, write, and hold stability. Our analysis shows 30% improvement in the read stability, 36% improvement in write margin, data retention in the presence of higher noise as well as 50% reduction in the leakage current due to a lower OFF current of the HyperFET structure. This comes at the cost of 28% increase in the read time. This can be controlled by judiciously choosing the CM with a smaller time associated with IMT and smaller $J_{C,IMT}$ values. Overall, the proposed design is suitable for on-chip SRAMs for ultralow power systems operating at low voltages.

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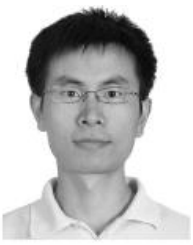

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