

# Exploration of Low-Power High-SFDR Current-Steering D/A Converter Design Using Steep-Slope Heterojunction Tunnel FETs

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**Abstract**—Steep-slope heterojunction tunnel field-effect transistor (HTFET) devices promise new opportunities beyond CMOS in low-power high-performance communication applications. In this paper, the circuit design optimization of a low-power 14-bit 1-GS/s current-steering digital-to-analog converter (DAC) using 0.4/0.3 V mixed-supply HTFETs is explored. Based on the device characteristics comparison and circuit analysis, it is shown in this paper that HTFET endorses significant differences in both  $I$ - $V$  and  $C$ - $V$  due to the steep-slope tunneling mechanism and a nature of vertically fabricated structure. While such differences significantly affect the circuit design corners, this paper gives the device-circuit co-optimization for the HTFET DAC, reaching at higher current source output impedance, less nonlinear switching glitch distortions, and thus superior spectral performance over the Si-CMOS DAC. HTFET device variation is also discussed, and calibration techniques are adopted for the static matching accuracy.

**Index Terms**—Digital-to-analog converter (DAC), low power, matching, spurious-free dynamic range (SFDR), steep slope, tunnel field-effect transistors (TFETs).

## I. INTRODUCTION

HIGH-PERFORMANCE current-steering digital-to-analog converters (DACs) have widely been used in various wideband transceivers in wireless communication systems [1]–[4]. Fig. 1 shows a current-steering DAC diagram, which consists of a series of parallel weighted current sources switched by the input digital signals through decoder and synchronized latches. For most wideband transceiver systems,

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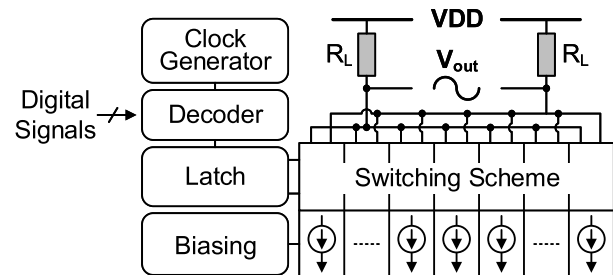


Fig. 1. Block diagram of a current-steering D/A converter.

the key specifications in DACs are the dynamic spectral performance, such as the spurious-free dynamic range (SFDR). This SFDR has widely been used to evaluate performance for wideband DAC designs [1]–[5].

In current wideband CMOS DAC designs, the primary bottlenecks include the finite output impedance, switching glitches, and current source mismatches [2], [3], [5], [6]. To relieve these bottlenecks and to achieve a high SFDR in existing CMOS DAC designs, some techniques have already been proposed, such as the complementary switched current source technique to mitigate the effect of finite output impedance at the cost of additional power [3], the calibration techniques to improve the matching performance [7], [8], and randomization and return-to-zero (RZ) techniques [6] to reduce effects of switching glitches [8]–[10]. However, the high-SFDR wideband DAC designs in deep-submicrometer CMOS technologies have become a challenge due to severe deterioration of intrinsic transistor gain ( $g_m \cdot r_o$ ), output resistance ( $r_o$ ), and transconductance over drain-current ( $g_m/I_{DS}$ ) in spite of these techniques for higher SFDR [9].

It is noted that not only high performance but also low power is crucial for such DAC designs in broadband systems, especially when the power budget is limited by batteries [2]. One example is the portable software-defined-radio communication system with broadband transceiver carried by a soldier [5]. However, the tradeoff between high performance and low power limits the design space of existing CMOS DAC designs. Meanwhile, it is beneficial to tackle such bottlenecks in CMOS design tradeoff by exploring more design freedom from other perspectives, one of which is making use of

different process technologies. Some effects have been carried out through the exploration of existing process technologies, such as BiCMOS and GaAs, to obtain both high signal bandwidth and higher SFDR simultaneously [11], [12].

This paper focuses on the emerging beyond-CMOS steep-slope tunnel field-effect transistor (HTFET), specifically, the GaSb-InAs heterojunction HTFET [13]–[18] which has been evaluated to achieve both higher performance and lower power consumption compared with CMOS in digital logics [13]–[19].

Recently, quite a few HTFET analog and RF circuit designs have also been proposed by taking the advantageous and even unique characteristics, such as the high transconductance over current ratio ( $g_m/I_{DS}$ ), unidirectional conduction behavior, and low-voltage operation, especially below 0.5 V benefiting from sub-60-mV/decade subthreshold voltage swing [14], [16]. In this paper, we explore the DAC design using a 20-nm HTFET process [18] through the investigation of the device-circuit codesign and optimizations, revealing the benefits of using the HTFET technology in low-power high-SFDR D/A conversion.

In the rest of this paper, Section II discusses the design challenges and introduces the HTFET device features and potential design space extension by HTFETs for DAC designs. Section III describes the design optimizations for the 14-bit 1-GS/s DAC. Section VI presents the simulation results. Finally, the conclusion is drawn in Section V.

## II. EXTENDED DESIGN SPACE BEYOND CMOS

### A. Challenges in CMOS DAC Design

In wideband DAC designs, SFDR is one key spectral performance merit limited by the output impedance ( $Z_{OUT}$ ) in the desired bandwidth [2], [10], [21]. The relationship between SFDR and  $Z_{OUT}$  is

$$\text{SFDR} = 20 \cdot \log \left( \frac{4 \cdot Z_{OUT}}{N \cdot R_L} \right) \quad (1)$$

$$Z_{OUT} \approx R_o \parallel \frac{1}{j\omega C_o} \approx \frac{R_o}{1 + j\omega R_o C_o} \quad (2)$$

where  $R_L$  is the load resistance,  $N$  is the number of unary-weighted current sources, and  $R_o$  and  $C_o$  are equivalent first-order output resistance and capacitance, respectively. Consequently, to achieve a high SFDR,  $Z_{OUT}$  modeled by  $R_o$  and  $C_o$  should sufficiently be high in the bandwidth [2]–[4], [7], [21]. In deep-submicrometer CMOS, the output resistance ( $r_o$ ) is severely lowered due to the short-channel effects [1]. On the other hand, using long-channel devices to increase the output resistance significantly increases the output capacitance, and unfortunately lowers  $Z_{OUT}$  at the high-frequency range. As a result, achieving a high  $Z_{OUT}$  for wideband CMOS DAC designs remains as a challenge. In this section, the potential bottlenecks derived from nanometer CMOS technologies in current-steering DAC designs introduce first.

1) *Degradation of  $Z_{OUT}$* : Advanced CMOS technologies offer several advantages with respect to circuit properties, such as smaller dimensions, better high-frequency operation,

and power efficiency. However, the drawbacks of those CMOS technologies, such as signal swing limitations due to decreased supply voltage and gain reduction due to lower transistor output resistance ( $r_o$ ), are introduced [21]. As delineated in (2), the resistive portion represents the highest output impedance achieved at a low frequency. As the frequency increases, the output capacitance gradually reduces the output impedance with a linear slope of 20 dB/frequency decade [1], [8], [10]. Hence, a large  $r_o$  with a small  $C_o$  is desired to achieve a high SFDR. However, in advanced CMOS technology, a large  $r_o$  is achievable only with a large gate length, which makes it impossible to achieve a small  $C_o$ . Even with a small gate length, a 70-dB SFDR requires a current source design with less than 7-fF capacitance in the 6-bit most significant bits (MSB) segment of a DAC, which is extremely difficult to satisfy. Some techniques, such as always-on biasing [21] and complementary current [3], help to reduce the burden, but the output impedance requirements continue to be one major design bottle neck. Meanwhile, a small transistor size for small capacitance is vulnerable to current source mismatch. To satisfy the matching accuracy, a large transistor size has widely been used for high-SFDR uncalibrated DACs, which further narrow the design space and making tradeoffs complicated and difficult.

2) *Matching Accuracy*: The current source matching accuracy determines the static integral nonlinearity (INL) in DACs, which should meet the DAC resolution so as not to deteriorate the spectral performance [8], [9]. However, CMOS transistor mismatches are increasing and becoming complicated with  $V_{TH}$  mismatch by the effective work-function variations (WFVs) in advanced CMOS technologies [13], [21], [22]. To improve matching, techniques, such as using large-size transistors [24], layout modifications [24], [25], or dynamic element matching [9], [24], have already been used to compensate the static mismatch. For higher resolutions, it is apparent that calibrations or similar techniques like sigma-delta modulations [26] will be inevitable to meet the static linearity requirement at the cost of additional power and area.

3) *Nonlinear Distorted Switching Glitches*: The code-dependent glitch energy leads to nonlinear distortion of signals, resulting in SFDR deterioration in current-steering DACs. The glitch mainly originates from the imperfect synchronization of the switching signals at input gates in switching transistors, the clocked switch control signals fed through the transistor and interconnection capacitance, and current source variations [21], [27]. To attenuate the glitch, useful techniques such as the cross-over voltage control and switching signals synchronization with latches, low-voltage gate control of the switches, RZ, non-RZ [6], digital-random RZ (DRRZ) [3], and time-relaxed interleaving DRRZ [3] can be utilized. However, among these methods, the randomization may lower the signal power and make the timing design of high-speed DACs more challenging with RZ techniques, or reduce the signal-to-noise ratio (SNR) with higher noise floor when randomization is applied which limits the applications where SNR is critical.

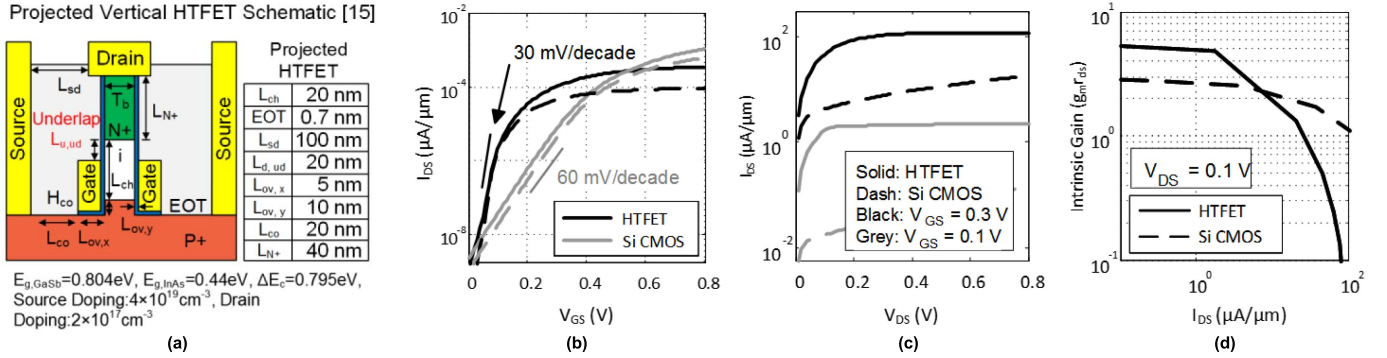


Fig. 2. (a) Projected vertical double-gate III-V HTFET structure [15], [18]. (b)  $I_{DS}$  versus  $V_{GS}$  for HTFET and Si-CMOS at  $V_{DS} = 0.1$  V (dashed line) and 0.3 V (solid line). (c)  $I_{DS}$  versus  $V_{DS}$  for HTFET and Si-CMOS at  $V_{GS} = 0.3$  and 0.1 V. (d) Intrinsic gain ( $g_m \cdot r_o$ ) of HTFET and Si-CMOS at  $V_{DS} = 0.1$  V.

4) *Power Consumption*: The DAC power includes the output signal power, and the power consumed for the current source and switch units and the digital decoder and latches to drive the switches. Since the output signal power is determined by the applications, lowering the DAC power comes from the digital circuits and the current sources and switches. In CMOS process, the limitation of energy slope of  $kT$  ( $k$  is the Boltzmann constant and  $T$  is the absolute temperature) in Fermi-Dirac distribution leads to a thermal-energy limited subthreshold slope (SS) of  $(kT/q) \cdot \ln 10$ , and it is challenging to further scale down  $V_{DD}$  and power [13] for digital control logics in the DAC. For the current sources, the challenge in reducing the power with fixed amount of current lies in how to reduce the drain-source voltage ( $V_{DS}$ ) of the transistors operating in the saturation region while maintaining sufficient output resistance to meet the current accuracy requirement as introduced above. Meanwhile, the above-mentioned techniques, such as the always-on biasing, calibration, and RZ techniques, increase the power significantly.

### B. New Design Space Brought by HTFETs

Steep-slope TFETs have emerged as alternative device candidates to further reduce the supply voltages for low-power applications [13], [14], [28], [29]. It employs the band-to-band tunneling induced carrier injection mechanism in a reserved biased and gated p-i-n diode structure with a  $<60\text{-mV/decade}$  SS of tunneling current, while Si-CMOS has a  $60\text{-mV/decade}$  SS originating from thermionic emission induced carrier injection mechanism [13], [14]. Among different types of TFETs, GaSb-InAs (III-V) HTFETs exhibit simultaneous enhancement of the tunneling current ( $I_{ON}$ ) and ON-/OFF-state ratio ( $I_{ON}/I_{OFF}$ ) with the heteroband alignment to reduce the effective tunneling barrier at the source-channel junction [12]. It consequently shows a comparable  $I_{ON}$  with subthreshold CMOS [13]–[15], [28], [29] with significant energy-efficiency advantages. In addition, Fig. 2(a) shows the device structure, which is constructed vertically. The current ( $I_{DS}$ ) flows perpendicular to the wafer, and such a vertically fabricated HTFET reduces the footprint area.

Here, we introduce the expanded design space with unique HTFET device characteristics for the current-steering DAC design.

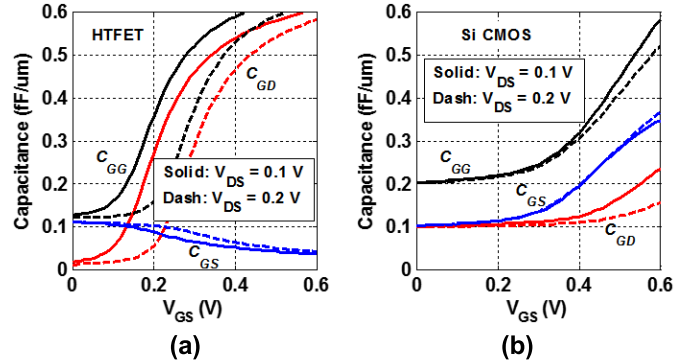


Fig. 3.  $C_{GD}$  (red line),  $C_{GS}$  (blue line), and  $C_{GG}$  (black line) characteristics of HTFETs in (a) Si-CMOS and (b) HTFET exhibits the lower capacitance than the Si-CMOS at  $V_{GS} < 0.2$  V.

1) *Steep-Slope Switching and No Gate-Length Modulation*: Fig. 2(b) and (c) shows the comparisons of drain-source current behaviors according to biasing voltages, such as  $I_{DS}$  versus  $V_{GS}$  and  $I_{DS}$  versus  $V_{DS}$  of 20-nm HTFET [18] compared with 20-nm Si-CMOS [13], [14]. HTFETs exhibit an average  $30\text{-mV/decade}$  SS due to the gate-controlled interband tunneling mechanism. This enables a significantly lower  $V_{DD}$  to lower than 0.5 V for the digitally controlled circuitry, including the binary-to-segmented decoder and clock distributions. This also enables a reduction of the gate-source driving voltage ( $V_{GS}$ ), leading to low-voltage biasing and switching with 0.3 V latches. Although it has been reported that the difference between the drain-source voltage  $V_{DS}$  of saturated TFET transistors and the overdrive voltage ( $V_{OV} \approx V_{GS} - V_{TH}$ ) is larger than CMOS due to the existence of drain-threshold voltage ( $V_{DTH}$ ) caused from the superlinear behavior of TFETs [30], as shown in Fig. 2(c), HTFETs have almost no gate-length modulation and thus require less  $V_{DS}$  than CMOS which helps reduce the analog voltage supply. Such characteristics contribute to both low-voltage and low-power advantages.

2) *High Output Impedance  $Z_{OUT}$* : Insufficient  $Z_{OUT}$  is one bottleneck in high-SFDR DAC designs for wideband DACs, as it is dominated by the parasitic transistor capacitance in the current routes. The capability of biasing the transistors at a voltage with less parasitic capacitance, together with a high intrinsic transistor gain ( $g_m \cdot r_o$ ), as shown in Figs. 2(d) and 3(a), helps increase  $Z_{OUT}$  and related SFDR.

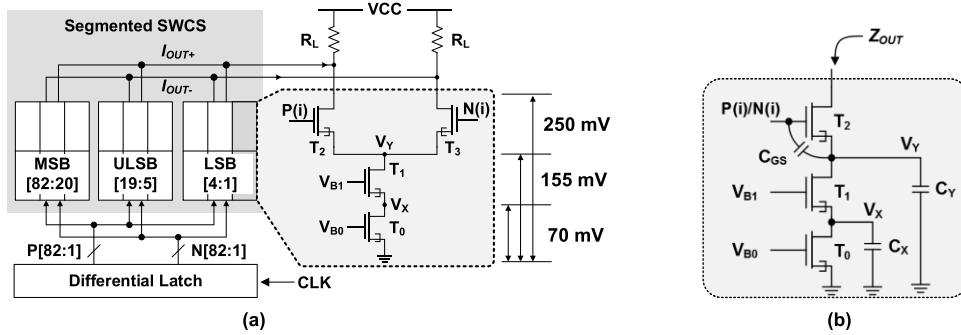


Fig. 4. (a) Description of array segmentations (MSB, ULSB, and LSB) and dc voltage distributions of SWCS unit cells. (b) Output impedance incorporating intrinsic capacitance with regard to  $C_{GS}$ ,  $C_{GD}$ , and  $C_{DS}$ .

3) *Nonlinear Coupling Distortion Suppression*: The ON/OFF switching operations introduce distorted nonlinear glitches at the current routes and deteriorate the SFDR, especially at high signal frequencies [3], [7], [8]. Fig. 3(a) and (b) shows less HTFET capacitance than Si-CMOS with low biasing  $V_{GS}$ , stemming from  $C_{OV}$  reduction because of a lower state density and III-V electron mass in HTFETs than CMOS [13]. As the coupling energy is proportional to the capacitance, the small capacitance at low-voltage HTFETs reduces the glitch energy and improves the SFDR.

4) *Current Source Matching Behaviors*: For high-performance DAC designs, the high resolution is also required and achieved by transistor sizing, physical layout floorplanning, or calibration techniques. Considering the tunneling mechanism different from CMOS, and the vertical HTFET process rather than a planar CMOS process, the transistor matching characteristics are still in the mist, even if some existing research has revealed that the TFET matching is vulnerable to the current variation compared with the Si-CMOS at a low voltage. In Section IV, we delineate the details of matching behaviors of HTFETs based on Synopsys technology computer-aided design (TCAD) Sentaurus simulations in current-steering DAC designs.

### III. CURRENT-STEERING DAC DESIGN USING HTFETs

In this section, the current-steering DAC design using steep-slope HTFETs is introduced with respect to fundamental building blocks and design specifications. The HTFET DAC has a power supply of 0.3 V for digital blocks, such as decoder and high-speed latches, and 0.4 V for the switched current sources (SWCSs). The full-scale current output is 6 mA, and the output voltage swing is 0.3 V with a  $50 \Omega$  differential load  $R_L$ . Fig. 1 describes the building blocks of the HTFET DAC, consisting of the SWCS array, a segmentation decoder, latches, and the biasing circuitry for the current sources. The 14-bit resolution of this DAC is segmented into 6T + 4T + 4B, i.e., six thermometer-coded MSB, four thermometer-coded upper-least significant bits (ULSB), and four binary-weighted LSB, as shown in Fig. 4(a).

#### A. Switched Current Source Cell

An SWCS is a fundamental component of a current-steering DAC, producing either positive or negative output at

a differential resistive load according to the digital-bit control at the differential switch pair. Fig. 4(a) shows the SWCS topology in n-type TFETs. It consists of a cascoded current source ( $T_0 - T_1$ ) and two switch transistors ( $T_2 - T_3$ ). The cascode transistor ( $T_1$ ) is connected in series with the transistor ( $T_0$ ) to increase the output resistance [2], [9], [21]. All SWCSs have the same circuit topology for LSB, ULSB, and MSB segments with scaled transistor size according to the bit weights.

As described in Section II-B, HTFETs have unique characteristics, such as a high  $g_m/I_{DS}$ , a high output resistance, a high intrinsic transistor gain  $g_m \cdot r_o$ , low-voltage operation, a late onset in the saturation region ( $V_{DSAT} > V_{GS} - V_{TH}$ ) due to the superlinear behavior [30], and an enhanced ON-state Miller capacitance effect [13], [31]. These characteristics mostly bring the benefits for designing of an SWCS. For example, a high  $g_m/I_{DS}$  affords the advantages with respect to operations at a low  $V_{GS}$  and  $V_{DS}$  in SWCS designs. This steep-slope characteristic also provides the transistor sizing benefit at even a low biasing voltage due to the high current density. One significant difference from the Si-CMOS circuit design, the gate length of an HTFET device does not contribute much to the tunneling current, which means that gate length could not be treated as an effective design parameter to tune the current or the matching property like in CMOS. For one thing, this prevents the challenging implementation of a varying gate length in a vertical structure. For another thing, no gate-length modulation effect improves the output resistance. For the third, matching design becomes different, as will be discussed later in this paper.

The principal aspects of the SWCS design can be classified into three portions: 1) the operation in the saturation region for all transistors for high output impedance; 2) low glitch energy due to the switching mechanism; and 3) sufficient matching accuracy. The tradeoff for SFDR according to 1) and 2) is shown in Fig. 5. All transistors work in the saturation region except one turned-OFF switch transistor (either  $T_2$  or  $T_3$ ), which is in the cutoff region. It is interesting that a larger  $V_{DS}$  is required to make all transistors work in saturation regions due to late onset of  $V_{DSAT}$  by the existence of  $V_{DTH}$  compared with the Si-CMOS as mentioned above. This larger  $V_{DS}$  significantly limits both minimum ( $V_{DD}$ ) and maximum biasing voltage  $V_{GS}$  for each transistor. As introduced in Section II-A, the spectral SFDR performance is a function

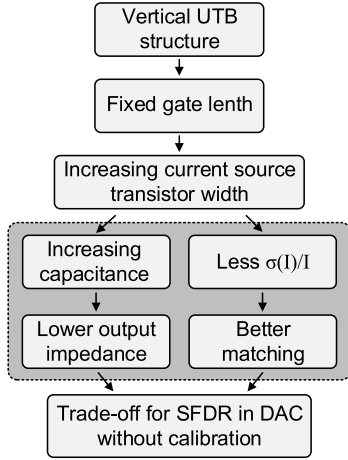


Fig. 5. Tradeoff for SFDR in the design of HTFET SWCS.

of  $Z_{OUT}$ . The small effective output capacitance at small biasing voltage, and the high output resistance in HTFETs could increase  $Z_{OUT}$  for higher SFDR.

1) *Large-Signal DC Operation*: Fig. 4(b) shows the dc voltage distributions in an SWCS at  $V_{DD} = 0.4$  V. The peak-peak output voltage ( $V_{PP}$ ) could be found out as

$$V_{PP} = V_{OUTP} - V_{OUTN} = 2V_{DD} - 2(V_{DSAT2-T2} + V_{DSAT-T1} + V_{DSAT-T0}). \quad (3)$$

Since HTFETs exhibit the late onset of the saturation due to the presence of  $V_{DTH}$  [30],  $V_{DSAT}$  of HTFETs ( $\approx V_{GS} - V_{TH} + V_{DTH} \approx V_{OV} + V_{DTH}$ ) is slightly higher than  $V_{DSAT}$  of CMOS at the same over-driving voltage  $V_{GS} - V_{TH}$ . This additional term,  $V_{DTH}$ , is a limiting factor in HTFET SWCS compared with CMOS SWCS designs. Therefore,  $V_{GS} \approx 100$  mV is applied to each transistor to ensure all transistors work in the saturation region at the given  $V_{DD}$  while retaining the desired output swing. This  $V_{GS}$  also helps to avoid large cross-coupling capacitance, because  $C_{GD}$  decreases as  $V_{GS}$  decreases, as shown in Fig. 2.

2) *High Output Impedance*: The output impedance  $Z_{OUT}$  could be expressed as

$$\frac{1}{Z_{OUT}} = \frac{1}{Z_{ON}} - \frac{1}{Z_{OFF}} \quad (4)$$

where  $Z_{ON}$  and  $Z_{OFF}$  represent the output impedance of the turned-ON branch and turned-OFF branch in the SWCS unit, respectively. At low frequencies, both  $Z_{ON}$  and  $Z_{OFF}$  are close to the dc output resistance, while at high frequencies,

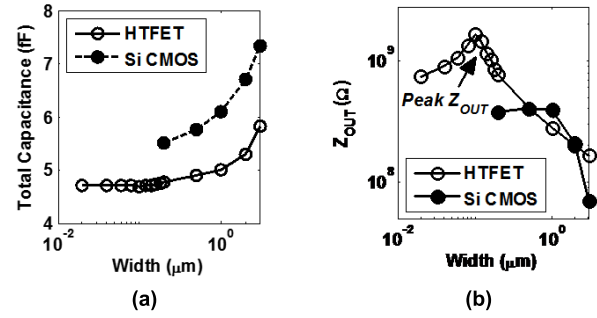


Fig. 6. Relationship between (a) average width of  $T_0$  and  $T_1$  and capacitance and (b) average width of  $T_0$  and  $T_1$  and  $Z_{OUT}$  at  $f_{Sig} = 500$  MHz.

$Z_{ON}$  and  $Z_{OFF}$  are mainly determined by the device, interconnection capacitance, and the intrinsic gain of the cascoded transistors (5)–(7), as shown at the bottom of this page, where  $A_{(i)}$  is the intrinsic saturation gain equal to  $g_{m(i)} \cdot r_{o(i)}$ . Unlike CMOS,  $C_{GD2}$  is not equal to  $C_{GD3}$  in (5)–(7), because the  $C_{GD}$  capacitance in HTFETs is more susceptible to  $V_{GS}$  compared with the Si-CMOS, as shown in Fig. 3.

For high output impedance, the two switch transistors  $T_2$  and  $T_3$  and the cascoded current source transistor  $T_1$  are minimally sized to reduce the device capacitance, as shown in Fig. 6(a). With the high  $g_m \cdot r_o$  of the transistors  $T_1$ ,  $T_2$ , and  $T_3$ , the impact of the capacitances  $C_X$  and  $C_Y$  in Fig. 4(b) on the output impedance  $Z_{OUT}$  is suppressed, as shown in (5)–(7). To find the optimal  $Z_{OUT}$ , the variance of  $Z_{OUT}$  is investigated with respect to various widths of transistor of  $T_0$  and  $T_1$ , as shown in Fig. 6(b). A peak  $Z_{OUT}$  is observed with an optimum transistor width of 200 nm for  $T_1$  and 40 nm for  $T_2$  and  $T_3$ . It stems from small capacitance at a small biasing voltage ( $\approx 100$  mV) and high  $r_o$  in fully saturation. If a smaller transistor width is used, a higher biasing voltage is required to obtain the same current, but it degrades  $r_o$ . This is because the transistors are not in full saturation with limited  $V_{DS}$ . On the other hand, if a larger transistor width is applied,  $Z_{OUT}$  also decreases because of more capacitance due to larger transistor width, even though the capacitance density [in fF/ $\mu\text{m}^2$ , as shown in Fig. 3(a)] is slightly lower.

In addition,  $Z_{OUT}$  and, thus, SFDR also depend on the parasitics originated from the interconnections and device layout structure. Therefore, the layout analysis for this vertical-structure HTFET in [40] is explored to extract the parasitics to get more accurate evaluation results of  $Z_{OUT}$  and SFDR. It is noted that no layout design rules of HTFETs are available from

$$Z_{ON} \approx \frac{1}{\frac{1}{A_2 A_1 r_{o0}} + j\omega \left[ C_{GD2} + \left( \frac{C_{GS2} + C_{GD1} + C_Y}{A_2} \right) + \left( \frac{C_{GS1} + C_{GD0} + C_X}{A_2 A_1} \right) \right]} \quad (5)$$

$$Z_{OFF} \approx \frac{1}{j\omega (C_{GD3})} \quad (6)$$

$$Z_{OUT} \approx \frac{1}{\frac{1}{A_2 A_1 r_{o0}} + j\omega \left[ (C_{GD2} - C_{GD3}) + \left( \frac{C_{GS2} + C_{GD1} + C_Y}{A_2} \right) + \left( \frac{C_{GS1} + C_{GD0} + C_X}{A_2 A_1} \right) \right]} \quad (7)$$

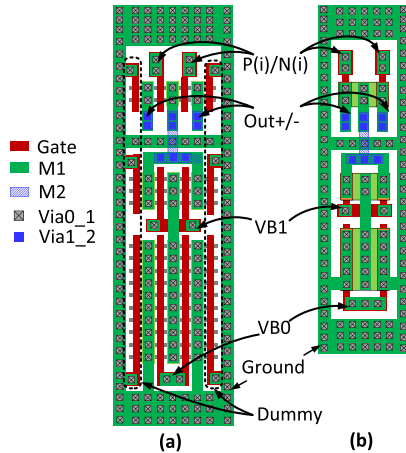


Fig. 7. Compact layout design of a current source and switch unit cell for (a) Si-CMOS and (b) HTFET.

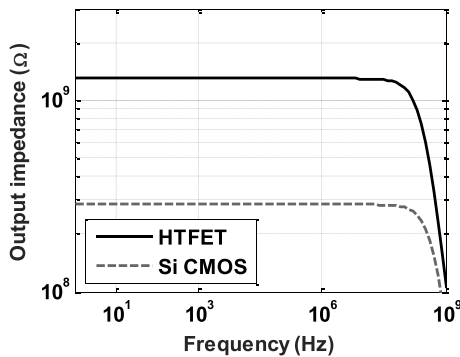


Fig. 8. SWCS output impedance in HTFET and Si-CMOS.

industry for at this time. Therefore, the widely used lambda ( $\lambda$ )-based design rules [32] were applied to study interconnect capacitances [33] with the assumption that  $\lambda$  is a half of gate length. Fig. 7 shows the layout design of a current source and switch unit cell in Si-CMOS and HTFET. The layout design is compact for less cell area and parasitic capacitance of interconnection lines. Dummy gates are used for better matching in the Si-CMOS cell. For HTFET, dummy gates are not added, because it is still unclear whether they help as the tunneling occurs in the vertical orientation, rather than the horizontal orientation in a planar MOSFET. The fringing capacitance and interconnection capacitance are extracted as [41] and [42]. Based on this layout, the HTFET unit cell exhibits much smaller layout footprint (even if dummy gates are not added to CMOS cells), and less extrinsic capacitance considering similar spacing design rules, the same wire width definition, and shorter interconnections. For parasitic resistance, because of minor performance impact on the current source and switch unit in the saturation region, it is not extracted or added into the DAC simulation in this paper.

Fig. 8 shows the output impedance ( $Z_{OUT}$ ) of SWCS within the entire Nyquist bandwidth with the transistor sizing and parasitic capacitance mentioned above. The simulation results show that  $Z_{OUT}$  of HTFETs is about seven times higher than that of Si-CMOS over the Nyquist bandwidth. It stems from not only high  $g_m \cdot r_o$  but also small capacitances (e.g.,  $C_{GS1} + C_{GD0} + C_X$ ) at given biasing conditions in the HTFET SWCS.

3) *Glitch Energy Reduction*: A glitch occurs in the current route when the current switches ( $T_2$  and  $T_3$ ) turn ON/OFF during the code transitions. The mechanism of such glitches is that the charging current and discharging current of the internal node  $V_X$  are different because of the charge transfer at node  $V_X$  due to the coupling from the gate control switching, simultaneous OFF-state of the switch pair, timing mismatches of the switching, and so on. As discussed in Section II, the high-order harmonics in the waveform with such glitches reduce the SFDR [3], [9], [27], [34]. In this paper, we focus on reduction of charge transfer by the coupling capacitance ( $C_c \approx C_{GST3} + C_{GST2}$ ). Similar to CMOS SWCS designs, the widely adopted way to reduce glitch is to use small switch transistors by reducing the charge transfer induced from parasitic capacitance [3], [34]. However, using a smaller transistor requires a higher  $V_{DS}$  for saturation.

In our design, we use the same sizing for the transistors  $T_1$ ,  $T_2$ , and  $T_3$  mentioned above not only to reduce the glitch energy by reducing the charge transfer but also to achieve high output impedance. In addition, as described in Section II-B and Fig. 2(b), HTFETs exhibit the unique behavior ( $C_{GD} > C_{GS}$ ) at a certain  $V_{GS}$  range by the enhanced ON-state Miller capacitance effect [8]. In our design, the biasing  $V_{GS}$  (i.e.,  $\approx 100$  mV) for each transistor to bypass Miller capacitance effect and small transistor size of switching  $T_2$  (or  $T_3$ ), and cascoded  $T_1$  for small  $C_{GS}$  and  $C_{GD}$ , respectively, are utilized to reduce the glitch energy. As shown in Fig. 2(b) and (c), both  $C_{GS}$  and  $C_{GD}$  in HTFETs are smaller than those in Si-CMOS at a low biasing conditions ( $V_{GS} \leq 100$  mV). It results in significant reduction of glitches at node  $V_X$  for HTFET SWCS compared with the Si-CMOS SWCS. In addition, to further reduce glitch energy originated from the simultaneous turning-OFF of the switches, the cross-over switching voltage adjustment is performed.

### B. Digitally Controlled Decoder and High-Speed Latch

As shown in Fig. 1, the rest of circuitry is the binary-to-thermometer decoder and latches. Due to a gigahertz sampling rate (GS/s), the decoder and latches are able to operate in designated frequency range. These high-speed decoder and latches are designed using an in-house HTFET standard cell library [20] to meet the timing requirements with low power consumption. For the decoder, as mentioned in Section III, the total 14 bits are segmented to 6T + 4T + 4B, the same as [3]. The MSB and ULSB are converted to thermometer codes, and LSB remains as binary. Based on the synthesis work, as will be shown in Section V, the HTFET decoder much lower power than Si-CMOS, which is consistent with [13]–[19]. This stems from not only the low-voltage operation (0.3 V in this design) but also the small capacitance in HTFETs. Compared with Si-CMOS DAC designs, HTFETs can keep a small transistor size in the decoder due to the steep-slope characteristics along with the high driving current ability at a low voltage.

Fig. 9 shows a schematic of the high-speed differential latch. This latch employs the differential outputs to directly control switches in the SWCS [3] and to avoid an undesired delay difference such as utilizing an additional inverter to convert

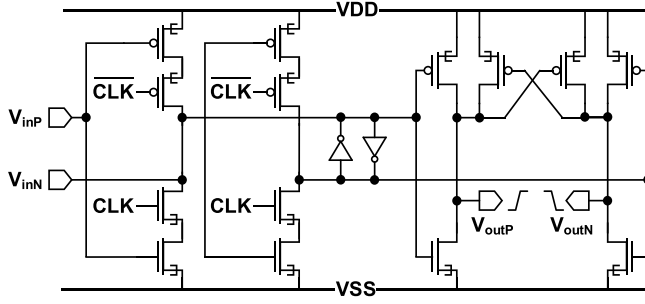


Fig. 9. High-speed differential output latch [3].

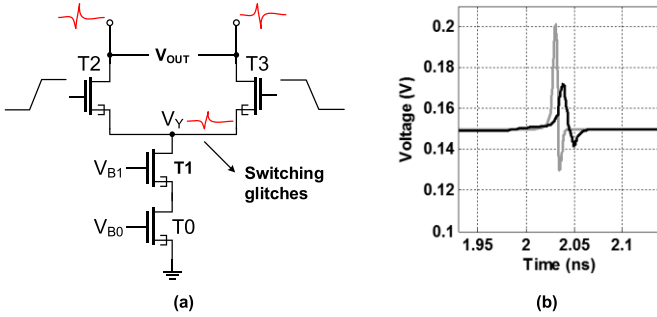
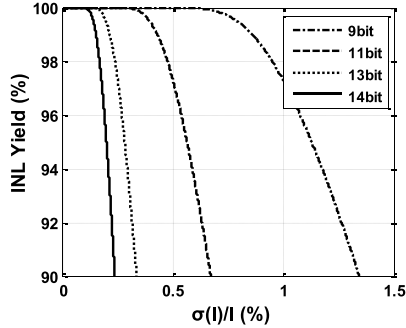


Fig. 10. (a) SWCS with glitches caused by switching. (b) Transient glitch waveform example for HTFET (black line) and Si-CMOS (gray line) SWCS.


 Fig. 11. INL yield with respect to  $\sigma(I)/I$ .

a positive signal to a negative signal. The main role of the latches is to synchronize switching signals from the decoder and to adjust the cross-over point of the switching signals to reduce the undesired glitch energy. In this design, an optimized cross-over point is chosen as 200 mV. Fig. 10 shows the glitches incorporating with the sizing strategies in SWCS and cross-over voltage adjustments of the switch control signals, resulting in smaller amplitude of glitches in the HTFET SWCS compared with the Si-CMOS SWCS.

#### IV. MATCHING PROPERTY IN HTFETs AND CALIBRATION

The static INL is strongly dependent on mismatch error described as a variance of the current source,  $\sigma(I)/I$ , due to the random mismatch [2]. In CMOS designs, the matching accuracy is influenced by the transistor area ( $WL$ ) and biasing conditions in cascoded current sources, so that  $W$ ,  $L_g$ , and  $V_{GS}$  are treated as critical design parameters to obtain high matching accuracy in SWCS designs [6], [10], [24], [25].

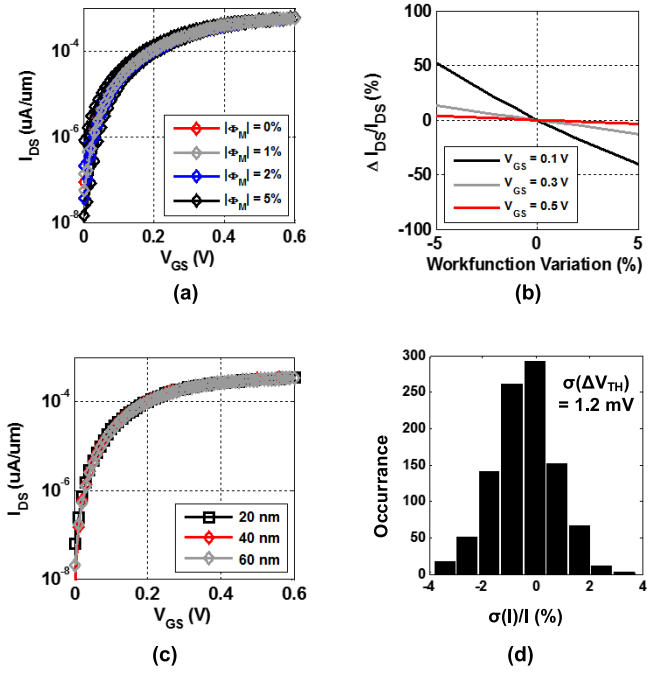


Fig. 12. (a)  $I_{DS}$  variation in terms of WFV ( $\Phi_M$ ) versus  $V_{GS}$  based on TCAD Sentaurus device simulations [35]. (b)  $\Delta I_{DS}/I_{DS}$  (TCAD simulations) versus WFV at various  $V_{GS}$ . (c) Independence of  $I_{DS}$  with respect to  $L_g$  (20, 40, and 60 nm). (d) Monte Carlo Spectre simulations (1000 iterations) in terms of  $\sigma(I)/I$  based on  $\Delta V_{TH}$  in (8). Note that the effective channel length has been fixed to 20 nm.

Fig. 11 shows an achievable yield of the INL as a function of mismatch [2]. For 14-bit high-resolution DACs, for instance,  $\sigma(I)/I$  should be less than 0.25% to meet 90% yield of the INL, indicating that  $44 \mu\text{m}^2$  is required to satisfy 0.25% based on Pelgram's theorem [35] with an assumption of  $A_{V_{TH}} = 1 \text{ mV} \cdot \mu\text{m}$  in our designs [23].

Unlike CMOS designs, it becomes a challenge to alter  $L_g$  for the desired transistor area due to a nature of vertically fabricated device structure and the independence of  $I_{ON}$  with respect to  $L_g$  in HTFETs. Many related works have already investigated the larger threshold voltage mismatch ( $\Delta V_{TH}$ ) shift and less immunization to the WFV ( $\Phi_M$ ) at a low-voltage biasing condition in TFETs [23], [36]. In this section, we explore the matching property of HTFETs in SWCS and digital-background calibration to investigate and to ameliorate the static performance for both Si-CMOS and HTFET DAC designs.

#### A. HTFET Mismatch Modeling Under Device Variations

In TFETs, transistor matching characteristics are yet unclear unlike CMOS. Since the ON-state current ( $I_{ON}$ ) in TFETs has an exponential dependence on the tunneling barrier, any sources of variation can bring a severe  $I_{ON}$  fluctuation [37]. Among various sources of variation, WFV is a leading source of variation [23], [36] in HTFET and Si-CMOS, resulting in  $\Delta V_{TH}$  shifts [23], [36]. Fig. 12(a) shows the sensitivity of  $I_{ON}$  to WFV for HTFET, resorting to results by TCAD Sentaurus [38] and Monte Carlo simulations. The approximately 20% current fluctuation is observed at low  $V_{GS}$  ( $<0.2 \text{ V}$ ) when  $\Delta\Phi_M$  is varied from 0% to 5%.

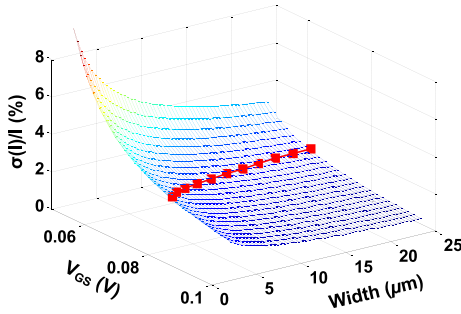


Fig. 13.  $\sigma(I)/I$  versus width and biasing  $V_{GS}$  for HTFETs. Red line: designated current for LSB SWCS.

Fig. 12(b) clearly shows the susceptible behavior to current variance ( $\Delta I/I$ ) in HTFETs with regard to  $V_{GS}$ . It turns out that  $\Delta I_{DS} = 490$  nA/meV at  $V_{GS} = 0.1$  V. This result describes that  $\Delta I$  in HTFET is also influenced by  $V_{GS}$  like CMOS, hence finding optimal  $V_{GS}$  for less current variance is crucial in high-resolution DAC designs.

Fig. 12(c) outlines the ON-state current ( $I_{DS}$ ) in TFET with respect to  $L_g$ . Unlike CMOS, it is clear that  $I_{DS}$  is not inversely proportional to  $L_g$ . However,  $I_{OFF}$  is lowered at a long-channel length (e.g., 40 and 60 nm). In CMOS,  $\Delta V_{TH}$  can be expressed using the Pelgrom theorem [35] as

$$\sigma(\Delta V_{TH}) = \frac{\overbrace{A_{V_{TH}}}^{\text{CMOS}}}{\sqrt{WL}} \rightarrow \frac{\overbrace{A_{V_{TH}}}^{\text{HTFET}}}{\sqrt{2WL_{\text{fixed}}}} = \frac{A_{V_{TH}}}{\sqrt{2W}\sqrt{0.02}} \quad (8)$$

where  $A_{V_{TH}}$  is the mismatch process parameter for the threshold voltage ( $V_{TH}$ ). This mismatch error is mainly determined by transistor area. For TFETs, however, due to the double-gate structure and independence on  $L_g$ , the term,  $(WL)^{1/2}$ , in (8) for CMOS can be amended to  $(2WL_{\text{fixed}})^{1/2}$ .

To evaluate  $\sigma(I)/I$ , the Verilog-A random  $V_{TH} \pm \sigma(\Delta V_{TH})$  model based on TCAD simulations is employed as an input offset voltage over the gate capacitor in  $T_0$  of SWCS with a given biasing voltage. Fig. 12(d) shows  $\sigma(I)/I$  in 1000 iterations of Monte Carlo TCAD simulation results for the unit current source. Fig. 13 shows the dependence of biasing  $V_{GS}$  and transistor width ( $W$ ) in HTFET for current variance. Based on results in Figs. 12 and 13, we obtained the optimized transistor size for the current sources. We make use of 24- $\mu\text{m}$  width for 1.4% of  $\sigma(I)/I$  in the unit current source with  $\Delta\Phi_M = 1\%$  [ $\approx\sigma(\Delta V_{TH}) = 1.2$  mV].

As shown in Fig. 11, an achievable intrinsic resolution with 1.4% of  $\sigma(I)/I$  is 9 bit at a 90% INL yield. Hence, the calibration techniques should be applied to improve static linearity. In this design, the 5-bit digital-background calibration technique is implemented to compensate the static nonlinearity.

### B. 5-Bit Digital-Background Calibration

Since HTFETs have bottlenecks to satisfy required area and output resistance, the conventional small-bit calibration techniques (e.g., digital-background calibration) can help the improvement of static linearity, although it also brings the increase of power and area. The simplified calibration blocks are shown in Fig. 14, utilizing the successive approximation

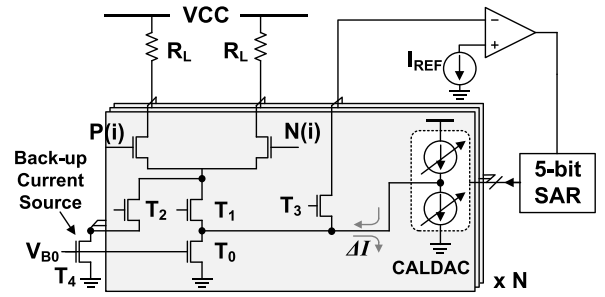


Fig. 14. Simplified 5-bit digital-background calibration scheme.

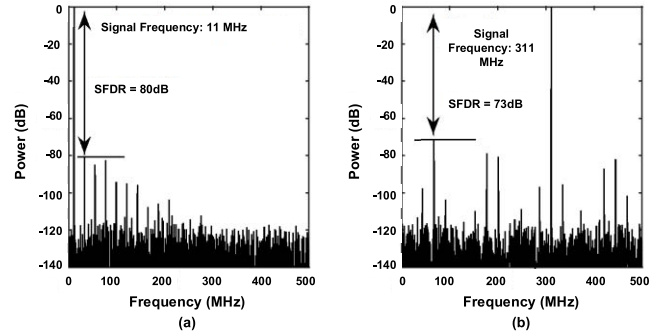


Fig. 15. Spectral performance at (a) signal frequency 11 MHz and (b) signal frequency 311 MHz.

register logic to control CALDAC for the desired current value. The CALDAC allows either sourcing or sinking currents to mitigate mismatch errors at the node of  $V_Y$ , as shown in Fig. 14. For the Si-CMOS DAC design, the digital-background calibration technique is also employed; however, only 3 bits are calibrated, since the intrinsic resolution of Si-CMOS DAC is higher than that of HTFET DAC due to the better matching behavior in Si-CMOS compared with the HTFETs.

## V. SIMULATION RESULTS AND DISCUSSION

The current-steering HTFET DAC has a 0.4 V analog voltage supply and 0.3 V for digitally blocks, whereas the Si-CMOS DAC is designed with 0.4 V supply voltage for both analog and digital blocks for comparisons. Both current-steering DACs have 14 bit with 6T+4T+4B digital-bit segmentations. Their differential load resistance ( $R_L$ ) is 50  $\Omega$  with 6-mA full-scale current ( $I_{fs}$ ). Circuit-level compact Verilog-A models [13] incorporated with the detailed electrical noise models [39] are used for DAC performance simulations at 1-GS/s sampling rate ( $f_s$ ). For the analog core composed of current sources and switch units, extracted parasitics discussed above are incorporated for more accurate performance evaluation. For digital blocks, e.g., the segmentation decoder, parasitics were not included because of the lack of a complete layout standard cell library.

Fig. 15(a) and (b) shows the output spectrums of the HTFET DAC at 11- and 311-MHz signal frequencies ( $f_{\text{sig}}$ ), respectively. It achieves 80-dB SFDR with 11-MHz signal frequency and 73-dB SFDR at 311 MHz. In comparison, the SFDR of the Si-CMOS DAC is 69 and 59 dB at 11 and 311 MHz, respectively. The SFDR in current-steering HTFET DACs is approximately 11~12 dB higher than the Si-CMOS



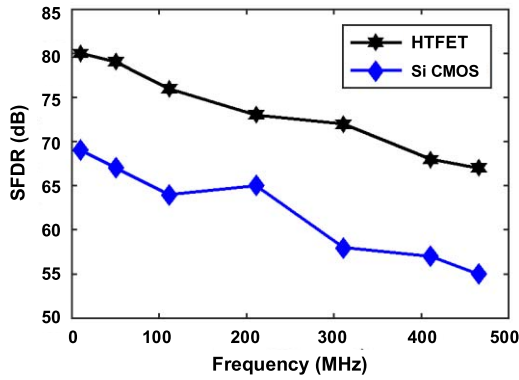


Fig. 16. SFDR versus signal frequency ( $f_{\text{sig}}$ ) comparison between the HTFET and Si-CMOS DACs.

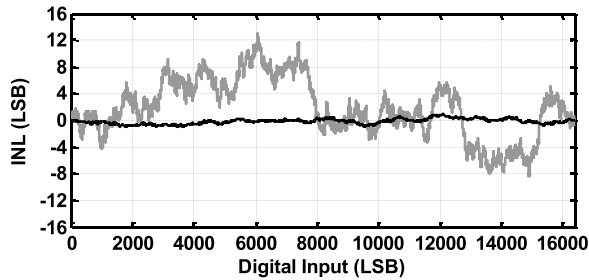


Fig. 17. INL versus digital code transitions. Gray line: without calibration. Black line: with calibration.

DAC due to achievable high  $Z_{\text{OUT}}$ , stemming from ten times of high intrinsic transistor gain ( $g_m \cdot r_o$ ), lower glitch energy, and low capacitance of HTFETs against that of Si-CMOS at a given current and biasing condition, as shown in Fig. 3.

Fig. 16 shows spectral performance with respect to the signal frequency. For the HTFET DAC, the SFDR over the entire Nyquist bandwidth is higher than 70-dB SFDR, while the Si-CMOS DAC achieves less than 60 dB as the frequency reaches Nyquist bandwidth. This DAC design focuses on the intrinsic design optimizations and is potential to gain even better performance with other existing compatible techniques, such as the complementary current source, RZ techniques, dynamic random operations, and so on. As a result, although the SFDR of this HTFET DAC is lower than the state-of-the-art DACs with those techniques, it is higher than the intrinsic performance before applying those techniques.

As described in Section IV-A, calibration is applied in this design for better matching resolution. In the simulations,  $\sigma(I)/I$  of HTFET and Si-CMOS are estimated to be 1.4% and 0.8%, respectively. Fig. 17 shows the static INL performance of the current-steering HTFET DAC. The black plot represents INL according to digital input transitions without calibrations, and the gray plot is for results after utilizing the 5-bit digital-background calibration. With calibration, the INL is improved from  $\pm 17$  to  $\pm 2$  LSB in the worst case, and from  $\pm 13$  to  $\pm 0.7$  LSB in average.

Table I summarizes the performance benchmarking in comparisons with other current-steering DACs [7], [8], including current-steering 20-nm Si-CMOS DACs. The 20-nm HTFET DAC power is 4.6 mW, compared with

TABLE I  
SIMULATED PERFORMANCE BENCHMARKING

Specifications	HTFET	Si CMOS
Process (nm)	20	20
Resolution (bit)	14	14
Sampling rate (GS/s)	1.0	1.0
Supply (V)	0.4/0.3	0.4
Current (mA)	6.0	6.0
Power (mW)	4.6	12.2
Analog (mW)	2.5	2.9
Digital (mW)	0.4	2.1
Calibration (mW)	1.7	7.2
DNL (LSB)	+0.56/-0.49	+0.71/-0.51
INL (LSB)	$\pm 0.7$	$\pm 1.0$
SNDR (dB)	76	62
SFDR <sub>LF</sub> (dB)	80	69
SFDR <sub>fs/2</sub> (dB)	67	55
FOM ( $10^4$ GHz/mW)	328	8.7

12.2 mW for the Si-CMOS design. Although the HTFET DAC needs to calibrate two more bits than FinFET DAC, HTFET DAC consumes much lower power because of power-efficient digital at a low voltage. For evaluating the overall performance of a fast DAC, several types of figure of merit (FOM) were introduced in [3] and [9]. The FOM considering the sampling rate ( $f_s$ ), SFDR at a low signal frequency (SFDR<sub>LF</sub>), SFDR near the Nyquist bandwidth (SFDR<sub>fs/2</sub>), the signal power ( $P_{\text{sig}}$ ), and the DAC power consumption ( $P_{\text{DAC}}$ ) is expressed as

$$\text{FOM} = 2^{\frac{\text{SFDR}_{\text{LF}} - 1.76}{6.02}} \times 2^{\frac{\text{SFDR}_{f_s/2} - 1.76}{6.02}} \times \left( \frac{f_s}{P_{\text{DAC}} - P_{\text{sig}}} \right). \quad (9)$$

A higher FOM in (9) implies higher power efficiency at a given sampling rate [3], [9]. The FOM of this design is significantly higher than other DACs in Table I.

## VI. CONCLUSION

In this paper, the performance advantages and design insights of a 14-bit 1-GS/s low-power high-SFDR current-steering DAC using GaSb-InAs (III-V) heterojunction TFETs have been explored through a codesign framework from devices to the circuit-level implementations: 1) we explored the potential design space with tradeoffs by expanding unique HTFET device characteristics; 2) we evaluated the HTFET DAC in terms of the output impedance, glitch, and matching property compared with the Si-CMOS DAC; and 3) we performed a benchmarking of the SFDR and power in comparison with Si-CMOS DACs. The HTFET DAC exhibits superior SFDR and power performance with higher  $Z_{\text{OUT}}$ , less capacitance, and lower voltage operation than Si-CMOS DAC. This HTFET DAC design offers promise for power reduction and spectral performance improvement in low-power wideband transceiver applications.

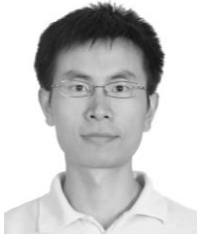
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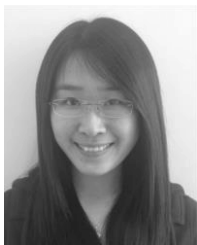


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