

Low-Power High-Speed Current Mode Logic Using Tunnel-FETs

Wei-Yu Tsai, Huichu Liu*, Xueqing Li, and Vijaykrishnan Narayanan

Dept. of Computer Science and Engineering and *Dept. of Electrical Engineering, Pennsylvania State University, USA

Email: wzt114@psu.edu, hxl249@psu.edu, lixueq@cse.psu.edu, and vijay@cse.psu.edu

Abstract—Current mode logic (CML) circuits have been widely used in high-speed data transceivers. The lower-voltage-swing makes the switching speed of CML much higher than the static logic can achieve, so it is worthy to adopt the CML circuits at the cost of higher power consumption in the high-speed applications. In order to obtain a better power efficiency (*Frequency/power*) in CML, it is critical to reduce the power consumption while maintaining the high operating frequency. This paper proposes an alternative approach by building the CML circuits with tunneling-field-effect-transistor (Tunnel FETs or TFETs) to achieve a high-throughput, low-voltage interface circuit design. By taking advantage of its steep subthreshold slope (less than 60 mV/dec), TFET exhibits the same on/off current ratio at the input voltage swing interval much lower than that of the MOSFETs, which enables the supply voltage scaling in CML circuits. For a design target data-rate (20 Gbps for multiplexer and 50 Gbps for buffer), our simulations show that the proposed TFET CML circuits are able to reduce the supply voltage from 0.6 V in conventional Si FinFET CML circuits to as low as 0.3 V while using the same constant tail current. As a result, a power consumption reduction of approximately 50% is achieved by the proposed TFET CML circuits, making the TFET CML approach a promising candidate for future low-power, high-performance applications.

Index Terms—CML, high-frequency, low-power, low-voltage, TFET.

I. INTRODUCTION

WITH the development of the emerging mobile systems, the communication speed, and correspondingly, the bandwidth of communication interface circuits between electronics devices, has been increasing rapidly. Meanwhile, lowering the power consumption for higher power efficiency has also become a key issue for those devices to extend the battery life and support the system operation with comparatively weaker power sources such as the RF power [1]–[4]. As a result, developing devices and circuits to design such low-power high-speed communication interfaces are intriguing for future applications.

On the other hand, the low-power high-speed circuit interface design is a challenging task. Static logic has been considered as a general approach for functional logic gates dealing with the bit-wise parallel data. However, the limited bandwidth of static logic circuits is not adequate for novel high-speed serial link interfaces. The high-speed transmitters with Current mode logic (CML) using BiCMOS and highelectron-mobility transistor (HEMT) technologies have been reported (SiGe [5], [6] and InP HEMT [7], [8] at speed of 50 Gbps and above).

CML circuits with a smaller output swing have been adopted for a faster switching speed at the expense of relatively higher constant power consumption at low data rates.

For those CML circuits, the power consumption is determined by the constant-current and the supply voltage, which is independent of the operation frequency. Therefore, the CML is more competent in the high-speed applications than the static logic. As the power-reduction of the CML circuits cannot be achieved by decreasing the frequency, some works have focused on reducing the gate counts [9], [10] as an architecture-level low-power approach for CML. However, the single-gate power consumptions of these works are still high because those CML gates have to operate with a high supply voltage. The challenge of the supply voltage reduction in CML logic comes from reduced voltage difference between logic-1 and logic-0, given the fact that the voltage level switch in CML logic is not full-swing (from VDD to GND). Hence, an aggressive scaling of the supply voltage will cause an increasing failure rate in the circuit operation, which becomes the main obstacle for power reduction of the CML logic.

In this work, we propose a low-voltage approach to reduce the power consumption of CML by using the steep slope tunneling field effect transistors (Tunnel FETs or TFETs). Benefited from its *sub* – 60 mV/dec subthreshold swing, TFET has shown its prominent energy efficiency advantages for ultra-low power applications, especially at reduced supply voltage of 0.3 V and below. Many works have explored TFET-based applications, such as static logic [11], D-FF [12], and SRAM [13]. TFET based analog/RF applications have recently been explored by taking advantage of its unique device characteristics such as the high transconductance to current ratio (g_m / I_{DS}), uni-directional operation, low voltage operation, etc. [14]–[16], where the TFET-based CML hasn't been explored so far. By taking the advantages of its desired low voltage operation characteristics, we highlight the performance benefits of the TFET CML circuits under extremely low biasing voltages to extend the application spaces of the CML logic. The design aspects and operation analysis of TFET CML circuits are presented compared with the baseline Si FinFET CML circuits. The low-voltage CML design is beneficial to explore the high-speed communication functions of some advanced low-power technologies, such as low supply voltage bio-electronic devices [17], or environmental power harvesting devices [2]–[4].

In the rest of this paper, Section II introduces the charac-

teristics of CML and TFET, respectively. Section III describes how the TFET characteristics benefit the CML operation as the supply voltage is reduced. Section IV presents the simulation results of the TFET CML compared with the baseline Si FinFET designs, followed by the conclusion in Section V.

II. CURRENT MODE LOGIC AND TUNNEL FET

A. Current Mode Logic Characteristics

The major difference between the CML circuits and the static logic circuits is that the CML has a voltage swing smaller than the static logic, and thereby it has a shorter switching time. The schematics of CML buffer and multiplexer (MUX) are shown in Fig. 1, respectively. A CML logic circuit is constructed by a constant current tail, several pairs of transistors, and a pair of resistors. In a CML buffer, there is only one pair of transistors, controlled by the differential inputs. The resistors and NMOS's are used to charge and discharge the output node pair, *OUTPUT*. The logic of *OUTPUT* is the inverse of that of *INPUT*, which controls the on/off state of the transistor pair. The voltage level is equal to the supply voltage (V_{SUPPLY}) when *OUTPUT* is logic-1, but it's not the ground-level when logic-0. The total constant current (I_C) passes through one of the resistors, making the voltage on the output node on that resistor drops to voltage of logic-0 (V_0):

$$V_1 - V_0 = R \times I_C. \quad (1)$$

It is noted that the CML circuits consume approximately constant amount of power ($V_{SUPPLY} \times I_C$), and the consumption is almost independent to the switching frequency of input logic.

V_{SUPPLY} of a CML buffer is distributed onto the three components the current pass through, which are one of the resistors, one of the transistor pair, and the current tail. Specifically, the current tail is usually implemented by a single transistor operating in the saturation region, so the current path would be considered as one resistor and two transistors. Similarly, the current in a CML MUX is selected by the lower transistor pair (*Pair-3*), and then be selected again by one of the upper pairs (*Pair-1* or *Pair-2*). Hence the V_{SUPPLY} of a CML MUX is distributed onto four components, which are one resistor and three transistors.

The bias conditions of the transistors' drain-to-source (V_{DS}) and gate-to-source (V_{GS}) voltages are the key aspects in CML circuit design. The V_{GS} and the V_{DS} are strictly related to the V_{SUPPLY} because of the voltage distribution as discussed above. In low-power design domain, there are several limitations for the operation of transistors while V_{SUPPLY} is reduced. First of all, the CMOS transistors can operate properly when V_{GS} , which is related to the output voltage swing of the previous stage, is above the threshold voltage (V_{TH}). If the V_{SUPPLY} of a CML circuit becomes too low for the voltage difference ($V_1 - V_0$) to be distinguishable, the succeeding stage circuits might have an indistinct input logic, resulting in a small on/off current ratio. Secondly, reducing the V_{SUPPLY} might also lower the V_{DS} of the current tail.

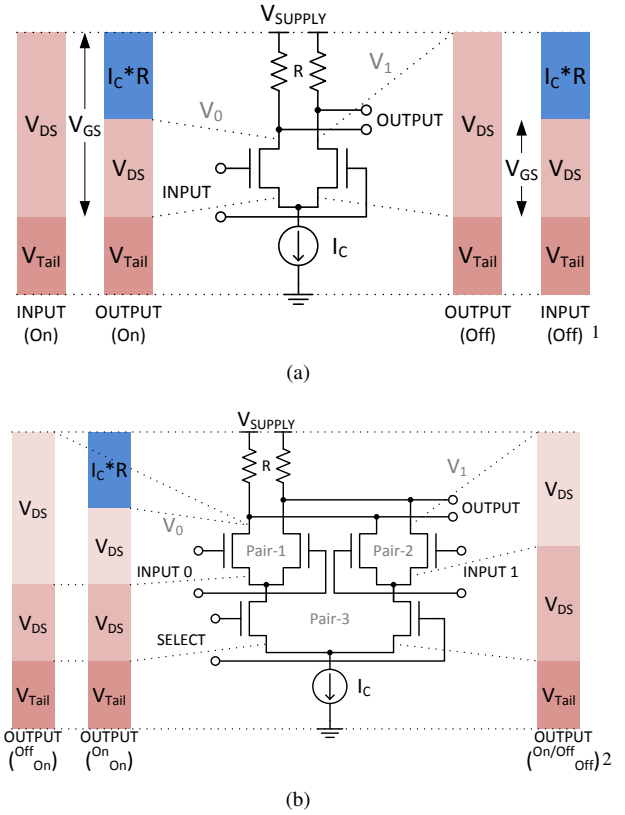


Fig. 1. Schematics and voltage distributions of current mode logic (CML) (a) buffer and (b) multiplexer (MUX) circuits.

Because the current tail should be operated in the saturation region in order to maintain a constant current insensitive to the glitch of V_{DS} , the aggressive reduction of V_{SUPPLY} is detrimental to the CML operation. Moreover, the lower the V_{SUPPLY} is, the lower V_{GS} and V_{DS} the CMOS transistors are operating with, and the more possibly the logic would fail or slow down. Given this reason, the subthreshold or near-threshold CMOS designs are not suitable in low-power CML circuits.

Therefore, it is challenging to reduce the power consumption in CMOS CML circuits using the V_{SUPPLY} scaling technique.

B. Tunnel FET Modeling and Device Characteristics

TFET has emerged as a promising alternative device technology for various low power applications, benefiting for its sub-60 *mV/decade* subthreshold slope (SS) [18]. III-V material-based heterojunction TFET (HTFET) has further improved tunneling current with the hetero-band alignment, exhibiting a comparable on-state current with the subthreshold MOSFET [19] with significant energy efficiency advantage.

As discussed in the Section II-A, to overcome the limitation of decreasing V_{SUPPLY} of the CML circuits, a transistor operates at a low supply voltage with high performance is critical. Hence, we employ the GaSb-InAs HTFET in CML

¹(*State*) is the state of the transistor, which might be turned on or off.

²(U_{Upper} U_{Lower}) are the states of the upper and lower transistors.

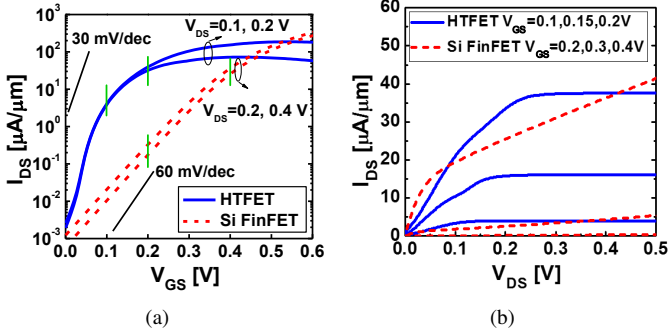


Fig. 2. The current characteristics of different operating region for Si FinFET and HTFET: I_{DS} vs. (a) V_{GS} and (b) V_{DS} .

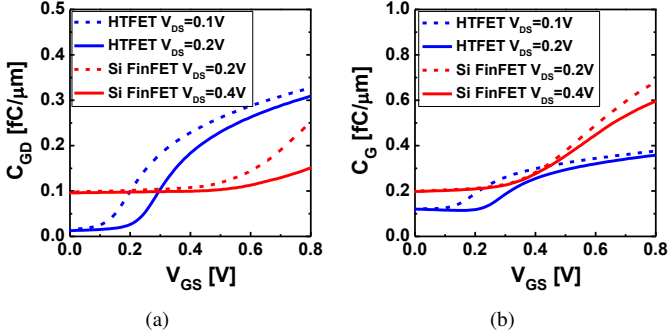


Fig. 3. The capacitance characteristics of different operating regions for Si FinFET and HTFET: (a) C_{GD} and (b) C_G .

circuits, which is known as one of the most promising device architectures to realize TFETs, to enable the further scaling the V_{SUPPLY} . In this paper, we employ the 20 nm III-V HTFET Verilog-A model [20] developed from the TCAD Sentaurus device simulation [21] and calibrated by full-band accurate atomistic simulations [22], which has already been applied in previous works [15], [23], [24]

A 20 nm Si FinFET Verilog-A model [20] is used as our baseline design for performance comparison.

Fig. 2(a) shows the I_{DS} vs. V_{GS} and I_{DS} vs. V_{DS} characteristics of the modeled HTFET compared to 20 nm Si FinFET. The interband tunneling induced carrier injection mechanism leads to a sub-60 mV/decade SS in TFET. An average sub-threshold slope of 30 mV/decade can be achieved in HTFET at supply voltage $V_{DS} = 0.1$ V and 0.2 V, where its I_{DS} outperforms that of the Si FinFET at $V_{DS} = 0.2$ V and 0.4 V below 0.5 V V_{GS} . Besides the low voltage operation, one of the most beneficial characteristic of HTFET for CML circuits is the improved saturation characteristics compared to Si FinFET, as shown in Fig. 2(b). Such characteristic has been recently observed in measured TFET output characteristics in reported literature [25]. In circuit simulation, we carefully design the V_{DS} bias of the current tail transistor to ensure the operation of TFET in saturation region to avoid the variation of V_{DS} during switching.

III. PROPOSED CML CIRCUITS IN HTFET

Given the fact that HTFET can operate with lower V_{GS} and V_{DS} , in this section, we focus on the CML circuit design

using HTFETs to achieve low-power, high-speed operation. To analyze the performances of CML circuits in CMOS (Si FinFET is chosen as a comparable technology) and in HTFET, the buffer and the MUX circuits in this section are constructed with the same structures as shown in Fig. 1.

A. Voltage Analysis for CML Buffer

When the V_{SUPPLY} is lowered, the logic voltage swing ($V_1 - V_0$) would also be reduced because of the lowered voltage distributions on each component of CML circuits. Fig. 1(a) shows the ideal cases of voltage distributions of CML buffer in stable status. The difference of input V_{GS} , i.e. $V_1 - V_0$, must be large enough so that the on- and off-current are distinguishable to each other. In Fig. 2(a), the slope and corresponding current of TFET at $V_{GS} = 0.15$ V are similar to those of Si FinFET at $V_{GS} = 0.3$ V, so 0.15 V is considered as the V_{TH} of TFET and is a proper bias voltage as the cross point (midpoint of logic-1 and logic-0). In other words, the current sensitivity to V_{GS} is preserved when the HTFET is adopted in a bias V_{GS} interval with an input swing 0.1 ~ 0.2 V, compared to the Si FinFET with 0.2 ~ 0.4 V. Therefore, the V_{GS} in on-state can be lowered to a half and the on-current is kept the same. As a result, the proposed HTFET CML buffer can operate correctly even when the V_{SUPPLY} and voltage swing are reduced to one half of those in FinFET.

Another design constraint of CML circuits is that the bottom transistor, which is used as the constant current tail, should provide a stable current that is insensitive to the variation of V_{DS} . In the conventional CML circuit design, the current tail FinFET transistor is biased at the saturation region so that the current is less sensitive to V_{DS} . As shown in Fig. 2(b), the Si FinFET shows a higher $g_{DS} = \Delta I_{DS} / \Delta V_{DS}$ in the saturation region due to the short channel effect. HTFETs, on the other hand, exhibits a much lower g_{DS} when the V_{DS} increases to the saturation region compared to Si FinFETs as discussed in Section II-B. Accordingly, the current tail in the proposed HTFET model can provide a more stable current that is insensitive to the variation of V_{DS} . In addition, the stable tail current and the differential signalling make the output of the CML circuits insensitive to peripheral noise.

B. Speed Analysis for CML Buffer

In CML circuits, the maximum operation frequency is determined by the charging and discharging time of the load capacitance. Figure 3 shows the capacitance characteristics of Si FinFETs and HTFETs. The total parasitic capacitance on the output node (C_{LOAD}) is the sum of gate-to-drain capacitance (C_{GD}) and gate capacitance (C_G) times the fanout number N . The HTFET has a smaller or equivalent C_{GD} and C_G in the bias region (0.1 V ~ 0.2 V) compared to the Si FinFETs in the respective region (0.2 V ~ 0.4 V). Moreover, because we use the similar I_C for both Si FinFET and proposed HTFET based designs, the proposed HTFET CML circuit has a smaller charging time constant which is

proportional to the voltage swing,

$$\begin{aligned} T_{charge} &= R \times C_{LOAD} \\ &= R \times (C_{GD} + N \times C_G). \end{aligned} \quad (2)$$

The discharging operation is through a different path, hence the resistance of the transistors should be considered. Since the bias condition V_{DS} varies with time, we use the equivalent R_T for the transistor resistance in the discharging time estimation,

$$\begin{aligned} T_{discharge} &= R_T // R \times C_{LOAD} \\ &= (V_{DS}/I_{DS}) // R \times (C_{GD} + N \times C_G). \end{aligned} \quad (3)$$

Ideally, the source voltage (V_S) of the switching transistor pair is assumed to be steady because only one of them is turned on due to the differential input. The drain-to-source current I_{DS} of the switching transistor pair varies with time. For simplicity, the current is assumed as the average I_{DS} , which is comparable for both Si FinFET and HTFET based designs. As mentioned in Section III-A, the TFET in the proposed CML conducts the similar current at a much lower biasing voltage than the FinFET in the conventional CML. Accordingly, the proposed HTFET CML buffer can save power by reducing V_{SUPPLY} , and it does not slow down the switching speed compared to the Si FinFET CML buffer.

C. The CML Multiplexer

Compared to the CML buffer, the voltage distributions in the CML MUX on every element are smaller, which imposes further challenges at reduced V_{SUPPLY} . Figure 1(b) shows that the additional voltage distribution on transistor *Pair* – 3 in the CML MUX. Compared to the CML buffer, at the same voltage swing, the V_{GS} of *Pair* – 1 or *Pair* – 2 transistors in Fig. 1(b) would be smaller due to the increased voltage level of source-nodes of these transistors. Therefore, at the same V_{SUPPLY} , the voltage bias constraint of the CML MUX is more restrictive than that of the CML buffer, especially when V_{SUPPLY} is reduced.

As shown in Fig. 2(a), the subthreshold slope of the HTFET is steeper than that of the Si FinFET when $V_{GS} < 0.1 V$. If the bias V_{GS} intervals are shifted left (because of the decreased voltage distributions in CML MUX) for both proposed HTFET and Si FinFET designs, the current I_{DS} for discharging of TFET might decrease slightly more than the current of FinFET. Consequently, the equivalent R_T of a proposed HTFET CML MUX might be increased more than that of a Si FinFET CML MUX. Fortunately, the ratio of V_{DS} to I_{DS} determines the time constant based on Eq. 3, where the proposed CML MUX has the smaller V_{DS} . If the voltage-current ratio for the proposed MUX is kept the same to that for the conventional MUX, then the operation speed would be similar for both designs.

For the Si FinFET CML MUX, the V_{GS} must be larger than V_{TH} (about 0.3 V in this paper). According to Fig. 1(b), there are two more voltage distributions for the *Pair* – 3 transistors and the current tail in addition to the V_{GS} , so the CML circuits are hard to operate with $V_{SUPPLY} < 0.6 V$. On

the contrary, the HTFET has an equivalent V_{TH} (assuming the equivalent V_{TH} of the HTFET is at $I_{DS} = 10 \mu A/\mu m$) about 0.15 V, so the proposed CML circuits in HTFET is possible to operate with a half V_{SUPPLY} (0.3 V). If the V_{SUPPLY} of the proposed HTFET CML MUX is further lowered, the I_C would drop much faster than that of the conventional Si FinFET design, therefore the time constants (the charging and discharging time) of proposed HTFET CML MUX would be increased significantly. As a result, the lowest V_{SUPPLY} for the proposed HTFET CML circuits is 0.3 V.

In summary, the desired device operation of HTFET at low bias voltages (V_{GS} and V_{DS}) is beneficial to lower the V_{SUPPLY} of high-speed CML circuits. The similar current of HTFET at a much smaller V_{GS} is important when the output swing is decreased. With a properly biased voltage, the time constants of proposed HTFET CML circuits during the discharging is less than or equal to those of the conventional Si FinFET CML circuits, so the decreased V_{SUPPLY} would not slow down the operating speed. As a result, the proposed CML circuits in HTFET are capable to operate at the same speed with a V_{SUPPLY} about 0.3 V.

IV. SIMULATION RESULTS

In this section, we present the simulation results of the proposed HTFET CML buffer and CML MUX compared to the Si FinFET designs, respectively. HTFET CML circuits can operate with a much lower V_{SUPPLY} at a similar high frequency compared to the conventional CMOS-based (Si FinFET in this paper) CML circuits.

To achieve the equivalent operating frequency, the conventional Si FinFET and proposed HTFET CML circuits with their lowest possible voltage (0.6 V and 0.3 V) are designed to have the similar I_C . However, the slope of I_C to V_{GS} is large in the both technologies, so it's difficult to have exactly the same I_C for the conventional and proposed models. Figure 4 shows the output eye diagrams of the conventional Si FinFET and the proposed HTFET CML circuits. As mentioned in Section III-C, the discharging time of HTFET and Si FinFET CML MUX may be similar when having an equivalent ratio of V_{DS} to I_{DS} . In the simulations, the output voltage swing ($V_1 - V_0$) of the CML circuit is kept the same ratio to the V_{SUPPLY} in each simulation, i.e. $(V_1 - V_0) = \alpha \times V_{SUPPLY}$, $\alpha = 0.4 \sim 0.5$. The comparisons of Si FinFET and proposed HTFET CML gates are shown in Table I. The comparisons of operating voltage and frequency for this work and related works are shown in Fig. 5. In [5]–[8], peaking inductors are used to enhance the bandwidth in addition to adopting the high-electron-mobility technologies. In this work, the inductorless design with reduced voltage swing can also achieve the high speed, but with an extremely low voltage.

The power consumptions in different operating frequency of CML buffer and MUX for both Si FinFET and proposed HTFET designs are shown in Fig. 6. Although the power consumption is the summary of static power and dynamic power, the static power dominates the total power in CML

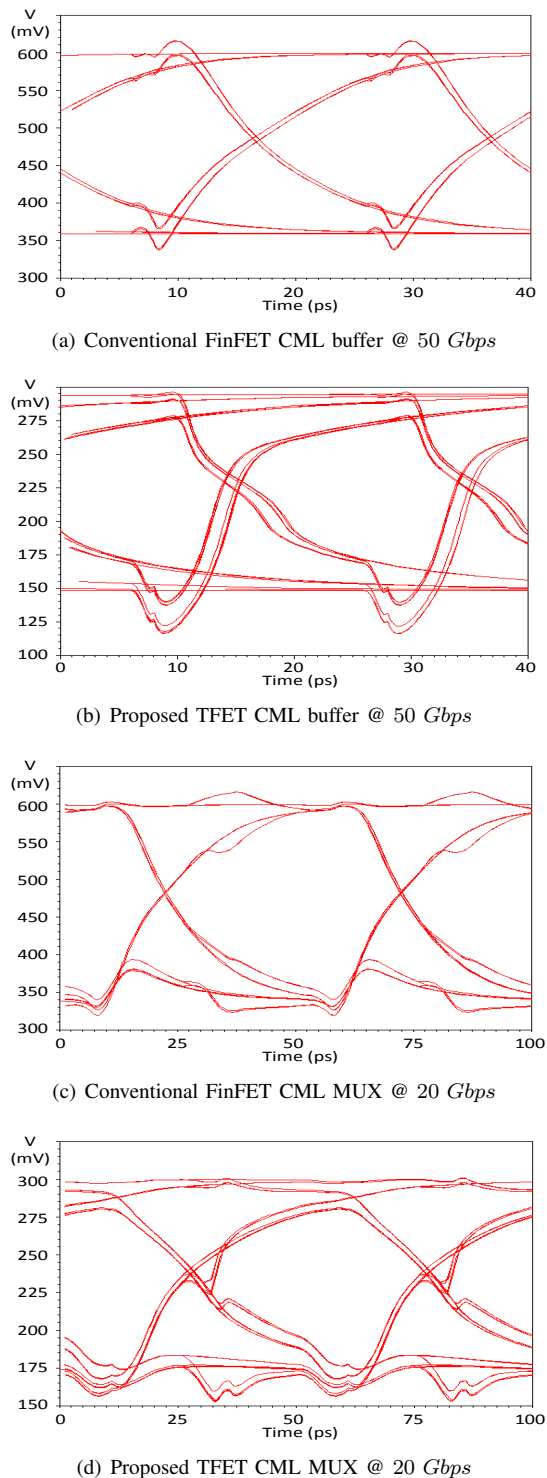


Fig. 4. The output eye diagrams of buffer and MUX for conventional FinFET model vs. proposed TFET model.

circuits. The dynamic power for charging and discharging tend to cancel the majority of each other and become small because the CML circuit structure is symmetric and the *INPUT* and *OUTPUT* logic is differential. The proposed HTFET CML circuits operate under $V_{SUPPLY} = 0.3 V$, whereas the conventional Si FinFET CML circuits operate

TABLE I
COMPARISON OF CONVENTIONAL AND PROPOSED CML BUFFER AND MUX GATES

	Conventional CML in FinFET		Proposed CML in TFET	
	buffer	MUX	buffer	MUX
Frequency	50 Gbps	20 Gbps	50 Gbps	20 Gbps
V_{SUPPLY}	0.6 V	0.6 V	0.3 V	0.3 V
Power per gate	306 nW	213 nW	159 nW	103 nW

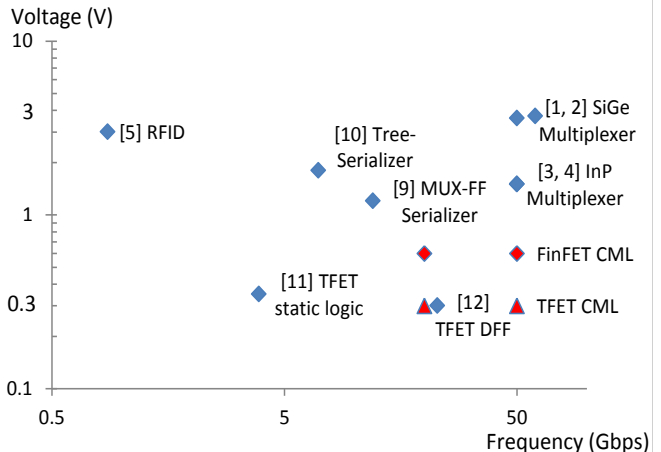


Fig. 5. The comparison of this work and related works in operating voltage and frequency.

under $V_{SUPPLY} = 0.6 V$. Therefore, the power consumption of proposed HTFET CML buffer is as low as about 1/2 to that of the conventional Si FinFET design when they are working at their highest frequency, which is 50 Gbps in this simulation. Similarly, the power consumption ratio of the proposed HTFET to the conventional Si FinFET MUX is also about 1/2 while working at 20 Gbps as shown in Fig. 6(b). In summary, the proposed HTFET CML buffer and MUX save 48% and 52% power consumption in the simulations, respectively.

The experimental verification is currently not available due to the infancy of the TFET process. Ongoing efforts are being carried out to improve the fabrication process for future experimental demonstrations of the TFET integrated chips.

V. CONCLUSION

In this paper, the high-speed CML circuits using heterojunction TFET are proposed to reduce power consumption. The proposed HTFET CML buffer and MUX circuits employ the conventional CMOS CML circuit designs with optimizations of the bias conditions for performance improvement. Because the HTFET have a much lower effective threshold voltage (about 0.15 V) and also a steep subthreshold slope, the proposed CML circuits are able to operate under a much lower supply voltage compared to the baseline Si FinFET design (with threshold voltage about 0.3 V). According to the voltage and speed analyses in Section III, the proposed HTFET CML circuits have a charging/discharging time constant less than or equal to that of the conventional Si FinFET designs with the proper design of the bias voltages, and therefore can operate

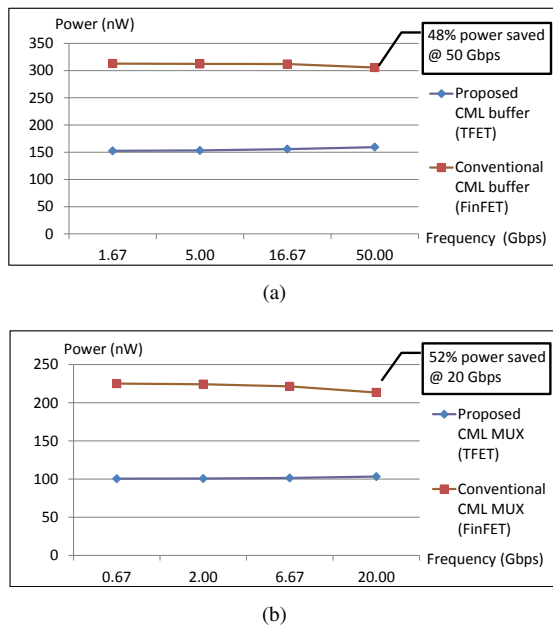


Fig. 6. The Power consumption under different frequency for conventional FinFET and proposed TFET CML (a) buffer and (b) MUX circuits.

with much lower power consumption without degrading the speed. The simulation results in Section IV have shown that the proposed HTFET CML circuits can operate with a supply voltage as low as 0.3 V at the same frequencies compared to the conventional Si FinFET CML circuits (50 Gbps for the buffer and 20 Gbps for the MUX). Meanwhile, the power consumption reduction is about 50% (because the supply voltage is reduced by half) when the HTFET is adopted in the CML buffer and the MUX. The sequential CML circuits (latches or flip-flops), which have more design constraints in clock timing, are part of the prospective future works.

ACKNOWLEDGEMENTS

This work was supported in part by the LEAST, one of the six SRC STARnet Centers, sponsored by MARCO and DARPA. The NSF award 1317560 supported equipment is used in this effort.

REFERENCE

- [1] D. De Donno, L. Catarinucci, and L. Tarricone, "A battery-assisted sensor-enhanced RFID tag enabling heterogeneous wireless sensor networks," *Sensors Journal, IEEE*, vol. 14, no. 4, pp. 1048–1055, April 2014.
- [2] S. Gollakota, M. Reynolds, J. Smith, and D. Wetherall, "The emergence of RF-powered computing," *Computer*, vol. 47, no. 1, pp. 32–39, Jan 2014.
- [3] H. Visser and R. Vullers, "RF energy harvesting and transport for wireless sensor network applications: Principles and requirements," *Proceedings of the IEEE*, vol. 101, no. 6, pp. 1410–1423, June 2013.
- [4] C. Alippi and C. Galperti, "An adaptive system for optimal solar energy harvesting in wireless sensor network nodes," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 55, no. 6, pp. 1742–1750, July 2008.
- [5] M. Meghelli, A. Rylyakov, and L. Shan, "50-Gb/s SiGe BiCMOS 4:1 multiplexer and 1:4 demultiplexer for serial communication systems," *Solid-State Circuits, IEEE Journal of*, vol. 37, no. 12, pp. 1790–1794, Dec 2002.
- [6] Y. Luo, G. Chen, and K. Zhou, "60Gb/s low jitter 4:1 mux and 1:4 demux," in *Circuits and Systems, 2008. MWSCAS 2008. 51st Midwest Symposium on*, Aug 2008, pp. 590–593.
- [7] T. Suzuki, T. Takahashi, K. Makiyama, K. Sawada, Y. Nakasha, T. Hirose, and M. Takikawa, "Under 0.5W 50Gb/s full-rate 4:1 MUX and 1:4 DEMUX in 0.13 μm InP HEMT technology," in *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, Feb 2004, pp. 234–252 Vol.1.
- [8] T. Suzuki, Y. Kawano, Y. Nakasha, S. Yamaura, T. Takahashi, K. Makiyama, and T. Hirose, "A 50-Gbit/s 450-mW full-rate 4:1 multiplexer with multiphase clock architecture in 0.13 μm InP HEMT technology," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 3, pp. 637–646, March 2007.
- [9] H. Lu, C. Su, and C.-N. Liu, "A tree-topology multiplexer for multiphase clock system," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 56, no. 1, pp. 124–131, Jan 2009.
- [10] W.-Y. Tsai, C.-T. Chiu, J.-M. Wu, S. Hsu, and Y.-S. Hsu, "A novel low gate-count pipeline topology with multiplexer-flip-flops for serial link," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 59, no. 11, pp. 2600–2610, Nov 2012.
- [11] U. Avci, R. Rios, K. Kuhn, and I. Young, "Comparison of performance, switching energy and process variations for the TFET and MOSFET in logic," in *VLSI Technology (VLSIT), 2011 Symposium on*, June 2011, pp. 124–125.
- [12] M. Cotter, H. Liu, S. Datta, and V. Narayanan, "Evaluation of Tunnel FET-based flip-flop designs for low power, high performance applications," in *Quality Electronic Design (ISQED), 2013 14th International Symposium on*, March 2013, pp. 430–437.
- [13] R. Pandey, V. Saripalli, J. Kulkarni, V. Narayanan, and S. Datta, "Impact of single trap random telegraph noise on Heterojunction TFET SRAM stability," *Electron Device Letters, IEEE*, vol. 35, no. 3, pp. 393–395, March 2014.
- [14] A. Trivedi, S. Carlo, and S. Mukhopadhyay, "Exploring tunnel-FET for ultra low power analog applications: A case study on operational transconductance amplifier," in *Design Automation Conference (DAC), 2013 50th ACM / EDAC / IEEE*, 2013, pp. 1–6.
- [15] H. Liu, R. Vaddi, S. Datta, and V. Narayanan, "Tunnel FET-based ultra-low power, high-sensitivity UHF RFID rectifier," in *Low Power Electronics and Design (ISLPED), 2013 IEEE International Symposium on*, 2013, pp. 157–162.
- [16] X. Li, H. Liu, K. Ma, U. Heo, S. Datta, and V. Narayanan, "RF-powered systems using steep-slope devices," accepted by *12th IEEE International New Circuits and Systems Conference (NEWCAS14)*, June 2014.
- [17] Y. Sundarasaradula and A. Thanachayanont, "A 0.7-V, 2.86- μW low-noise logarithmic amplifier for neural recording system," in *TENCON 2013 - 2013 IEEE Region 10 Conference (31194)*, Oct 2013, pp. 1–4.
- [18] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS Logic," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2095–2110, 2010.
- [19] D. Nikonov and I. Young, "Uniform methodology for benchmarking beyond-CMOS logic devices," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, pp. 25.4.1–25.4.4.
- [20] V. Saripalli, G. Sun, A. Mishra, Y. Xie, S. Datta, and V. Narayanan, "Exploiting heterogeneity for energy efficiency in chip multiprocessors," *Emerging and Selected Topics in Circuits and Systems, IEEE Journal on*, vol. 1, no. 2, pp. 109–119, 2011.
- [21] Synopsys, *TCAD Sentaurus Device Manual*, 2010.
- [22] U. Avci, S. Hasan, D. Nikonov, R. Rios, K. Kuhn, and I. Young, "Understanding the feasibility of scaled III-V TFET for logic by bridging atomistic simulations and experimental results," in *VLSI Technology (VLSIT), 2012 Symposium on*, June 2012, pp. 183–184.
- [23] H. Liu, M. Shoaran, X. Li, S. Datta, and V. Narayanan, "Tunnel FET-based ultra-low power, low-noise amplifier design for bio-signal acquisition," in *Low Power Electronics and Design (ISLPED), 2014 IEEE International Symposium on*, 2014.
- [24] X. Li, H. Liu, U. D. Heo, K. Ma, S. Datta, and V. Narayanan, "RF-powered systems using steep-slope devices," in *IEEE International New Circuits and Systems Conference (NEWCAS 2014)*, 2014.
- [25] R. Rooyackers, A. Vandooren, A. Verhulst, A. Walke, K. Devriendt, S. Locorotondo, M. Demand, G. Bryce, R. Loo, A. Hikavy, T. Vandeweyer, C. Huyghebaert, N. Collaert, and A. Thean, "A new complementary hetero-junction vertical Tunnel-FET integration scheme," in *Electron Devices Meeting (IEDM), 2013 IEEE International*, Dec 2013, pp. 4.2.1–4.2.4.