Enabling Internet-of-Things: Opportunities Brought by Emerging Devices, Circuits, and Architectures

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***Abstract*—The Internet-of-Things (IoT) has excited low-power design from device, circuits, to architectures levels. This paper talks about how recent emerging beyond-CMOS devices, such as tunnel field effect transistor (TFET), negative capacitance FET (NCFET), and phase transition devices (PTD), could extend the low-power design space to enable IoT applications with beyond-CMOS features.**

Keywords—Internet-of-things; emerging devices; tunnel FET; negative capacitance FET; energy harvesting; nonvolatile memory; nonvolatile processor; neural network

I. INTRODUCTION

Living in an era where human and the world are becoming more and more closely connected through intellegent devices, human life has significantly improved through sensing, signal processing, and communication with so-called Internet-of-things (IoT) [1]. Meanwhile, the foundation of solid-state devices, and the circuits and systems built upon them, are the key core that enables the functionality of IoT signal processing and connectivity.

With the common need for portability, many IoT devices are powered by batteries or energy harvesters [2]. In the past few decades, the scaling of CMOS technology together with signal processing techniques has lowered the power consumption significantly, which makes the recent efforts in IoT applications feasible with a decent battery capacity or ambient energy density. However, such conventional CMOS transistor technology, as well as the computation and communication methods built on it, are facing a situation that further power reduction becomes more and more challenging. This is essentially because further voltage scaling in CMOS to reduce the dynamic computation power while providing sufficient speed conflicts with the exponentially increasing leakage power. This fundamentally limits the growing of functionality and scenarios where IoT devices are powered by batteries or harvested energy.

Another IoT implementation challenge is how to tackle with the low and intermittent harvested power from the environment when operating in the battery-less mode [3]. While low input power limits the average amount of task being performed, the intermittency causes more severe problems of losing computation progress that is not backed up.

Fortunately, the advent of emerging technologies, including emerging transistor devices, circuits, and architectures, provides the opportunity of further power scaling. On the one hand, there are new transistors that behave as a boolean switch that could be directly used in conventional computing approaches where most existing algorithms need no significnat change [4]. One the other hand, with new features of some new devices, non-boolean logic or non-Von Neumann architecture is more suitable [5][6].

In this paper, we focus on three types of emerging devices, including tunnel field effect transistor (TFET) [7], negative capacitance FET (NCFET) [8], and phase transition devices (PTD) [9]. They are all promising beyond-CMOS candidates that could work with a lower voltage for futher power reduction in boolean computation. They also exhibit substantially new features that could be captured for new attractive functionalities.

In the rest of this paper, we will first talk about the bottlenecks of existing IoT implementation efforts in Section II. Then the three abovementioned emerging devices will be introduced, with focus on their electrical characteristics in Section III. Section IV describes how these device characteristics could enable new opportunities in IoT applications while mitigating existing bottlenecks. Section V continues to discuss future work and related work. Finally Section VI summarizes this paper.

II. IOT SYSTEMS AND THEIR BOTTLENECKS

In this section, we present a general IoT system diagram and describe the function of each block in it. A few examples will be given. Then we will analyze the bottlenecks in each block considering existing efforts towards optimizations.

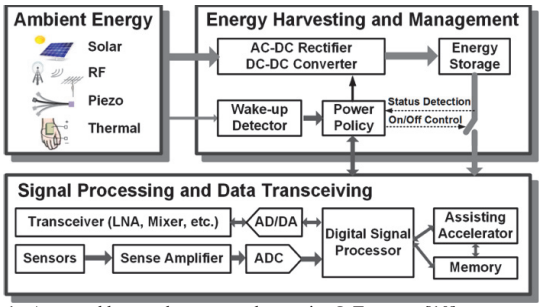

Fig. 1. A general battery-less energy-harvesting IoT system [10].

A. General IoT System Diagram and Examples

Fig. 1 illustrates a general battery-less IoT system powered by energy harvesting techniques [2][10]. It consists of the power supply and management module, sensors and interface, memory storage, and a digital signal processor and accelerators. Fig. 1 only shows the battery-less system diagram. Based on the application requirement, one or more blocks in Fig. 1 may not be necessary. For example, the wake-up detector and accelerator might be removed if there is no need for waking-up or acceleration. More details of each block will be discussed in the next sub-section (Section II. B).

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There have been quite a few IoT system examples powered by harvested radio-frequency (RF) energy [2], including the highway RFID pass, glucose level sensor on a contact lens, and some bio-signal sensors on animals or insects. Based on how much energy is obtainable with restrictions on the package weight and size, their system functionality varies from a simple signal recorder to complex in situ signal processor, such as one with EEG signal processing, and wireless transmission.

B. Bottlenecks and Existing Efforts

Energy sources and energy harvesting techniques. Typical ambient energy sources include solar energy, RF radiation, piezoelectric effect and thermal gradients [2][3]. In order to obtain a DC supply from an RF signal antenna and piezoelectric films, a rectifier is required to converter AC signals to DC output. DC-DC converters are also widely used when a higher or lower DC voltage is needed. While the ambient energy sources differ in their energy density, generation mechanism, voltage range, AC/DC features, and dependence on the environment, they do have features relatively in common: generally low and varying energy density, intermittency, dependency of the efficiency on the load condition, and unpredictability. While circuit optimizations including tracking and adaptive operations, e.g. maximum power point tracking [11], could be applied to mitigate these effects, there still exists two other concerns. On the one hand, harvesting weak power from the environment usually lands up with low power-converion efficiency (PCE) because conventional commercial CMOS technology has high resitive energy loss in low-voltage operation [12][13]. On the other hand, saved energy in capacitors is also leaking and will be wasted if not used in time.

Sensing, interface, and communication. The development of sensors has been notable in the past decade, showing significant reduction in both size and power. However, the amount of data being transferred between the IoT devices, the analog world, and human (or other reader devices) has increased significantly, especially in audio, image, and videos. In this scenario, the request for lower power digital-analog conversion, signal amplification, wired and wireless data transceivers, has never been so urgent before. Some techniques, such as passive sensing and communication (e.g. backscatter in [17]) become useful to reduce the power, but still face the limitation of the types of sensed signals, or the operation range and speed.

Digital signal processing. As introduced in Section I, the slowing down of voltage scaling fundamentally restricts the power reduction. Frequency power failures cause many backup-restore operations, limiting the forward computing progress. While there are some initial results and conclusions on these topics, study of signal processing algorithms, computing architectures for IoT systems is still insufficient [14][15][16].

Data storage. Memory element is needed before the processing and transmission are carried out. While the amount of required data storage depends on the application, higher density, lower voltage and lower power are preferred. As many IoT devices benefit from a smaller size, the system integration compatibility of memory is also important. More importantly, recent research has revealed the advantage of integrated nonvolatile memory (NVM) into the chip so reduce access energy and delay [14][15][16][18][19]. For some applications where memory access becomes the bottleneck, the co-design of data storage and signal processing architecture is useful [20].

Other issues. Besides aforementioned bottlenecks, there are other concerns such as security [21], privacy, etc., which are not the main focus of this paper.

III. Emerging Beyong-CMOS Devices

This section introduces three emerging beyond-CMOS devices, i.e. TFET, NCFET, and PTD. The devices will be compared with conventional CMOS. While introducing these devices, there are a few terms that we use frequently:

ON-state current (I_{ON}): drain current when the transistor is on, usually with gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}) equal to the supply voltage. A higher I_{ON} indicates less turn-on resistance, and is preferred for higher speed.

OFF-state current (I_{OFF}): drain current when the transistor is off, usually with V_{GS} equal to zero and V_{DS} equal to the supply voltage. A lower I_{OFF} indicates lower leakage current.

Subthreshold swing (SS): the amount of required voltage change applied to the gate of a device so as to change the drain current by a decade in the subthreshold region. For conventional CMOS technology, the thermionic emission of carrriers limit its SS to be higher than 60mV/dec at the room temperature. With a smaller SS, a lower-voltage supply suffices the same I_{ON}/I_{OFF} ratio and reduces the sum of dynamic and leakage power. A smaller SS also lead to higher $g_m I_D$ that indicates higher current efficiency for analog and RF circuits, because

$$\frac{g_m}{I_D} = \frac{\partial I_D}{\partial V_{GS}} \frac{1}{I_D} = \frac{\partial \ln I_D}{\partial V_{GS}} = \frac{\ln 10}{SS}. \quad (1)$$

Steep-slope devices: devices with SS less than 60mV/dec of conventional CMOS transistors at the room temperature.

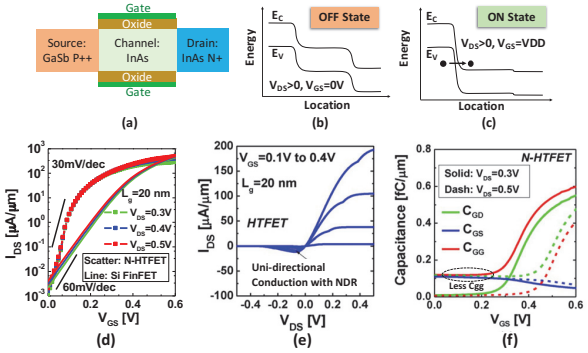

Fig. 2. HTFET. (a) Structure of an N-type HTFET; (b-c) OFF and ON state energy diagrams; (d, e) I_{DS}-V_{GS} comparisons; (f) Capacitance [2][12][13][22].

A. TFET

TFET is essentially a gated reverse-biased p-i-n diode with asymmetric doping [7]. Among various types of TFET devices, a double gate GaSb-InAs heterojunction TFET (HTFET) device structure that shows good balance between steep slope and high I_{ON} is shown in Fig. 2(a) [12]. At a low gate bias voltage, the device current is small because the energy barrier is wide enough to suppress the band-to-band tunneling (BTBT) probability, as illustrated in Fig. 2(b). As the gate voltage increases, the tunneling barrier is narrowed and the quantum-mechanical

TABLE I. RECENT ADVANCES IN TFET, NCFET, AND PTD-BASED HYPERFET

	NCFET		TFET			HyperFET	
Source	[30] EDL'16	[31] EDL'16	[52] IEDM'14	[51] EDL'15	[50] VLSI'15	[9] Nature comm'15	[40] VLSI'16
Structure	P(VDF-TrFE)	BiFeO3, FinFET	Si FinFET	III-V vertical	III-V vertical	External connection	Monolithic
I_{ON} (μA/μm)	100	1e-4-1e-6	-	8.4	275 N; 30 P	20% gain	35% gain
I_{OFF}	~5pA/μm	1e-12-1e-14	I_{ON}/3e4 N; I_{ON}/2e6 P;	0.1nA/μm	0.8nA/μm N; 0.3nA/μm P	~1μA/μm	4nA/μm
SS_{min} (mV/dec)	45-52 (2-4 w/ hysteresis)	8.5-11 P; 16-50 N	56 N; 58 P;	64 N	55 N; 115 P;	<15 forward; <30 reverse	8 forward; <20 reverse
With Hysterisis	no	yes	no	no	no	yes	yes

BTBT phenomenon shown in Fig. 2(c) provides an abrupt transition between the ON and OFF states, achieving below 60mV/decade SS at the room temperature shown in Fig. 2(d).

Besides the steep-slope switching, HTFET also exhibits other new features shown in Fig. 2(e-f) [2][12][13][22]. Originating from the asymmetric structure, the uni-directional tunneling makes TFET conducting current almost in one-way only fashion in a moderate voltage range. Negative differential resistance also appears within moderate negative V_{DS} range. HTFET also has lower and higher capacitance than Si FinFET in low and high voltage regions, respectively. Some recent TFET experiments are summarized in Table I. TFET device modeling is already available for circuit designs [12][13][23]-[26].

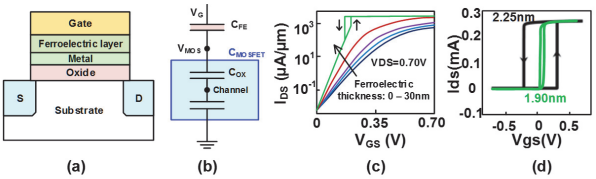

Fig. 3. NCFET. (a) Device structure; (b) Capacitance model; (c-d) Simulated switching behavior versus ferroelectric layer thickness [8][19][35][35][37].

B. NCFET

In 2008, it was predicted that, negative differential capacitance, could be stacked into the gate insulator of MOSFET, so that a small voltage at the gate could create a larger change in the surface potential, leading to a steeper switching behavior in the transistor [27]. Fig. 3(a-b) shows the device structure and the gate capacitance in concept. The performance of an NCFET depends on the matching of the magnitude of the ferroelectric negative capacitance and the channel capacitance. And the capacitance tuning is the key to the NCFET process [8].

Fig. 3(c-d) shows the dependence of switching slope and hysteresis on the ferroelectric layer thickness [19][37]. As the thickness increases, SS reduces, and the hysteresis finally appears and opens up, with the hysteresis window covering from only part of the positive V_{GS} range to both positive and negative V_{GS} range. It is noted that the abovementioned capacitance matching affects the hysteresis, and the simulated results in Fig. 3(c) and (d) are based on two different NCFET devices.

Such characteristics of steep slope, hysteresis, and their tuning methods, have been the main focus of device optimization and circuit design start points [19][35][36]. In the past years, there have been both fundamental and experimental results [28]-[34]. Due to the challenge of integrating the ferroelectric layer, some devices are built with an external ferroelectric capacitor. Some recent NCFET results are summarized in Table I.

C. Phase Transition Devices and HyperFET

Steep-slope phase transition devices (PTD) are making use of the abrupt phase change according to the voltage or current applied to a certain type of material called correlated material [38]. With the aid of the correlated material characteristics shown in Fig. 4(a), the operation mechanism of PTD could be understood. A correlated material is a two-terminal symmetric structure that could operate in either metallic state with low resistivity, or insulator state with much higher resistivity. A typical correlated material is vanadium dioxide (VO2), which has significant resistivity difference between the two states up to a few orders [9][40]. At a very low voltage, the correlated material is in the insulator state. Such an insulator state will stay unit the voltage applied to the material reaches the insulator-to-metallic transition (IMT) voltage V_{IMT}, where the abrupt resistivity reduction occurs and the correlated material enters the metallic state. The metallic state will not go back to the insulator state unless the voltage applied to the material drops below the metallic-to-insulator transition voltage V_{MIT}, which is lower than V_{IMT}. By proper material design, the resistivity in the two states, and the state transition voltage could be tuned.

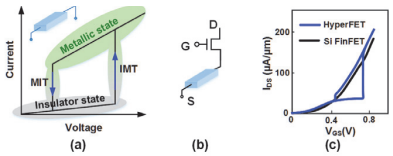

Fig. 4. VO2 and HyperFET. (a) VO2 and its insulator-metallic hysteresis; (b) HyperFET device structure; (c) I_{DS}-V_{GS} comparison [9].

A HyperFET could be built by connecting the source of a MOSFET to the correlated material, as shown in Fig. 4(b). The correlated material could also be deposited directly on top of the source contact [9]. When V_{GS} is low, the correlated material in the insulator state suppresses the drain current to reach low leakage. When V_{GS} is high, the correlated material enters the metallic state, the resistance of which has small impact on the drain current. Through proper threshold tuning, HyperFET could have the same I_{OFF} as conventional MOSFET, while achieving higher I_{ON}. The orders of resistivity difference between the two states provides sharp switching slope in HyperFET, leading to <60mV/dec SS. Recent experimental results achieve 8mV/dec SS [40], as shown in Table I. HyperFET provides two potential applications, one with higher I_{ON} and the same I_{OFF}, the other with the transition between two states in the hysteresis window.

IV. NEW OPPORTUNITIES ENABLED BY EMERGING DEVICES

This section re-visits the bottlenecks discussed in Section II, and see how they could be mitigated by these emerging devices.

A. *Energy Harvesters and Sensors with Higher Efficiency*

Increasing the amount of harvested energy in the same environment directly increases the number of performable tasks and functionalities in an energy-harvesting IoT system. Because of the steep switching characteristics, these emerging devices well suit the low-voltage operations. Fig. 5 shows typical voltage conversion circuitry, with rectifier in (a), and conventional DC-DC charge pump topology in (b), and enhanced DC-DC charge pump topology with TFET in (c) [12][13]. Fig. 6 shows power conversion efficiency (PCE) comparisons between Si FinFET and III-V heterojunction TFET (HTFET).

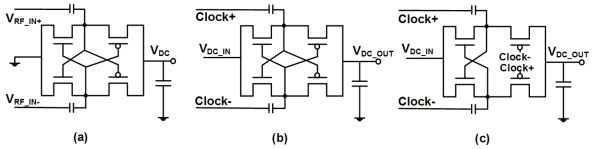

Fig. 5. rectifier and DC-DC charge pumps. (a) Rectifier; (b) Conventional DC-DC charge pump; (c) Enhanced DC-DC charge pump in III-V HTFET [12][13].

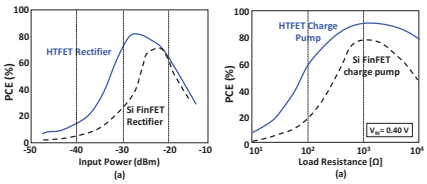

Fig. 6. PCE of rectifier in (a) and DC-DC charge pump in (b) [12][13].

It is observed that the designs in HTFET have a higher PCE, especially when the resistive power loss becomes more significant, i.e. the low input voltage range. This is partially achieved by a better trade-off between the resistive power loss and switching capacitive loss. The uni-directional tunneling conduction feature also contributes to a higher PCE because of less reverse power loss by the leakage current from the output to the input. For the enhance HTFET DC-DC converter, the change of the output p-type transistor gate control to the input clock signal enables doubled gate driving and less resistive power loss. Such significantly extend the IoT operating scenarios.

From another aspect, an energy harvester itself is a sensor that senses the amplitude of the input power level. A higher PCE also also improves the sensing sensitivity in some applications, such as ultraviolet (UV) sensor, motion or vibration sensor, and radio sensor, etc. For NCFET and HyperFET based designs, although there has been no reported result for rectifiers or DC-DC charge pumps, a higher PCE will not be a surprise.

B. *Analog Processing and Communication*

For analog processing and wired or wireless communication, the desired low power depends on the trade-off between speed (or bandwidth), gain, linearity or spectral performance (such as input-referred noise, signal-to-noise+distortion ratio or SNDR, spurious-free dynamic range or SFDR), etc. Considering the widely used front-end and back-end circuits shown in Fig. 1, including A/D converters, D/A converters, sense amplifiers, and RF blocks, Fig. 7 shows some evaluation results using TFET.

Fig. 7(a) shows a 6-bit 10MS/s successive-approximate-register (SAR) A/D converter, and Fig. 7(b) shows how HTFET could lower the energy beyond the limit of CMOS [25]. Such gain is achieved because of higher current efficiency for both digital SAR logic and comparator (higher g_m/I_D). Fig. 7(c-d) shows the performance comparison of a low noise bio-signal telescopic amplifier (LNA) [23]. Here HTFET also outperforms Si FinFET in gain because of higher g_m/I_D. This feature also reduces the input referred noise as it is the output noise divided by the gain. Fig. 7(d-e) shows the performance comparison of a current-steering D/A converter [26]. HTFET shows higher SFDR with less capacitance at low voltage region, which leads to higher output impedance and less coupled switching glitches.

In [41], RF circuit designs in TFET were review, including mixer, RF LNA, oscillators, frequency doubler, etc. HTFET shows substantial benefits in low-voltage high-frequency circuits, with high nonlinearity for mixers, and high transconductance and gain at low current and low power levels.

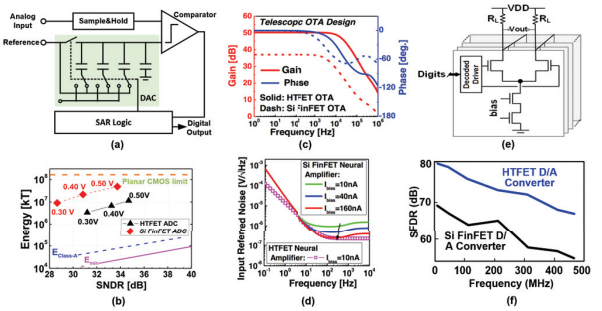

Fig. 7. Comparisons between HTFET and Si FinFET designs. (a-b) SAR A/D converter and performance; (c-d) OTA gain and input referred noise versus frequency; (e-f) Current-steering D/A converter and its SFDR [23][25][26].

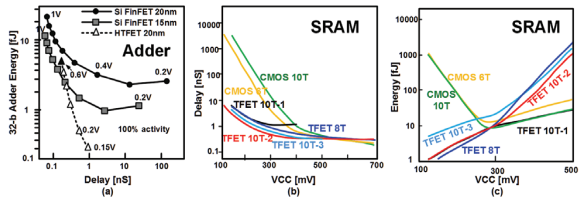

Fig. 8. TFET design examples. (a) 32-b Adder; (b-c) SRAM [43][44].

C. *Digital Logic and Nonvolatile Memory*

Existing research work on combinational gates and adders, sequential gates like D flip-flops, SRAM, has shown that TFET outperforms conventional CMOS in energy-delay with a low supply voltage, as shown by a few examples in Fig. 8 [43][44]. While using TFET for pass-transistor logic, the impact of uni-directional tunneling conduction should be mitigated by either adding another pass transistor for the other direction conduction, or changing the circuit scheme. A newly work considering both layout parasitics also shows that, even with a higher contact resistance due to the need to connect the vertical structure, similar performance advantage is still observed [45]. For a processor design, with less energy per instruction, TFET extends the design space considering thermal limit and the number of parallelism, leading to higher performance [46].

NCFET in logic has lower energy-delay for low-voltage scenarios with moderate-to-high capacitive wire load, as shown in Fig. 9(a) [36]. The hysteresis within positive V_{GS} region as shown in Fig. 5(c) significantly improve the input noise margin by the width of the hysteresis window [35]. To understand this,

consider an NCFET inverter, both p- and n-type transistors will not turn on until the input increases beyond the rising hysteresis edge, nor will they turn off until the input signal reduced beyond the falling hysteresis edge, as illustrated in Fig. 9(c). The use of HyperFET in digital logic works similarly.

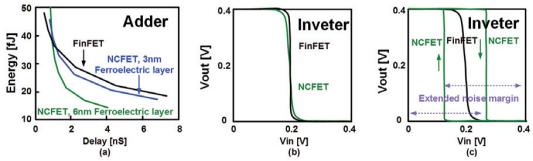

Fig. 9. NCFET evaluation [35][36]. (a) Energy-delay for a Koggy-Stone adder; (b) Input-output transfer function (NCFET has 16nm ferroelectric layer thickness); (c) Input-output transfer function (NCFET has 27nm ferroelectric layer thickness) showing improved input noise margin with NCFET hysteresis.

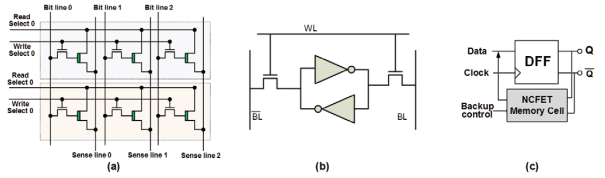

Fig. 10. NCFET circuits [19][35]. (a) 2-transistor nonvolatile memory array; (b) NCFET SRAM with enhanced noise margin; (c) Nonvolatile NCFET D flip-flop.

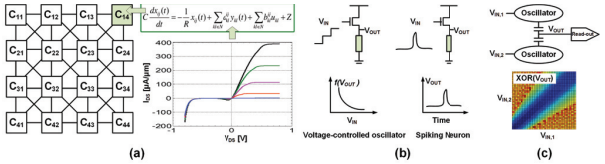

Fig. 11. NN and coupled oscillators. (a) TFET based CNN; (b) HyperFET based oscillator and spiking neuron; (d) Coupled oscillators [39][42][48][49].

D. Nonvolatile Data Storage and Nonvolatile Processing

Nonvolatile memory (NVM) is intriguing for IoT energy-harvesting applications, in its non-volatility that is immune to power failure and removal of refreshing. With on-chip NVM and associate sensing and control, a nonvolatile processor (NVP) could be built to backup processor states and data into this NVM before power failures, and restore them after the power recovery [47][55][63]-[65]. Such on-chip data backup and restore have less power, energy and interface overhead than conventional nonvolatile check-pointing solutions with out-of-chip NVM, and thus improves the computational progress in scenarios with an intermittent power supply [14]. Fig. 10(a) shows an NCFET NVM design with hysteresis around V_{GS}=0V shown in Fig. 3(d) [19]. It is reported that this NCFET NVM improves the trade-off between density and access energy, which is crucial for IoT applications, leading to more computational forward progress for an NVP. The improved input noise margin of NCFET logic could also be used to build SRAM cells with enhance noise margin, as shown in Fig. 10(b) [35]. NCFET could also be used to build nonvolatile D flip-flops (DFF)by attaching the NCFET bit storage to a conventional DFF, as illustrated in Fig. 10(c) [35].

E. Neural Network (NN) and coupled Oscillator Accelerators

When operating as Boolean logic devices for accelerators, TFETs, NCFETs, HyperFETs could provide higher efficiency than conventional CMOS, especially in low-voltage scenarios. One intriguing scenario is using them for power reduction in non-von Neumann architectures, such as cellular neural network (CNN), and spiking neural networks for machine learning in applications including object recognition, classification, etc.

In Fig. 11(a), the nonlinearity between input gate voltage and output drain voltage in TFET is used, which removes the output transfer function in conventional CNN design, and lowers the complexity and power of CNN [42]. The NCFET could also serve as the weight storage in a cross-bar based synapse array for neural networks. The non-volatility ensures low power consumption. The gating control of NCFET provides more flexibility and isolation than RRAM based synapse array.

HyperFET is also promising in implementing analog spiking neural network [48][49]. The abrupt and significant resistance change between the metallic and insulator states could be exploited to trigger a spike when the input exceeds a certain threshold, as what is in a real neuron axon. Fig. 11(b) shows that a HyperFET could work as either an oscillator or a spiking neuron depending on its input: a slow change input, or a spiking input [39][48][49]. Such oscillators could be coupled, as shown in Fig. 11(c). It has been reported that, the output of the coupled oscillator settles as a nonlinear function of the input pair in voltage. Such a transfer function could be exploited to efficiently compute some nonlinear computations, such as nonlinear norms, in a way of power-efficient "let physics do the computation".

V. Future Work for IoT with Emerging Devices

There is still a large gap towards system implementation and application mapping. This section briefly discusses future IoT work with emerging devices.

Device understanding, optimization, integration, and characterization: Continuous optimization of material and process is required for large-scale integration. Abstracting and modeling features devices are also a key, especially for features that may not be scalable, reliable, or controllable.

Circuit and architecture techniques: It is unlikely for emerging device features to be used as a drop-in replacement for all conventional CMOS techniques. Circuit and architecture optimizations to make the most use of pros and mitigate cons of emerging devices are necessary [14]-[16][53][58]. Meanwhile, device features deviating from conventional CMOS behavior may actually be very useful in some applications, highlighting the necessity of device-circuit-application co-design.

Higher-level considerations: Quality-of-service (QoS) and task schudeling optimization, with support from software design [54][56]-[62]. Security, privacy, and communication protocals would be of rising concern. All of them need more work from device to architecture.

VI. Conclusion

This paper has discussed the bottlenecks in efforts towards Internet-of-things, and emerging devices, circuits and architectures that could bring enhanced and new features to the implementations. The future work for IoT is also discussed.

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