# A Comprehensive Model for Ferroelectric FET Capturing the Key Behaviors: Scalability, Variation, Stochasticity, and Accumulation 

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Abstract: In this work, we developed a comprehensive model for ferroelectric FET (FeFET), which can capture all the essential ferroelectric behaviors. Unlike previous models, which can describe only a subset but not all the reported ferroelectric behaviors, the proposed model can: i) predict device performance with geometry scaling; ii) quantify the device-to-device variation with device scaling; iii) exhibit stochasticity during a single domain switching; and iv) capture the accumulation of domain switching probability with applied pulse trains. This comprehensive model would enable researchers to explore a wide range of FeFET applications and guide device development, optimization and benchmarking.
Introduction: The accelerated research activities in ferroelectric $\mathrm{HfO}_{2}$ based FeFET need a unified model to predict its major physical behaviors such as scalability, variation, stochasticity and accumulation of domain switching probability (Fig.1). However, previously reported models can only capture a subset of ferroelectric behaviors, limiting the exploration of FeFET applications. For example, the multidomain Preisach model [1] and the Landau-Devonshire model [2] fail to capture the transition from continuous to discrete switching with device scaling (scalability) [3], the exacerbated device-to-device variation with geometry scaling (variation) [4], and the stochasticity of single domain switching (stochasticity) [3-4]. Additionally, both previous models, along with the kinetic Monte Carlo (kMC) model [4], cannot predict the accumulation of switching probability under pulse trains (Accumulation) [3]. These phenomena have enabled design of FeFET based random number generators [5], neurons [6] and synapses for neuromorphic computing and in-memory computing, etc. As such, a comprehensive model is desirable.
Model Structure: The model is based on a reported Monte Carlo framework [7], where the ferroelectric film is composed of multiple independent domains. Instead of executing the simulation event-by-event (domain switching) in the kMC model [4], the proposed model progresses in time, where the domain switching probability at each time step is calculated (Fig.2). The nucleation-limited switching model is adopted to describe switching in poly-crystalline $\mathrm{HfO}_{2}$ [1]. This model introduces a parameter $h=\int_{t_{o}}^{t} t^{\prime} / \tau_{i}\left(E_{a, i}, E\left(t^{\prime}\right)\right) d t^{\prime}$, where $\tau_{i}$ is switching time constant for domain $i$, and depends on its activation field $E_{a, i}$ and the applied field $E\left(t^{\prime}\right)$. This parameter keeps track of all the ferroelectric history and thus is capable of capturing the accumulation behavior. This model is then solved self-consistently with the transistor charge-voltage equations to obtain FeFET characteristics (Fig.2).
Scalability, Variation, Stochasticity, and Accumulation in FeFET: The model is first calibrated with measured metal-ferroelectric-metal (MFM) charge-voltage ( $Q_{\mathrm{FE}}-V_{\mathrm{FE}}$ ) hysteresis loops (Fig.3a) and switching dynamics (Fig.3b). Non-saturated hysteresis loops caused by small applied field are successfully captured by the model. The switching dynamics are also accurately reproduced with the model. Especially, it predicts that the device variation becomes significant with the geometry scaling ( 2000 domains to 40 domains) due to domain switching stochasticity. The dynamics of a single domain switching can
be probed in FeFET, where ultra-scaled device can be measured. With a large number of domains, the FeFET model can reproduce the measured memory window of the 28 nm FeFET technology (Fig.4a). This calibrated model predicts the degradation of the array memory window due to increased inter-device variation with scaling (Fig.4c). This phenomenon has also been observed in experiment (Fig.4b). It is ascribed to the randomness caused by domain switching stochasticity, reduced number of domains, and domain inhomogeneity [4].

The discreteness of single domain switching starts to emerge with device scaling. Fig.5a shows that threshold voltage ( $V_{\mathrm{TH}}$ ) shift exhibits an abrupt jump above a certain write pulse amplitude. This abrupt switching is stochastic in nature, whose switching probability follows a sigmoid dependence on the amplitude (Fig.5c). Since the proposed model is based on a distributed Monte Carlo framework, it can nicely handle the geometry scaling and predict the stochastic switching in scaled devices (Fig. 5b, d). Another ferroelectric behavior is the accumulation of polarization under identical pulse trains. No models exist to date can capture this behavior. In the case of FeFET, the polarization accumulation causes $V_{\text {TH }}$ shift and hence drain current change, which has been utilized to demonstrate synaptic weight cell in large FeFETs. In scaled devices, it exhibits an abrupt $V_{\mathrm{TH}}$ jump above a pulse number threshold (Fig.6a). This abrupt switching is also stochastic (Fig.6b) and the required pulse number for switching depends exponentially on the pulse amplitude (Fig.6c). The proposed model can qualitatively capture all the described accumulation behaviors (Fig.6d, e, f). This is achieved by tracking the $h$ parameter (Fig.6g, h), which keeps increasing until the domain flips. The growth in $h$ causes the accumulation of switching probability, and eventually the $V_{\text {TH }}$ shift in FeFET.
Model Applications: With all the essential ferroelectric behaviors captured, various applications can be explored. Without loss of generality, two examples are presented here. One is the true random number generator (TRNG) by harnessing the entropy of the switching process in scaled FeFET (Fig.7a-c). To generate a single bit, a FeFET is reset first and then a write pulse inducing $50 \%$ switching probability is applied, which causes negligible bias in the generated bits. The other example is the analysis of AND type FeFET memory array (Fig.7d-f). Various write pulses are applied to the array and the resulting statistics collected indicate the necessary write conditions (shmoo plot) for successful array operation.
Conclusion: We have developed a comprehensive model for FeFET and demonstrated its applications in memory array optimization and TRNG. Unlike previous models having limited applicability, the proposed model can capture key characteristics of FeFET, including the scalability, variation, stochasticity, and accumulation. Therefore, this model could be valuable for device optimizations and application explorations.
References: [1] K. Ni et al., VLSI 2018; [2] A. Aziz et al., EDL 2016; [3] H. Mulaosmanovic et al., Appl. Mater. Interfaces 2018; [4] K. Ni et al., VLSI 2019; [5] H. Mulaosmanovic et al., EDL 2017; 2018; [6] S. Dutta et al., VLSI 2019; [7] C. Alessandri et al., TED 2019;

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Fig.1. A model for FeFET need to capture its key physical behaviors, which include scalability, variation, stochasticity, and accumulation.


Fig.3. Calibration of the model with measured (a) $Q_{\mathrm{FE}}-V_{\mathrm{FE}} \quad$ Fig.4. (a) Calibration of the FeFET model with Fig.5. (a)/(b) FeFET model captures minor loops; (b) polarization switching dynamics. Device memory window; (b)/(c) measured and simulated measured abrupt switching in scaled variation from 200 capacitors become worse with the device variation for large and scaled devices. The device. (c)/(d) the model can predict decrease of domain number (from 2000 to 40). model predicts degraded variation with scaling. the stochasticity of domain switching.


Fig.6. (a)/(b)/(c) and (d)/(e)/(f) show that the model can capture the accumulation of switching probability with pulse trains. The model can qualitatively show the exponential dependence on the pulse amplitude of required pulse number to switch a domain. (g)/(h) Waveform shows accumulation of switching probability with pulses, causing domain flip.
i. Random number generator using scaled FeFET


Fig.7. Model applications for (i) random number generator (RNG) and (ii) memory array analysis. i-(a) shows the waveform to extract random bits out of stochastic switching process and the random bits (b) and (c) are almost bias free. ii-(d-e) are the model application for AND array analysis. The shmoo plot indicates the necessary write conditions for array operation. (f) shows the $\mathrm{I}_{\mathrm{D}}$ distribution at different write conditions.


