A High-Efficiency Switched-Capacitance HTFET Charge Pump For Low-Input-Voltage Applications

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***Abstract*—This paper presents a high-efficiency switched-capacitance charge pump in 20 nm III-V heterojunction tunnel field-effect transistor (HTFET) technology for low-input-voltage applications. The steep-slope and low-threshold HTFET device characteristics are utilized to extend the input voltage range to below 0.20 V. Meanwhile, the uni-directional current conduction is utilized to reduce the reverse energy loss and to simplify the non-overlapping phase controlling. Furthermore, with uni-directional current conduction, an improved cross-coupled charge pump topology is proposed for higher voltage output and PCE. Simulation results show that the proposed HTFET charge pump with a 1.0 kΩ resistive load achieves 90.4% and 91.4% power conversion efficiency, and 0.37 V and 0.57 V DC output voltage, when the input voltage is 0.20 V and 0.30 V, respectively.**

Keywords—DC-DC converter; power-conversion-efficiency (PCE); Charge pump; switched-capacitance; tunnel FET (TFET)

I. INTRODUCTION

With the development of Internet of Things (IOT), power efficiency has been a primary issue in portable and wearable system design to support a long operation time [1-4]. To obtain a sufficiently high voltage supply from low-voltage energy sources such as thermoelectric cells and solar cells in a dark office, DC-DC step-up charge pumps are required to boost the voltage. For these charge pumps, the power conversion efficiency (PCE) is one key performance specification because it determines the total power budget [5]-[16].

The challenge is how to obtain a high PCE with a low input voltage. Considering a temperature gradient of 3~4 K in body-wearable applications, and a single solar cell in dark office environment, generates an output voltage as low as 200 mV, which is much lower than the threshold voltage of most standard CMOS technologies [2]-[5]. Fig. 1 illustrates a conventional cross-coupled switched-capacitance charge pump, behaving as a DC-DC voltage doubler with non-overlapping phase control signals [7][8]. With a low input voltage, it cannot work with a high PCE as with a high input voltage because of the large turn-on voltage, or equally, large on-resistance of the switches in the sub-threshold region. Start-up mechanisms could be employed to kick-start the system using an extra charge pump [5][11], external voltage [10], or mechanical switch [2], but they also increase the system complexity significantly [2][5][10][11].

The advent of non-CMOS technologies, such as the steep-slope tunnel field-effect transistors (TFETs), gives rise to possibility of a higher PCE for low-input-voltage applications [17]. TFET has already been drawing extensive attention at device, circuits, and architectural levels, and is considered as a promising candidate in the "post-CMOS" era for future low-voltage, high-efficiency computation and communication systems [18]-[29][31]-[34]. In this paper, we propose a step-up charge pump in a 20 nm III-V heterojunction tunnel field-effect transistor (HTFET) technology which is capable of boosting an input voltage as low as 0.20 V. The contribution of this paper mainly includes: (a) Exploration and optimization of the proposed HTFET charge pump is presented. The circuit parameters are analyzed and optimized for a high PCE with a low input voltage. In addition, the non-overlapping phase driver in conventional CMOS charge pumps is simplified to consume less power by the utilization of HTFET uni-directional current tunneling. (b) An improved cross-coupled charge pump topology is proposed, which increase both the output voltage and the PCE.

Simulation results show that with an input voltage as low as 0.2 V, the proposed HTFET charge pump has a peak PCE higher than 90%. The rest of this paper is organized as follows. Section II introduces the charge pump design challenges. Section III introduces the HTFET device and circuit-level modeling. Section IV presents the proposed HTFET charge pump design along with simulation results and discussions. Finally, Section V draws the conclusion.

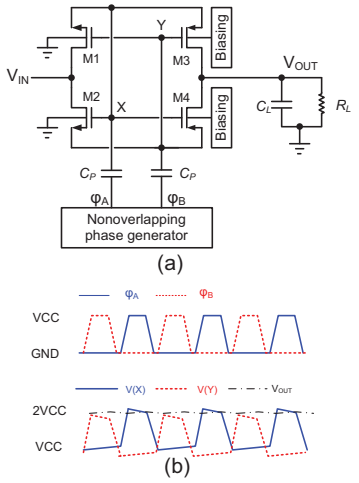

Fig. 1. A conventional cross-coupled charge pump.

II. CROSS-COUPLED CHARGE PUMP DESIGN CHALLENGE

A. The Circuit and Operation Theory

Fig. 1(b) illustrates the operation waveforms of the conventional cross-coupled voltage doubler in Fig.1(a). φ_A and

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φ_B are two non-overlapped phase control signals ranging from GND to VCC. V(X) and V(Y) are the voltage on the top plate of the pump capacitor C_P. When φ_A goes low and φ_B goes high, V(X) drops to below VCC and V(Y) increases to 2VCC; Also M1 and M4 are turned on while M2 and M3 are turned off. As a result, the top plate of capacitor C_P is charged to VCC through M1, and the output node is connected to the node Y through M4. In the opposite phase, the charge pump operations are similar.

B. The PCE Analysis and Design Challenges

As the most critical parameter in the charge pumps, PCE is defined as the ratio of delivered energy to the output load E_{OUT} to the input energy E_{IN} [6][7], i.e.

$$PCE = \frac{E_{OUT}}{E_{IN}} = \frac{E_{OUT}}{E_{OUT} + E_{LOSS}} \times 100\%, \quad (1)$$

where E_{LOSS} represents the energy loss by the charge pump itself. For a resistive load R_L, the E_{OUT} within a clock cycle T is

$$E_{OUT} = P_{OUT} T = \frac{\overline{V_{OUT}^2}}{f_{CLK} R_L}, \quad (2)$$

where f_{clk} represents the clock frequency. For the charge pump in Fig. 1, the energy loss E_{LOSS} could be described as

$$E_{LOSS} \approx E_{DRIVER} + E_{REDIS} + E_{SW} + E_{REVERS} + E_{COND}, \quad (3)$$

where E_{DRIVER} represents the energy consumed by the non-overlapping phase control driver, E_{REDIS} represents the energy loss due to the charge redistribution of capacitors when switching occurs, E_{SW} represents the switching loss due to charge and discharge of parasitic stray capacitance, E_{REVERS} represents the energy loss due to reverse current conduction through the switches, and E_{COND} represents the energy loss due to on-resistance of the switches and parasitic equivalent series resistance (ESR) of the capacitors [6]-[8].

With a lowered input voltage, the major challenge is how to overcome the large on-resistance to obtain a small E_{COND} and E_{SW} at the same time. Increasing the switch size is efficient in reducing the on-resistance, however, it inevitably makes the switching loss E_{SW} a new bottleneck.

III. HTFET Characteristics And Modeling

In this section, the HTFET technology and device model will be introduced. The 20 nm gate-length GaSb-InAs HTFET technology employed in this paper has a steep-slope I_{DS}-V_{GS} curve. It is one type of TFET that has been reported to present steep-slope and low-threshold characteristics [17]-[20].

A. TFET Device Characteristics

Fig. 2 illustrates simplified structures of Si FinFET, N-type HTFET, and P-type HTFETs [18]-[20]. Essentially, TFET is a reverse-biased, gated p-i-n tunnel diode with asymmetrical source/drain doping [17]-[20]. The off-state current I_{OFF} is controlled by the reverse biased diode leakage, and the on-state current I_{ON} is determined by the band-to-band tunneling at the source-channel junction under the gate control [17]-[20]. Two HTFET features have essential impact on the PCE of a charge pump, including the steep-slope and uni-directional conduction characteristics.

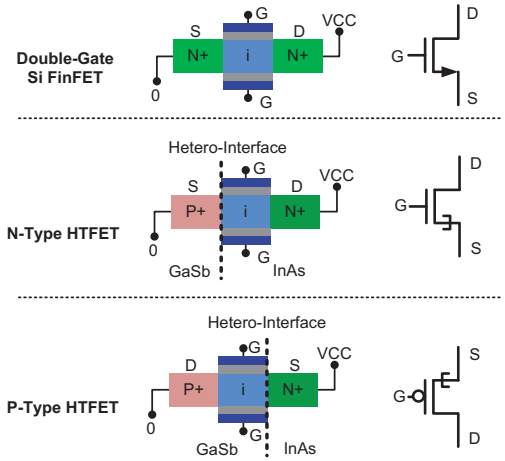

Fig. 2. Device structure and circuit symbol of N-type Si FinFET, N-type HTFET, and P-type HTFETs [18].

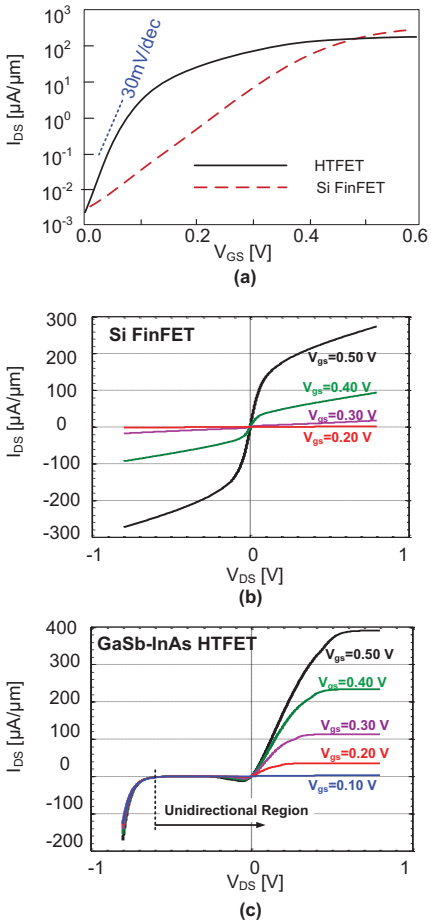

Fig. 3. Comparisons between Si FinFET and HTFET [18][20][23]. (a) Subthreshold slop comparison; (b) Si FinFET I_{DS}-V_{DS} curves; (c) HTFET I_{DS}-V_{DS} curves showing unidirectional tunneling current conduction.

Steep-Slope With A Low Input Voltage. Different from the CMOS process, the subthreshold slope (SS) of TFET is not limited to 60 mV/decade [17][18]. With III-V material and

heterojunction, the energy efficiency of III-V HTFET is higher than state-of-the-art CMOS technologies with a power supply lower than 0.5 V [19]. Fig. 3 shows the I-V comparisons. With 5 nA/um off-state leakage for low-power applications, the HTFET has an average SS of 30 mV/decade over two decades of current, and seven times improvement of on-state current over 20 nm Si FinFETs at a 0.30 V voltage supply [18][20]-[23].

Uni-directional Tunnel Conduction without Substrate Modulation. Thanks to the asymmetrical p-i-n structure and reduced drain doping to restrain the ambipolar transport, HTFET exhibits unique uni-directional tunnel current [18]-[20]. As shown in Fig. 3, when the p-i-n diode is forward-biased within -0.6 V < V_{DS}=V_{neg} < 0 V, the drain-source current is negligible compared with the VDS>0 V region.

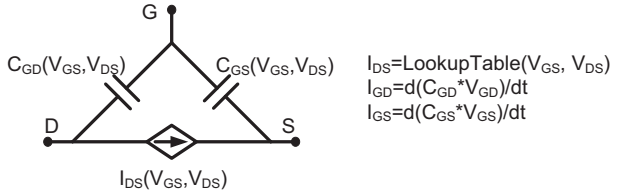

Fig. 4. HTFET circuit-level Verilog-A model [19][21].

B. HTFET Modeling for Circuit Simulations

Although no mature compact SPICE models have been developed, the Verilog-A model developed from TCAD Sentaurus [30] has been reported. After calibration by fabricated III-V TFET data, this model is able to capture both DC and transient characteristics, and is consistent with the atomistic simulations [31]. Fig. 4 shows the circuit-level Verilog-A HTFET model employed in this paper [19][21]. It is based on three two-dimensional look-up tables: $I_{DS}(V_{GS}, V_{DS})$, $C_{GS}(V_{GS}, V_{DS})$, and $C_{GD}(V_{GS}, V_{DS})$. This Verilog-A model has provided an accurate way to simulate the emerging HTFET device in previous designs [19]-[21][23].

IV. Proposed HTFET Charge Pump

Fig. 5 shows the proposed HTFET cross-coupled charge pump. This section first introduces the advantages over the conventional CMOS charge pumps in Fig. 1, and then gives optimizations and discussions together with simulation results.

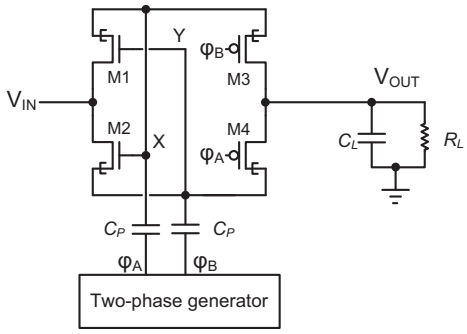

Fig. 5. Proposed cross-coupled HTFET charge pump.

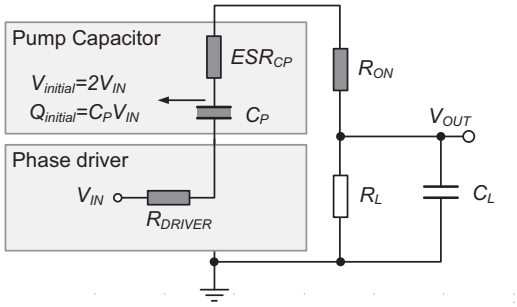

Fig. 6. Equivalent simplified circuit of the charge pumps in Fig. 1 and Fig. 4.

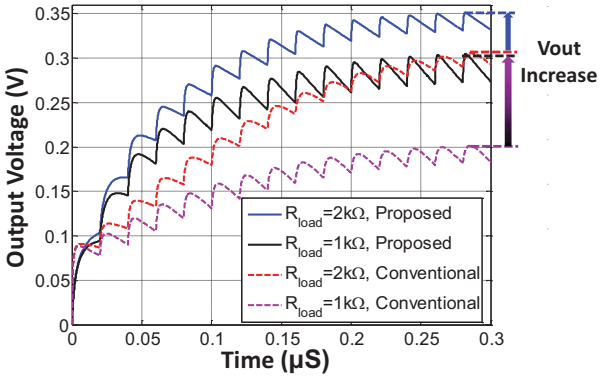

Fig. 7. Transient waveforms of the output voltage with and without the proposed improved topology.

A. Low-Input-Voltage Operation Capability

Fig. 6 shows an equivalent circuit of a charge pump, where ESR_{CP} is the ESR of the capacitor C_P, R_{DRIVER} is the output resistance of the phase control generator, and R_{ON} is the on-resistance of the turned-on switches. In the charging path, the conduction energy loss E_{COND} within a clock cycle is

$$E_{COND} = \int_0^{1/f_{CLK}} (I_D(t))^2 (ESR_{CP} + R_{ON}(t) + R_{DRIVER}(t))dt, \quad (4)$$

where $I_D(t)$ represents the instantaneous current flowing through the turned-on switch in the charging path [13]. From Eq. (4), a higher R_{ON} results in higher conduction energy loss E_{COND}. Therefore, as shown in Fig. 3, due to the steep-slope switching and a lower turn-on resistance with a low input voltage than the Si FinFET, the HTFET enables the DC-DC conversion with a low input voltage by a much lower E_{COND}.

B. Less Phase Driving Power and Less Reverse Power Loss

In conventional CMOS charge pumps in Fig. 1, the two phase control signals are non-overlapping so as not to turn on M1 and M3 (or M2 and M4) simultaneously. Otherwise, the output V_{OUT} will be connected to the VCC through M1 and M3 (or M2 and M4) directly, affecting the voltage boosting function. It is also noticed that the non-overlapping phase control does not eliminate all reverse energy loss. When both φ_A and φ_B are low in the non-overlapping phase, the two p-type switches are turned on, and a transient current flows from V_{OUT} to internal nodes X and Y, resulting in energy loss. In contrast, in the proposed HTFET cross-coupled charge pump, such

reverse current becomes negligible because of the uni-directional tunneling conduction. Therefore, the reverse energy loss is significantly reduced. Further, there is no need for non-overlapping phase control, which also simplifies the circuit design and saves driving power.

C. Improved Cross-Coupled Charge Pump

Different from conventional cross-coupled charge pumps in Fig. 1, the proposed charge pump shown in Fig. 5 redirects the gate control signals of the two output p-type switches, i.e. M3 and M4, to the bottom of the two capacitors C_P. As a result, the gate-source voltage difference $|V_{GS}|$ of M3 and M4 is 0 in the OFF region, and $2VCC$ in the ON region. With unique HTFET uni-directional tunneling, the OFF-state reverse current is negligible, which is impossible for CMOS designs without uni-directional current conduction. Compared with Fig. 1, the M3/M4 in Fig. 5 have similar ON-OFF behavior, but twice gate-source voltage $|V_{GS}|$ when turned on. In other words, the on-resistance of M3 and M4 is significantly reduced. Simulation shows that doubling $|V_{GS}|$ from 0.20 V to 0.40 V achieves about 83% on-resistance reduction. Fig. 7 shows the transient voltage waveforms of at the output port, showing significant higher output voltage with the proposed topology. In [6][7], a level shifter boosting the phase control swing from 0~VCC to 0~2VCC was employed to control PMOS switches, reaching the same on-resistance reduction. In contrast, the proposed topology needs no level-shifters, which saves area and power in return.

It is important to note that the proposed improved cross-coupled charge pump topology is designed specifically for the HTFET devices, by taking the advantage of the uni-directional tunneling current conduction capability. Differently, for the CMOS devices without such a uni-direction feature, the PMOS switches connected to the output node could not be fully turned off if the same topology is applied. In contrast, the PCE in this case would be deteriorated significantly accordingly. In other words, the improved cross-coupled topology is actually a device-circuit co-design innovation.

D. HTFET Charge Pump Optimization

Optimizations of the switch size and the pump capacitor C_P are presented for a high PCE for further understanding of the proposed topology. In the simulations, the phase control driver has the same transistor size as the switches in the charge pump. This setting is based on the fact that R_{DRIVER} of the phase driver and R_{SWITCH} of the switch are in series and affect the output in the same way, as illustrated in Fig. 6. The phase control clock frequency f_{CLK} and the load resistance R_L are set to be 30 MHz and 1.0 kΩ, respectively. A different clock frequency, or a multi-phase control could be used depending on the power budget of the control circuitry and the ripple requirement in the applications, which is beyond the scope of this paper.

Fig. 8 and Fig. 9 shows the simulated PCE and DC output voltage V_{OUT} versus the pump capacitor C_P and the switch size, respectively. When C_P is less than 100 pF, the pumped charge through C_P is insufficient to drive the load, resulting in a low V_{OUT} and PCE. However, when C_P is too large, the PCE turns to drop due to two facts: (a) the delivered power to the load is not further increased even if C_P is further increased; (b) much larger phase generator power is consumed to drive such a

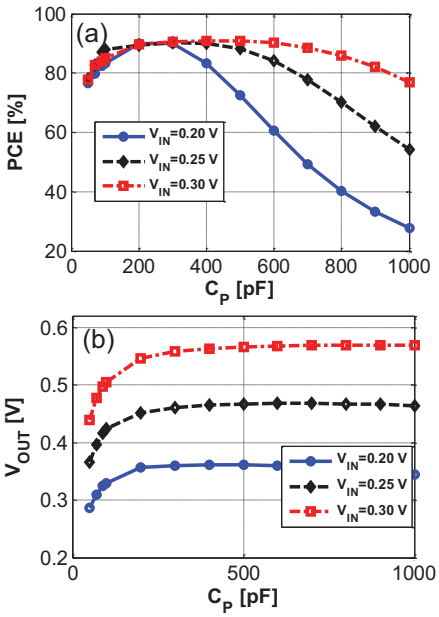

Fig. 8. C_P optimization of the proposed HTFET charge pump with 250 μm switch width: (a) PCE; (b) V_{OUT}.

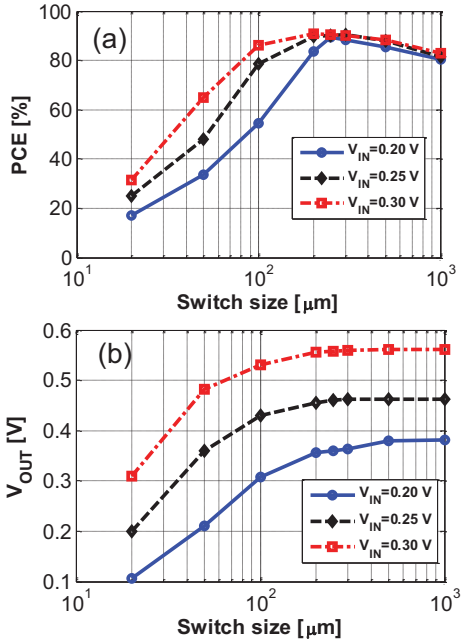

Fig. 9. Switch width optimization for the proposed HTFET charge pump with 300 pF C_P: (a) PCE; (b) V_{OUT}.

larger C_P. In the applications with a certain input voltage, a trade-off between the capacitor area and optimum PCE can thus be made accordingly.

As for the switch size optimization, because a larger switch size has lower on-resistance, the V_{OUT} increases with the switch size. Similarly, to reduce the dominating conduction energy

loss E_{COND} and obtain a high PCE, the transistor width needs to be large enough to make its on-resistance negligible. However, the PCE can be degraded by an excessively large transistor width which consumes more switching energy E_{SW}. When the input voltage V_{IN} is larger, this becomes more significant because E_{SW} is generally proportional to the square of V_{IN}.

After optimizations, the highest achieved PCE is larger than 90% for V_{IN} ranging from 0.20 V to 0.30 V. The maximum DC output voltage V_{OUT} is 0.37 V and 0.57 V, for a V_{IN} of 0.20 V and 0.30 V, respectively.

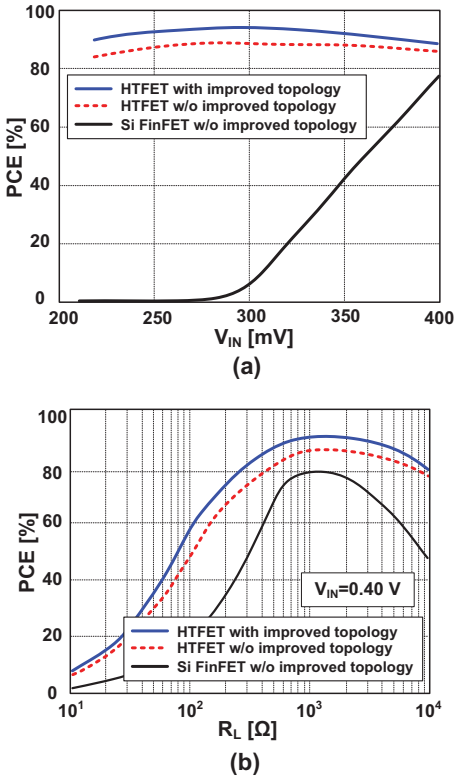

Fig. 10. Performance comparisons: (a) PCE versus V_{IN} with R_L=1.0 kΩ ; (b) PCE versus R_L with V_{IN}=0.40 V.

E. Performance Benchmarking

Fig. 10 shows the simulated performance comparisons between the Si FinFET charge pump and the proposed HTFET charge pump. The switch size, R_L, C_P, and f_{CLK} are set to be 250 µm, 1.0 kΩ, 300 pF, and 30 MHz, respectively. In Fig. 10(a), the PCE versus V_{IN} is shown with R_L=1.0 kΩ. For V_{IN}<0.34 V, the conventional Si FinFET charge pump has a PCE less than 40% and V_{OUT} is in fact lower than the input amplitude due to too large on-resistance of the switches. In contrast, the proposed HTFET charge pump has a >90% PCE when V_{IN} is as low as 0.20 V.

Fig. 10(b) shows the PCE versus R_L, which represents the load resistance impact on the performance. The change of R_L results in the change of the load current of the charge pump. When R_L increases, the PCE gradually increases to its peak because a larger R_L gathers more percentage of power with a size-fixed switch (see Fig. 6). Then PCE drops when R_L further increases, because the output power turns to decrease with further increasing R_L, while the input power is not decreasing by the same rate. Within the simulated R_L range 200 Ω to 10 kΩ, the HTFET charge pump has a higher PCE than the Si FinFET charge pump.

Fig. 10 also shows the performance comparison between the two HTFET charge pumps. When V_{IN} is small, the PCE improvement by the proposed charge pump is more significant than that of a high V_{IN}. This is because the on-resistance of the PMOS switches is larger and E_{COND} has more influence on the PCE. When R_L is small, the PCE improvement is limited by the on-resistance of the NMOS switches; when R_L is large, the PCE improvement is limited by the amount of delivered power. Within a target 30x range of 100 Ω to 3000 Ω, the impact of reducing E_{COND} is more significant. In this case, the proposed HTFET topology reduces the on-resistance and E_{COND}, and finally helps to increase the PCE, as shown in Fig. 10(b).

Table I gives the comparisons with recently fabricated voltage boosters. Extra start-up assistance is required for [10] and [11] when the input voltage is low. In contrast, the proposed HTFET charge pump can operate with VIN as low as 0.17 V without the need for start-up assistance. Compared with [9][12][13], the proposed HTFET supports much lower input voltage with a much higher PCE. With an input voltage range of 0.20~0.30 V, the proposed charge-pump has an output voltage range of 0.37~0.57 V, which is fair enough for steep-slope TFET and sub-threshold CMOS devices. The proposed charge-pump can also be cascaded to form multiple stages, if a higher V_{OUT} is required for certain high -voltage applications.

TABLE I. LOW-VOLTAGE VOLTAGE BOOSTER PERFORMANCE COMPARISONS *

	[10]	[11]	[9]	[12]	[13]	this work
Process	130 nm CMOS	65 nm CMOS	130 nm CMOS	350 nm CMOS	32 nm CMOS	20 nm HTFET
Start-up mechanism	external voltage	charge pump	none	none	none	none
Input voltage (V)	0.10 **(0.02 min.)**	0.18	1.0	0.6 **(0.5 min.)**	0.60	0.20
PCE	75%	/	82%	70%	75%	90.4%
Output voltage (V)	1.0	0.74	1.8	2.0	1.0	0.37

*: This work uses simulation data and the others experimentally measured.

It is noted that this work is based on simulations while the other works in Table I are experimentally measured due to the early infancy of the emerging HTFET technology with no industry fabrication support. Uncounted parasitics of the contacts and interconnections in this paper would more or less affect the optimized parameters and actual performance. On the other hand, our projected performance can also benefit from further HTFET device optimization that is still ongoing as compared to more mature CMOS process. Although it is still challenging to fabricate a commercial HTFET integrated circuit chip, we have factored effects like intrisic capacitance that could affect the circuit performance in the simulations. The comparisons with CMOS DC-DC charge pumps have indicated that the proposed HTFET charge pump is competitive in low-input-voltage applications. The simulations and discussions in

this paper, together with the proposed improved charge pump circuit topology, are of significance in both evaluating the HTFET technology and enhancing the performance of future energy harvesting and power management.

V. Conclusion

In this paper, HTFET device characteristics have been explored for performance enhancement in the proposed step-up switched-capacitance DC-DC voltage charge pump. Performance evaluation and design optimizations have been presented. Both theoretical and simulated results have shown that the proposed HTFET charge pump is superior with a high power efficiency at low input voltages. The improvement is achieved in part by the steep-slope switching, uni-directional tunneling conduction, and a simplified phase driver. The performance improvement is also achieved by the proposed novel cross-coupled charge pump topology to reduce the on-resistance. After design optimizations, the proposed charge pump achieves a simulated power efficiency higher than reported CMOS charge pumps. Further fabrication and measurement work is of significance.

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