Code-Independent Output Impedance: A New Approach to Increasing the Linearity of Current-Steering DACs

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***Abstract*—This paper proposes a novel complementary current approach to eliminating the code-dependence in the output impedance of current-steering digital-to-analog converters (DACs), and increasing the spurious-free dynamic range (SFDR) significantly. A 14bit 1.0GS/s current-steering DAC design example shows an SFDR increase of 10~15dB. In traditional designs, one major effect that degrades the linearity is the code-dependence of the DAC's output impedance, which becomes a bottleneck at high frequencies because of the parasitic capacitance in the current branches. By adding additional current sources and switches to keep the DAC's output impedance nearly constant at different digital input codes, the proposed approach increases the DAC's SFDR by tens of dBs.**

I. INTRODUCTION

To design a fast digital-to-analog converter (DAC) with a high spurious-free dynamic range (SFDR), a lot of work has been done on reducing glitches, increasing the DAC's output impedance, randomizing the switching transient errors, and achieving better component matching [1-7]. However, traditional solutions in published literatures have not successfully averted the SFDR degradation problem caused by the reduced output impedance at high frequencies [2][3]. This fact has become a bottleneck in designing a wide-band DAC with a high SFDR.

This paper proposes a novel complementary current approach to eliminating the code-dependence in the output impedance of a current-steering DAC. It obtains an SFDR increase by tens of dBs. In the approach, additional current branches including current sources and switches are added in parallel with the original current branches. Although the output impedance of a current branch decreases as the frequency increases, the DAC's output impedance becomes nearly constant at varying digital input codes. Such code-independence suppresses the harmonics in the output greatly.

In this paper, section II introduces the new approach. Section III gives a 14bit, 1.0GS/s current-steering DAC and section IV gives the conclusion.

II. THE PROPOSED APPROACH TO INCREASING CURRENT-STEERING DACS' SFDR

Fig. 1 shows a conventional current-steering DAC with typical current source and switch units. The current in each unit is switched either to the positive or to the negative output node, depending on the digital input code. So the number of parallel current branches switched to an output node is a function of the input code, so is the DAC's output impedance. This makes the DAC's load, which is the parallel combination of external resistors and the DAC's output impedance, code-dependent. Further, harmonics occur in the output because of the code-dependence, as given in [3] [6]. Furthermore, let N be the total number of current sources for a thermometer-decoded DAC, I_0 be the current of the least significant bit (LSB), R_L be the constant resistive load at each output of the DAC, Z_0 be the output impedance of a current branch composed of a current source and switch unit, and the output analog signal be $\sin(\omega t)$, then the differential output voltage can be derived as

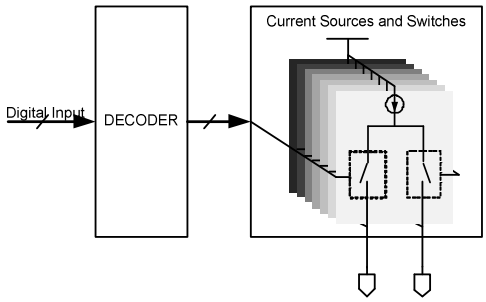

Fig. 1. A conventional current-steering DAC structure.

$$V_{out}(\omega t) = \frac{4I_0 Z_0^{\,2}}{NR_L}\frac{\sin(\omega t)}{(2Z_0/N/R_L+1)^2-\sin(\omega t)^2}. \quad (1)$$

Using Taylor series expansion and Fourier series method, (1) results in

$$V_{out}(\omega t) = \frac{4I_0 Z_0^{\,2}}{NR_L}\times(B_1+B_2+\cdots), \quad (2)$$

where

$$B_1 = (64A^3+48A^2+40A+35)\sin(\omega t), \quad (3)$$

$$B_2 = -(16A^2+20A+21)\sin(3\omega t), \quad (4)$$

$$A = (2Z_0/N/R_L+1)^2. \quad (5)$$

So, the SFDR determined by the third order harmonic is

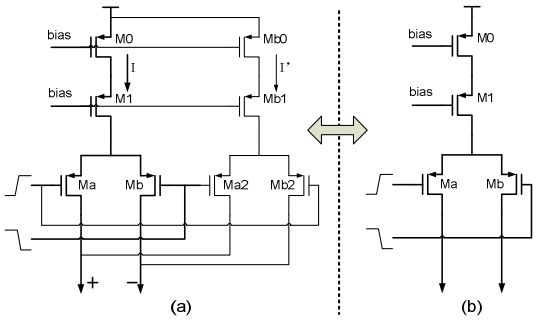

Fig. 2. The proposed current source and switch unit in (a) and a corresponding traditional unit in (b).

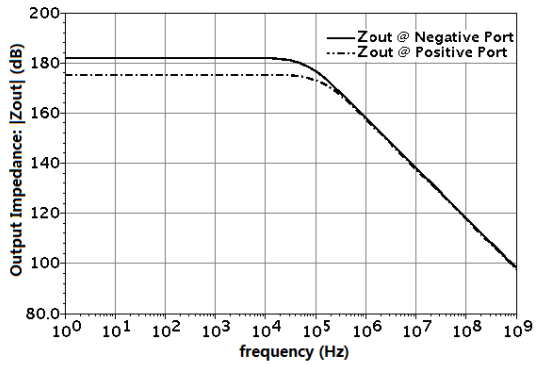

Fig. 3. A simulation result of the output impedance (in dB) at the two output ports in Fig. 2, when Ma/Mb2 are "on" and Mb/Ma2 are "off".

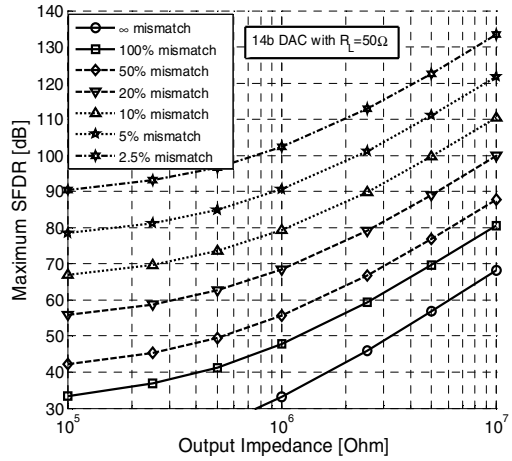

Fig. 4. Calculated SFDR of (14) for different output impedance (Z_{out}) and mismatch errors between Z_{out}' and Z_{out}.

$$SFDR = 20\lg\left(\frac{64A^3 + 48A^2 + 40A + 35}{16A^2 + 20A + 21}\right)(dB). \quad (6)$$

This conclusion also holds for segmented DACs. In order to achieve a >70dB SFDR, the output impedance of a LSB current branch must be >2.9 mega ohms if the DAC's load is 50ohm. For a 6+6 segmented DAC, the parasitic capacitance of one most-significant-bit must be less than 7fF at 500MHz, which is challenging to satisfy with large current transistors and long interconnection lines in traditional DAC designs.

It is clear that the harmonics occur when the output impedance of the DAC fluctuates with the input code. If the dependence of the DAC's output impedance on input code is removed, i.e. the $\sin(\omega t)$ term is removed from the denominator in (1), then the harmonics would disappear and SFDR would increase.

We propose a new approach, named complementary current solution, to suppressing the code-dependence of the output impedance. It is illustrated in Fig. 2 (a). Compared with the traditional current source and switch unit shown in Fig. 1 and repeated in Fig. 2 (b), the difference is the additional current branch composed of a cascaded current source labeled as Mb0 and Mb1 and two switches labeled as Ma2 and Mb2. Mb0 and Mb1 have the same gate length and bias conditions as M0 and M1, respectively, but different in gate width. Ma2 and Mb2 utilize the same control signals as Ma and Mb. By doing this, the current of M0 and Mb0 flows to different output nodes at the same time. More importantly, for each current source and switch unit, there is always one current path from each output node to the power supply through a switch and a current source, no matter what the control signals are. As a results, the number of a DAC's parallel current branches switched to an output node is no longer a function of the DAC's input code, and the term $\sin(\omega t)$ in (1) is suppressed, i.e., the output harmonics in (2) is suppressed.

The current flowing through M0 and Mb0 must not be the same; otherwise the differential output of the current branch would be zero. In Fig. 2, when Ma is on and Ma2 is off, the output resistance at the positive output node of the current source and switch unit equals

$$R_{out} \approx g_{m\_Ma} r_{ds\_Ma}\left(g_{m\_M1} r_{ds\_M1} r_{ds0}\right) \approx \frac{4V_E L_{Ma}}{V_{ov\_Ma}} \frac{V_E L_{M1}}{V_{ov\_M1}} \frac{V_E L_{M0}}{I_D}. \quad (7)$$

At DC, the output resistance at the port which carries more current is smaller than that at the other port because of larger I_D in (7). At higher frequencies, for example, tens of mega hertz, the difference between the two output impedance is much smaller. In Fig. 3, an HSPICE simulation result of the circuits in Fig. 2 shows a difference less than 10% at frequencies higher than 10MHz. As a result, when Ma is turned off and Ma2 is on, the output impedance of the current branch remains nearly unchanged. And the differential output of the DAC under a sinusoid input is

$$V_{out}(\omega t) \approx \left(NI_0 \sin(\omega t)\right) \times \left(R_L \parallel (Z_0 / N)\right). \quad (8)$$

So the harmonics are greatly suppressed in the output. In reality, the output impedance difference between the positive and negative output nodes of a current source and switch unit is not zero, e.g. 10% in Fig. 3. This leads to some third order distortion in the differential output. Let N be the total number of current sources in a thermometer-decoded current-steering DAC, I_0 be the current flowing through M1, I_0' be the current flowing through Mb1, I be the sum of I_0 and I_0', and ΔI be the difference, then the positive current output of the DAC is

$$I_o^+ = \frac{1+\sin(\omega t)}{2} NI_0 + \frac{1-\sin(\omega t)}{2} NI_0' = \frac{N}{2}\left(I + \Delta I \sin(\omega t)\right), \quad (9)$$

And the output impedances of the positive branch is

$$Z_o^+ = R_L \parallel \frac{Z_{out}}{(1+\sin(\omega t))N/2} \parallel \frac{Z_{out}'}{(1-\sin(\omega t))N/2} \triangleq \frac{A}{B - \sin(\omega t)}, \quad (10)$$

where

$$A=\frac{2Z_{out}k}{N(1-k)},\ B=\frac{2Z_{out}k+NR_L(1+k)}{(1-k)NR_L},\ k\triangleq\frac{Z_{out}'}{Z_{out}}, \quad (11)$$

and Z_{out} is the output impedance of a current branch at one output port which carries more current, and Z_{out}' is the output impedance at the other port which carries less current. Let x represent $\sin(\omega t)$, then the differential output voltage is

$$V_{out}=I_o^+Z_o^+-I_o^-Z_o^-=\frac{AN(B\Delta I+I)}{B^2}\left(x+\frac{x^3}{B^2}+\frac{x^5}{B^4}+\cdots\right). \quad (12)$$

Neglecting the terms with orders high than seven, using Fourier transform, (12) can be reshaped to be

$$V_{out}=\frac{AN(B\Delta I+I)}{B^2}\left((1+\frac{3}{4B^2}+\frac{5}{8B^4}+\frac{35}{64B^6})\sin(\omega t)\right.$$
$$\left.-(\frac{1}{4B^2}+\frac{5}{16B^4}+\frac{21}{64B^6})\sin 3(\omega t)+\cdots\right), \quad (13)$$

yielding the third order harmonic determined SFDR to be

$$SFDR=20\lg\left(\frac{64B^6+48B^4+40B^2+35}{16B^4+20B^2+21}\right), \quad (14)$$

where B is defined in (11).

The corresponding curve for a 14-bit DAC with R_L=50ohm is calculated and plotted in Fig. 4. The bottom line with round markers is the SFDR curve as a function of the output impedance of the LSB current source (Z_{out}), assuming the ratio of Z_{out}' and Z_{out} to be ∞. The others lines use the complementary current solution and have different matching errors between Z_{out}' and Z_{out}.

Two conclusions can be drawn from the results of Fig. 4:

i. Larger output impedance yields higher SFDR for a fixed matching errors between Z_{out}' and Z_{out}. In other words, the increase of the output impedance is beneficial to the improvement of SFDR, no matter the complementary current is applied or not.

ii. Better matching yields higher SFDR at fixed output impedance. If the matching error is reduced from 100% to 10%, the SFDR increases by about 30dB. Further, even if the output impedance is not large enough for the SFDR requirements in conventional DAC architectures, getting better output impedance matching would still be an effective way to meet the SFDR requirements. For example, when the output impedance of the current source and switch unit is 100k ohm, the SFDR of the DAC's output may still be larger than 65dB if the matching error is less than 10%. Otherwise the SFDR would be less than 45dB if the matching error is more than 50% (a typical case when the complementary current is not applied).

The second conclusion discussed above is different from any other existing techniques and exhibits new possibilities for designing wide-band DACs with high SFDR. As the scaling of complementary metal–oxide–semiconductor (CMOS) technologies, the intrinsic gain and output impedance are severely lowed [8], but the proposed complementary current approach is still effective for better output impedance matching and higher SFDR.

The disadvantage of the complementary current solution is

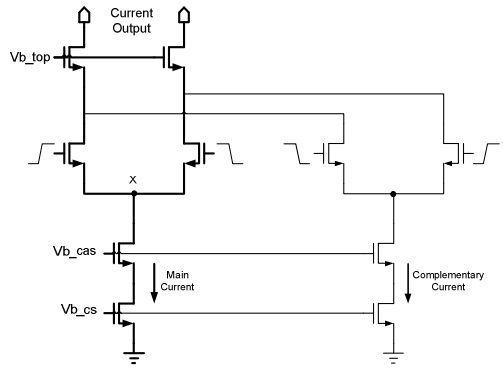

Fig. 5. The current source and switch unit used in the 14-bit 1.0 GS/s current-steering DAC using the proposed complementary current.

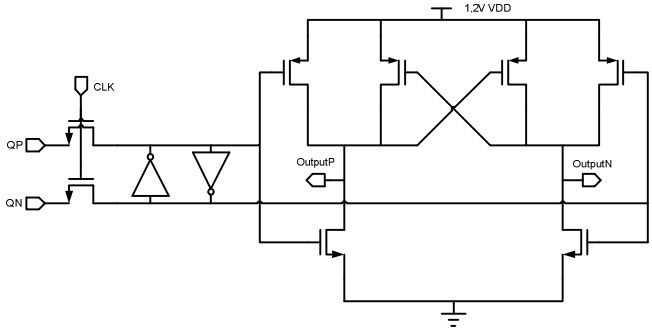

Fig. 6. The latch used in the 14 bit 1.0GS/s DAC.

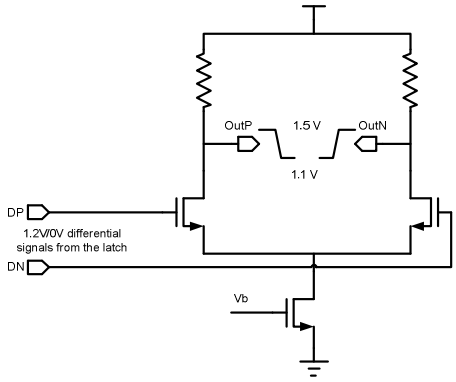

Fig. 7. The level-shifter used in the 14 bit 1.0GS/s DAC.

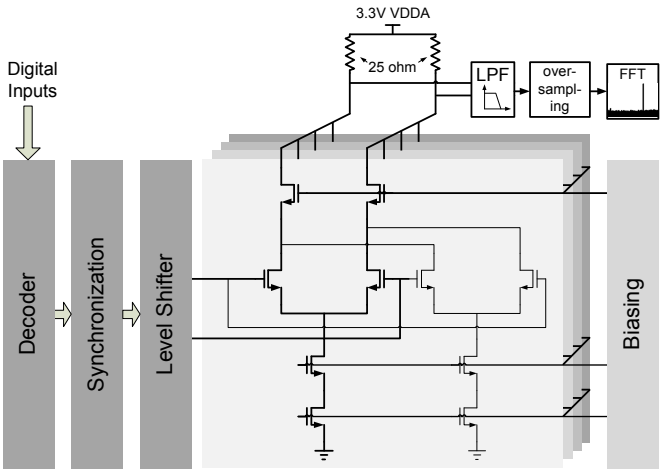

Fig. 8. The simulation diagram of the 14 bit 1.0GS/s DAC.

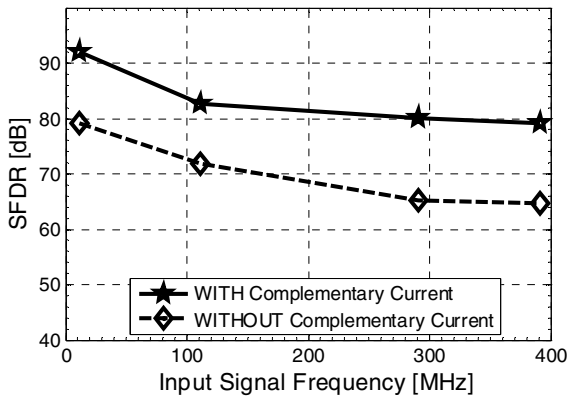

Fig. 9. The simulated SFDR of the 14 bit 1.0GS/s current-steering DAC.

more power consumption because of the additional current branches. It introduces two side effects: more current and less voltage headroom. In fact, these effects are not the key factors in the DAC design. For one thing, the additional static current is only a small part of the total current consumed by a fast DAC with power-hungry digital circuits. For another thing, if the complementary current is small, the decrease in the voltage headroom is negligible. What's more, the additional current forms a common-mode voltage at the DAC's positive and negative output nodes, and the use of a higher supply provides the same voltage headroom and the same working conditions for the transistors, without the worry about the transistors' stabilities.

III. A 14-BIT 1.0GS/S DAC DESIGN EXAMPLE

To further verify the effectiveness of this new technique, a 6+8 segmented current-steering DAC is designed using 0.13μm CMOS technology. The 6 MSB's are thermometer-decoded and the 8 LSB's are binary-decoded.

i. The Current Source and Switch Unit.

The analog part uses NMOS current sources with 3.3 V power supply and applies 1.5/1.1 V low-swing control signals for the switches. The current source and switch unit is shown in Fig. 5. The main current branch, i.e. the original current branch before utilizing the complementary current, is drawn in bold. The ratio between the main current and the complementary current is 5:1. All transistors in the complementary current branch are scaled according to the current ratio. For an output swing of 1-Vpp, the MSB main current is 390μA and the MSB complementary current is 78μA. The LSB currents are scaled proportional to the digital weights. Different from the current branch given in Fig. 2, a pair of cascaded transistors with thick-gates and a bias *Vb_top* is placed on top of the differential current output, for the sake of larger output impedance and better output impedance matching between the main current branch and complementary current branch.

ii. Simulations.

The inputs of the latches, QP and QN in Fig. 6, are generated by a 6-bit thermometer decoder. The timing and driving abilities of the decoder's outputs should be carefully dealt with. This DAC has been simulated at the sampling frequency of 1.0 GS/s. In the simulation, the full-scale differential current is 20mA and the differential output swing is 1.0V. Fig. 10 shows the simulation diagram, where the 4th order Butterworth low-pass filter (LPF) has a pass-band of 500MHz and the oversampling frequency is 40GHz.

After the implementation of the complementary currents, the output impedance mismatch is reduced from 30% to 8%. Calculations using (14) results in a 20dB SFDR improvement. And the 14bit 1.0GS/s DAC simulations results, as illustrated in Fig. 9, reveal that the SFDR increases by 10~15dB after using the proposed implementation of complementary current. Although there is a discrepancy in the simulation and calculation results, the simulations attest the function of the complementary current, reaching a SFDR of 79.2dB under a sinusoid input of 391MHz.

IV. CONCLUSION

The complementary current solution to the elimination of the code-dependence in the current-steering DAC's output impedance is proposed. Different from traditional techniques, additional current branches with corresponding control signals are applied in parallel with the original current branches, to keep the DAC's output impedance nearly constant at different digital input codes and thus increase the SFDR by tens of dBs. In this paper, the principle of this approach is analyzed, and two ways of increasing SFDR, i.e. increasing output impedance and improving output impedance matching, are also compared and discussed. For the purpose of higher SFDR, it is of significance to further improve the output impedance matching by using the complementary current in the future.

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