A 14-Bit 1.0-GS/s Dynamic Element Matching DAC with >80 dB SFDR up to the Nyquist

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***Abstract*—A 14-bit 1.0-GS/s current-steering digital-to-analog converter (DAC) was designed in a 65-nm CMOS process. For such current-steering DACs with a high sampling rate, the code-dependent load variations and switching glitches are a main bottleneck which limits the spurious-free dynamic range (SFDR). Dynamic element matching (DEM) has been an effective solution to randomize these glitches for a higher SFDR and also to reduce the matching requirement of the current cells for an area-efficient design which also improves the SFDR with reduced parasitic capacitance. An effective method named TRI-DEMRZ is proposed in this paper, consisting of time-relaxed interleaving, DEM and return-to-zero encoding. We also apply TRI-DEMRZ in synergy with complementary switched current sources (CSCS) to design the DAC for the purpose of a small die size and enhanced SFDR performance. Post-layout simulations show >80 dB SFDR up to the Nyquist. This DAC has a mixed 1.2 V / 2.5 V power supply and an active area of 0.48 mm^2.**

Keywords—Digital-to-analog converter (DAC); mismatch; Dynamic element matching (DEM); return-to-zero (RZ); spurious-free dynamic range (SFDR)

I. INTRODUCTION

Current-steering digital-to-analog converters (DACs) with a high resolution and a high sampling rate have been widely used with increasing spectrum performance requirement such as the spurious-free dynamic range (SFDR) [1]-[7]. Fig. 1 shows the basic structure of a traditional current-steering DAC. The digital inputs are decoded into control signals, switching the current sources to either the positive or negative output node and forming a differential output voltage.

For high-speed DACs, the current source mismatches [1], [2], [8]-[10], code-dependent load variations [3]-[5], [11] and code-dependent switching glitches [2]-[4], [7] are the main issues that limit the SFDR. At higher frequencies, the finite output impedance due to parasitics worsens the code-dependent load variation and deteriorates the SFDR. A smaller current-source transistor can be adopted for less parasitics but will do harm to the matching performance of the current sources [2]. Dynamic element matching (DEM) has been a solution to using smaller-sized transistors while maintaining good matching properties and achieving better SFDR, as its randomized decoder mitigates not only the current source mismatch but also the effect of the code-dependent switching glitches [1], [2], [10].

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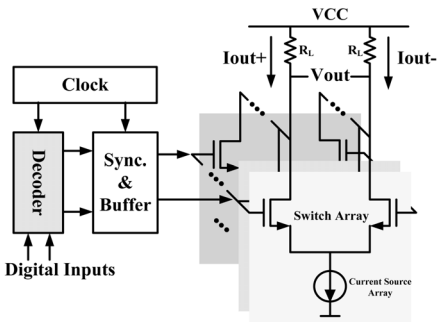

Fig. 1. Diagram of a traditional current-steering DAC.

In this paper, an effective time-relaxed interleaving return-to-zero DEM (TRI-DEMRZ) technique is proposed to design a 14-bit 1.0-GS/s CMOS DAC with > 80 dB SFDR up to the Nyquist. The complementary switched current sources (CSCS) in [3] are employed to further compensate the code-dependent load variations due to the finite output impedance effect.

II. PROPOSED TRI-DEMRZ TECHNIQUE

With the development of CMOS process, transistor mismatch is becoming a challenge especially for high resolution DACs. Another challenge is the code-dependent switching glitches which inherently result in harmonic distortions and limit the SFDR. One effective solution to the mismatch is to use sufficiently large-area current source transistors together with the switching sequence optimization [16], but this results in larger chip area and larger parasitic capacity, which leads to deteriorated finite output impedance and switching glitches, especially at a higher sampling rate and signal frequency. Another choice is the use of calibration techniques with additional costs [9], [17]. The third choice is the Dynamic Element Matching (DEM), which has been widely adopted to make DAC outputs insensitive to transistor mismatch for higher SFDR performance while maintaining smaller chip area without calibration costs [1], [2], [10]. Furthermore, by modulating the switching activities of the current sources randomly, DEM is also effective in SFDR improvement through randomizing the switching glitches and thus suppressing the harmonic distortions [10]. Fig. 2 shows

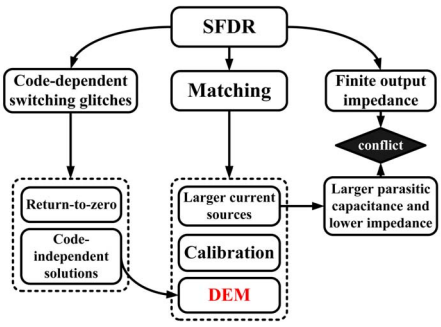

Fig. 2. Interrelation and trade-off of different techniques for DAC design.

the interrelation and trade-off of the above techniques for DAC design.

A. Theory of Dynamic Element Matching

In traditional DACs, the mapping between the digital input code and the switch control signals generated by the decoder in Fig. 1 remains unchanged. Accordingly, the chosen current sources remain the same with the specific input, which is the main cause of code-dependent issues.

In a DEM decoder, the mapping between the input code and the switch control signals is randomized, so the chosen current sources with the same input will be random every clock cycle, while the total number of chosen current sources remains the same. For example, an *N*-bit DEM decoder with an input digital code *P* will randomly select *P* output codes to be "*1*" from a total of (2^N-*1*) outputs every clock cycle. This randomization detaches the output code-dependent issues from the input code and turns both the mismatch-caused distortions and the code-dependent harmonics into white noise, which mitigates the area demand for matching property and improves the output SFDR.

B. Existing DEM and TRI-DRRZ Techniques

Existing DEM decoders are usually based on traditional binary-to-thermometer decoders, with complex randomization algorithms [2]. This makes it difficult to realize a fully-random DEM decoder, especially for high resolution ones, since the complexity may increase exponentially [10].

A simplified DEM implementation named Random Rotation-Based Binary-Weighted Selection (RRBS) is given in [1], which significantly mitigates the design complexity. Fig. 3 shows the structure of an *N*-bit RRBS DEM decoder, which is made up of a simple *N*-bit binary weighted decoder and a simple random shifter. By randomly rotating the control list of the binary weighted decoder outputs, this RRBS decoder realizes a nearly random mapping relationship.

This RRBS decoder is easy to design even though higher-order RRBS decoders have more complex interconnection and parasitic resistance. However, it is apparently not a fully random decoder because the wiring connection for the same input bit are always in a sequence, and these adjacent switch control signals will rotate together, giving successive decoder outputs. As the signal frequency increases, less randomization room is achievable. As an example, when the signal frequency

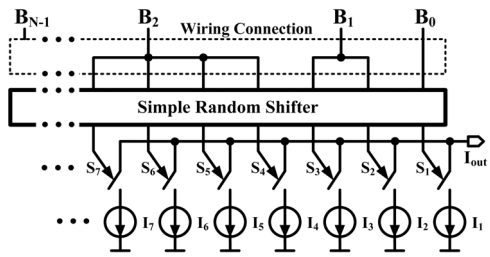

Fig. 3. Structure of an N-bit RRBS DEM decoder.

approaches the Nyquist, almost all switches are turned on or off which leaves almost no room for randomization. Because the functionality of DEM is purely the result of randomization, DEM may not function well without enough randomization.

Time-relaxed interleaving digital-random-return-to-zero (TRI-DRRZ) [3] can be introduced to improve the degree of randomization for existing DEM techniques. In TRI-DRRZ, two sub DACs are alternately controlled by the thermometer decoder and random RZ signals. By adding the second sub DAC, even in near-Nyquist signal frequencies, the switching operations could still be fully random.

C. The Proposed TRI-DEMRZ Technique

The TRI-DEMRZ technique we proposed in this paper successfully integrates the TRI-DRRZ and DEM techniques to implement a DEM decoder with enough randomization and less code-dependent switching glitches. Fig. 4 shows the TRI-DEMRZ diagram. Using *N* swappers each composed of a pair of 2-to-1 multiplexers, two sub DACs are alternately controlled by the *N*-output DEM decoder and *N* random RZ signals generated by the pseudo random number generator (PRNG), where *N* stands for the total number of current sources in one DAC, and the outputs of the two sub DACs are added together, forming the entire DAC output. The PRNG can be reused for the DEM decoder.

In TRI-DEMRZ, we propose a simplified DEM implementation with a 6+4+4 segmented decoder for a higher level of randomness and better linearity, using RRBS for the 6 Most Significant Bits (MSBs) and 4 Upper Significant Bits

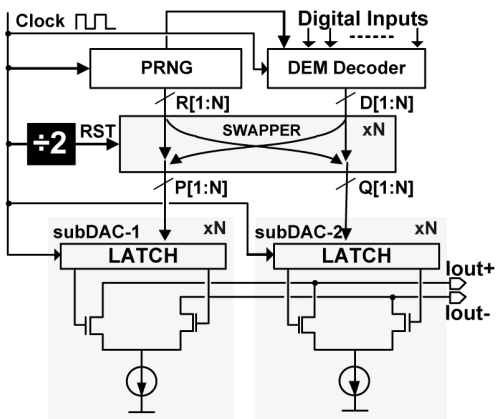

Fig. 4. Diagram of the proposed TRI-DEMRZ.

(USBs). The 4 Least Significant Bits (LSBs) use simple binary weighted decoder. The 6-bit MSB DEM decoder is built by reusing four 4-bit RRBS decoders instead of simply a 6-bit RRBS, with greatly reduced scale and design complexity. Fig. 5 shows the realization of this 6-bit decoder, with the allocation of the input codes. In this implementation, inputs of the higher bits are allocated into four different sub RRBS decoders, and the sub decoders which are given different random numbers will rotate separately, with an improvement of randomness for output control signals.

By combining TRI-DRRZ with the simplified segmented DEM implementation, our TRI-DEMRZ achieves a higher level of randomness, and the effect of the current source mismatch and switching glitches is greatly mitigated. Compared with [2], the settling time is relaxed from half a clock cycle to one clock cycle which highlights the advantage of relaxed-timing design. The interleaving operation also enables increased signal power and flattened spectrum envelop in the 1st Nyquist zone [3]. Section IV will verify the effectiveness of TRI-DEMRZ.

III. THE 14-BIT 1.0-GS/S TRI-DEMRZ DAC DESIGN

A 14-bit 1.0-GS/s DAC in 65-nm CMOS is implemented with the proposed TRI-DEMRZ technique. Fig. 6 shows the architecture of this DAC, including a current source and switch array, a latch array, a TRI-DEMRZ decoder, and a clock generation block. The DAC has a power supply of 1.2 V (digital) and 2.5 V (analog), with a 50 Ω differential load and a 16 mA full-scale current output.

As discussed in Section II, this DAC is segmented into 6 MSBs, 4 USBs and 4 LSBs for both high linearity and less area cost. TRI-DEMRZ is applied to the decoder, and the two sub DACs are realized with the same circuit and layout. These two sub DACs alternately work in the RZ phase and the DEM phase. A 32-bit linear feedback shifting register (LFSR) is used as the PRNG for random number generation for both the RZ signal module and the DEM decoder.

CSCS in [3] is employed in this paper to further mitigate the code-dependent load variations caused by the finite output impedance effect. Fig. 7 shows the structure of a CSCS unit. By adding an additional complementary current branch with optimized amount of "bleeding" current I_0' to the main current I_0, this structure reduces the output impedance difference of switched on and switched off current routes, which greatly mitigates the code-dependent load variation effect due to finite output impedance. As analyzed in [3], CSCS also contributes to differential glitch cancellation, which is also helpful for mitigating the effect of the extra switching operation in a DEM DAC.

CSCS is applied to both MSBs and USBs, in which a 16 μA current source is used as the current unit. Each MSB current source is made up of 20 such units for the main current and 4 units for the complementary current, forming a differential output of 256 μA. In USBs, the number of current units for main current and complementary current is 2 and 1, forming an output of 16 μA. In LSBs, The 16 μA current unit is divided into 8 μA, 4 μA, 2 μA and 1 μA for LSB outputs, and another 1μA as a dummy current source.

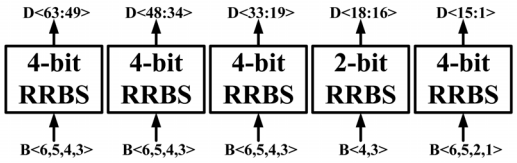

Fig. 5. Diagram of the proposed 6-bit DEM decoder.

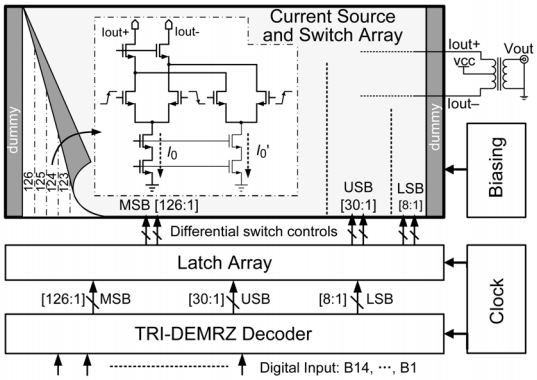

Fig. 6. Architecture of the 14-bit 1.0-GS/s DAC.

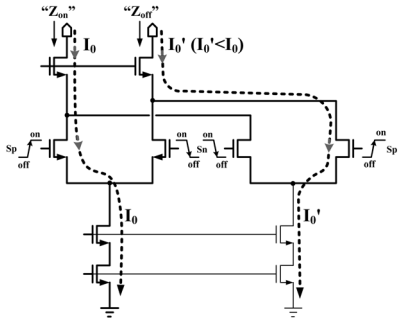

Fig. 7. The CSCS unit.

Both the sub DAC in TRI-DEMRZ and the complementary current sources in CSCS introduce more transistors and lead to a larger chip area. As we analyzed in Section II, randomization of DEM mitigates the effect of transistor mismatches, so we can reduce the area of current sources while maintaining enough matching property. Based on the matching model in [8] and simulation results about mismatch in Section V, we adopt smaller-sized current sources with required sigma(I)/I for an INL yield of 90% [12]. Smaller chip area also mitigates gradient matching errors in the current source array, as discussed in [3].

Fig. 8 shows the overall layout of this DAC design in a 65 nm 1P8M CMOS process. The DAC core area is only 1.2 × 0.4 mm^2, and the entire chip area is 1.9 × 1.1 mm^2.

IV. SIMULATION RESULTS

Simulation results are given in this section in order to verify the effectiveness of the proposed TRI-DEMRZ.

Based on the current source design introduced in Section III and the CMOS process mismatch characteristic projection provided by the foundry, a 0.2% normal distributed mismatch

is derived and added to the pre-layout simulation, with the results shown in Fig. 9(a). As shown in Fig. 9(a), the primordial DAC without DEM and TRI-DRRZ has the lowest SFDR performance. DEM is proved effective in mitigating mismatches, and TRI-DEMRZ can effectively improve the performance of DEM by more degree of randomization and cancellation of the switch glitches caused by DEM.

At 1.0 GS/s sampling rate, this TRI-DEMRZ DAC with ideally matched elements has an SFDR of 103 dB at 11 MHz signal frequency and 93 dB at 491 MHz for pre-layout simulation. For post-layout simulation with extracted parasitics, this DAC realizes an SFDR of 87.2 dB at 11 MHz and 80.4 dB at 491 MHz signal frequency, achieving >80 dB SFDR up to the Nyquist.

Fig. 9(b) shows the post-layout simulated SFDR performance compared with some recent related works. TABLE I gives the comparison among these DACs. The proposed TRI-DEMRZ DAC achieves a higher SFDR for post-layout simulation over the entire Nyquist band with a relatively smaller core area.

V. Conclution

A 14-bit 1.0-GS/s 0.48 mm^2 current-steering CMOS DAC has been presented with > 80 dB SFDR in the entire Nyquist band. The proposed time-relaxed interleaving return-to-zero DEM (TRI-DEMRZ) technique has been discussed in detail and verified by this DAC. Using TRI-DEMRZ for such a small-area DAC design, the effect of both the current source mismatches and the code-dependent glitches are mitigated effectively. TRI-DEMRZ is also able to work together with complementary switched current sources (CSCS) to further compensate the finite output impedance effect and improve the spectrum performance.

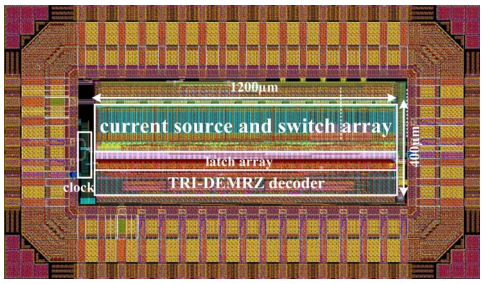

Fig. 8. Layout of the proposed DAC.

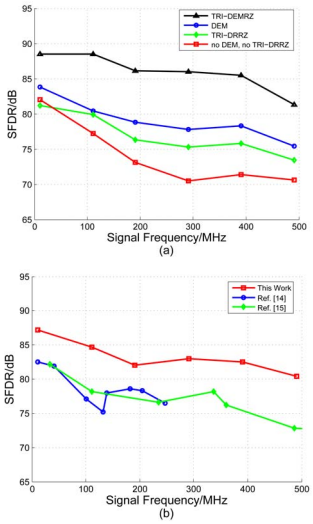

Fig. 9. Simulation results. (a) Pre-layout simulation for matching property. (b) SFDR performance comparisons.

TABLE I. Comparisons Between Related DACs

Specifications	This work	Ref. [14]	Ref. [15]
Technology (nm)	65	180	65
Core area (mm^2)	0.48	1.44	0.9
Sampling rate (GS/s)	1.0	0.5	2.0
Resolution (bits)	14	12	14
$SFDR_{LF}$ (dB)	87	82	82
$SFDR_{fs/2}$ (dB)	80	76	70

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