Yu Wang

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GENDER: MALE

BIRTH: 21/03/1982, MAANSHAN, ANHUI, PEOPLE'S REPUBLIC OF CHINA

EDUCATION

09/2002 – 07/2007 **PhD** (with honor), co-supervised by Prof. Huazhong Yang and Prof. Yuan Xie
Circuit and System Division, Department of Electronic Engineering, Tsinghua University
Dissertation – Optimization for Leakage Current and Reliability in Digital Integrated Circuits

09/1998 - 07/2002 **Bachelor of Science in Electronic Engineering**
Department of Electronic Engineering, Tsinghua University

09/1996 –07/1998 National Science Experimental class (High School attached to Tsinghua University)

RESEARCH SUMMARY

Dr. Yu Wang is an Associate Prof. in EE Dept, Tsinghua University. Dr. Wang's research mainly focuses on parallel circuit analysis, brain inspired computing, application specific hardware computing (especially on the Brain related problems), and power and reliability aware system design methodology. He is an IEEE Senior Member.

Dr. Wang has authored and coauthored over 130 papers in refereed journals and conferences. He is the recipient of IBM X10 Faculty Award in 2010, Best Paper Award in ISVLSI 2012, Best Poster Award in HEART 2012, and 6 Best Paper Nomination in ASPDAC/CODES/ISLPED. He serves as the Associate Editor for IEEE Trans on CAD, Journal of Circuits, Systems, and Computers. He is the TPC Co-Chair of ICFPT 2011, Finance Chair of ISLPED 2012/2013/2014, and serves as TPC member in many important conferences (DAC, FPGA, DATE, ASPDAC, ISLPED, ISQED, ICFPT, ISVLSI, etc).

RESEARCH AND WORK EXPERIENCE

12/2011 – now **Associate Prof.**
Head (2011.01-2014.04), Research Institute of Circuits and Systems
Vice Chair of the Department in Charge of the students' Affairs (2013.07- now)
Department of Electronic Engineering, Tsinghua University

- Application specific Hardware Computing, for brain/network/video applications
- Parallel circuit analysis (Sparse Linear System Solver)
- Emerging technology for circuits and systems (3D and NVM based design)
- Low power/reliability aware circuit design methodology

04/2011 – 07/2013 **Visiting Scholar**
Imperial College, London, with Prof. Wayne Luk

- Optimising performance and energy efficiency for large-scale data analysis
- Schemes for Engineers in Research and Development: Research Exchanges with China and India (Major Awards).

08/2007 – 12/2011 **Assistant Prof.**
Research Institute of Circuits and Systems

Department of Electronic Engineering, Tsinghua University

- Application specific FPGA (Field Programmable Gate Array) design
- Low power circuit design methodology
- Reliability-aware circuit design methodology
- On-chip communication strategies for MPSoC (Multi-Processor System On Chip)

10/2008 – 01/2009 **Visiting Scholar**

Hong Kong University of Science and Technology, with Prof. Jiang Xu

- Power ground noise aware MPSoC scheduling

05/2007 – 11/2007 **Visiting Student/Scholar**

Microsoft Research Asia

- Application specific FPGA design for search applications

PROJECTS (PI AND CO-PI)

NATIONAL PROJECTS

- Research on Power Efficient Heterogeneous Hardware Computing System for Video Data Analytics
  - National Science Foundation of China,
  - PI: **Yu Wang**, 2014.1-2017.12
- Research on LTE-Advanced Soft-Baseband Processing System
  - National Key Technology Program,
  - PI: **Yu Wang**, 2013.6-2014.12
- Research on Generic Technology for New IMT-Advanced Baseband Processing System
  - National Key Technology Program
  - PI: **Yu Wang**. 2011.01-2013.12
- Low Power Clock Tree Synthesis for Embedded CPU
  - Nation Key Technology Program on Core Electronics Devices/ Advanced Universal Chips/ Fundamental Software
  - PIs: Huazhong Yang, **Yu Wang**, 2010.01-2011.12
- Advanced EDA platform development
  - National Key Technology Program on Core Electronics Devices/ Advanced Universal Chips/ Fundamental Software
  - PIs: Huazhong Yang, **Yu Wang**. 2008.10-2010.12
- Research on FPGA based Anti-Degradation Machine Learning
  - National Science Foundation of China,
  - PI: **Yu Wang**, 2009.1-2011.12
- Low power Heterogeneous MPSoC based on Sensor Network on Chip
  - National 863 program,
  - PI: Yongpan Liu, **Yu Wang**, 2009.01-2010.12
- Research on Performance/Power/Reliability-driven Incremental Floorplanning
  - Tsinghua National Laboratory for Information Science and Technology (TNList) Cross-discipline Foundation,
  - PI: Yuchun Ma, **Yu Wang**. 2008.11-2010.10

INDUSTRY PROJECTS

- A-Eye --- a smart camera with real-time CNN
  - Microsoft,
  - PI: **Yu Wang**, 2015.02-2016.02
- Research on Multi-GPU training for DNN systems
  - Unisound,
  - PI: **Yu Wang**, 2014.12-2015.12
- Research on Hardware Database System
  - Huawei,
  - PI: **Yu Wang**, Guoliang Li, 2014.9-2015.9
- Heterogeneous Hardware Computing for Deep Neural Network
  - Microsoft,
  - PI: **Yu Wang**, 2013.4-2014.4
- Development of a real-time image processing hardware prototype system

- Mitsubishi Heavy Industries (MHI),
- PI: **Yu Wang,** 2010.1-2012.4

- Smart IOT Database Appliance on Hybrid System
  - IBM,
  - PI: **Yu Wang**, 2011.12-2013.12
- Low-Latency/High-Efficiency Programming Model for Pub/Sub Application on a Heterogeneous Multi-core Platform
  - IBM,
  - PI: **Yu Wang**, 2010.9-2011.8
- Heterogeneous Hardware Computing for Brain Network Research on Alzheimer's Disease
  - Microsoft,
  - PI: **Yu Wang**, 2010.4-2011.4
- GPU-based Acceleration for Machine Learning Algorithms
  - AMD China University Research Program,
  - PI: **Yu Wang**, 2009.4-2010.4
- General FPGA-based Acceleration for Machine Learning
  - Microsoft,
  - PI: **Yu Wang**, 2008.4-2009.4

HONORS

- Best Paper Candidate, Asia and South Pacific Design Automation Conference (ASPDAC) 2014.
- Best Paper Award, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2012.
- Best Poster Award, International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies, 2012.
- Best Paper Candidate, Asia and South Pacific Design Automation Conference (ASPDAC) 2012.
- IBM X10 Innovation Faculty Award.
- Excellent Student Research Training (SRT) Program Instructor, Tsinghua University, 2010.
- Second prize of AMD GPU (Graphics Processing Unit) Competition, China, 2010.
  (Our Team: Brainstorm, Team Member: Di Wu, Yi Shan, Xiaorui Zhang, Yu Wang)
- Two Best Paper Candidates, Asia and South Pacific Design Automation Conference (ASPDAC) 2010.
- Best Paper Candidate, International Symposium on Low Power Electronics and Design (ISLPED) 2009.
- Best Paper Candidate, IEEE/ACM International Conference on Hardware/Software-Coesign and System Synthesis, CODES+ISSS 2009.
- First prize of AMD GPU Competition, China, 2009.
  (Our Team: Sokudo Tsinghua, Team Member: Tianji Wu, Bo Wang, Feng Yan, Yu Wang)
- Excellent Student Research Training (SRT) Program Instructor, Tsinghua University, 2009.
- Excellent PhD Dissertation, Tsinghua University, 2007.

PRESENTATIONS

- Visiting Intel Research China, Jan. 2014, "Energy Efficient Neural Networks for Big Data Analytics".
- Visiting UCSB, Nov. 2014, "Energy Efficient Neural Networks for Big Data Analytics".
- Invited talk, Asia Sensor Workshop, Taiwan, Mar. 2014, "Time Series Data Mining on FPGAs".
- Visiting Cambridge, Computing Lab, July 2013, "Energy Efficient Computing System in NICS CAD".
- Visiting Imperial College London, Feb 2013, "Streaming Similarity Search on FPGA based on Dynamic Time Warping".
- Invited Talk, DSMC Workshop at ICCAD 2012, "Streaming Similarity Computing on FPGAs".
- Invited Talk, Profit'12, China, 2012, "A Heterogeneous Accelerator Platform for Multi-Subject Voxel-based Brain Network Analysis".

- ISVLSI'12, USA, August, 2012, "Temporal Performance Degradation under RTN: Evaluation and Mitigation for Nanoscale Circuits".
- Visiting Imperial College London, Jan, 2012, "Voxel-based Brain Network Analysis based on hybrid computing platforms".
- Invited talk, ICCAD'11, San Jose, USA, Nov. 2011, "A Heterogeneous Accelerator Platform for Multi-Subject Voxel-based Brain Network Analysis".
- Visiting National Tsinghua University, Sept. 2011, "Sparse Matrix/Graph Problems on Many Cores: LU Decomposition and Brain Network Analysis".
- ARC'11, Belfast, United Kingdom, March, 2011, "FPGA Accelerated Parallel Sparse Matrix Factorization for Circuit Simulations".
- Invited talk, ASQED'10, Penang, Malaysia, August, 2010, "Hardware Computing for Brain Network Analysis".
- Visiting National University of Singapore, Singapore, August, 2010, "Recent MPSoC research work in Nano-Integrated Circuits and Systems (NICS) Tsinghua".
- Visiting Pennsylvania State University, USA, April, 2010, "Recent MPSoC research work in Nano-Integrated Circuits and Systems (NICS) Tsinghua".
- ASPDAC'10, Taipei, Taiwan, Jan. 2010, "Three Dimensional Integrated Circuit (3D IC) Floorplan and Power/Ground Network Co-synthesis".
- ISLPED'09, San Francisco, USA, Aug. 2009, "Variation-Aware Supply Voltage Assignment for Minimizing Circuit Degradation and Leakage".
- DATE'09, Nice, France, Apr. 2009, "Gate Replacement Techniques for Simultaneous Leakage and Aging Optimization".
- APCCAS'08, Macao, China, Dec. 2008, "Dynamic TDM Virtual Circuit Implementation for NoCs".
- ASPDAC'08, Seoul, Korea, Jan. 2008, "A Capacitive Boosted Buffer Technique for High-Speed Process-Variation-Tolerant Interconnect in UDVS application".
- ASICON'07, Guilin, China, Oct. 2007, "Leakage power reduction through dual Vth assignment considering threshold voltage variation".
- DATE'07, Nice, France, Apr. 2007, "NBTI Modeling and Impact on the Input Vector Control Technique Considering Temperature Variation".
- APCCAS'06, Singapore, Dec. 2006, "Leakage Optimized DECAP Design for FPGAs".
- APCCAS'06, Singapore, Dec. 2006, "Fine-grain Sleep Transistor Placement Considering Leakage Feedback Gate".
- ISLPED'06, Munich, Germany, Oct. 2006, "Two-phase Fine-grain Sleep Transistor Insertion Technique in Leakage Critical Circuits".
- PATMOS'06, Montpellier, France, Sept. 2006, "IR-drop Reduction through Combinational Circuit Partitioning".
- ISQED'06, San Jose, USA, Mar. 2006, "Simultaneous Fine-grain Sleep Transistor Placement and Sizing for Leakage Optimization".

PROFESSIONAL ACTIVITIES

- Program Co-Chair
  - International Conference on Field Programmable Technology (**ICFPT**), 2011.
- Publicity Co-Chair
  - International Symposium on Low Power Electronics and Design (**ISLPED**), 2011.
- Finance Co-Chair
  - International Symposium on Low Power Electronics and Design (**ISLPED**), 2012/2013/2014/2015.
- Demo Session Chair, Special Session Chair
  - International Conference on Field Programmable Technology (**ICFPT**), 2010.
- Special Session Chair
  - International Symposium on Low Power Electronics and Design (**ISLPED**), 2013.
- Technical Program Committee Member
  - Design Automation Conference **(DAC)**, 2014/2015
  - ACM International Symposium on Field-Programmable Gate Arrays **(FPGA)**,

2014/2015

- Design Automation and Test in Europe (**DATE**), 2012/13/14/2015
- International Symposium on Quality Electronic Design (**ISQED**) 2008-now
- IEEE Computer Society Annual Symposium on VLSI (**ISVLSI**) 2009-now
- Asia Symposium on Quality Electronic Design (**ASQED**) 2009/10
- IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**) 2009/10
- International Symposium on Low Power Electronics and Design (**ISLPED**) 2010-now
- Asia and South Pacific Design Automation Conference (**ASPDAC**) 2010-12, 2014-15
- International Conference on Field Programmable Technology (**ICFPT**) 2010-now

- Associate Editor of JCSC (Journal of Circuits, Systems, and Computers, from 2013.6- now).
- Associate Editor of IEEE Trans on CAD (from 2013.12- now)
- Reviewer of APCCAS, ISCAS, ISQED, GLSVLSI, DAC, VLSID08/09, ASPDAC08/09, DATE09; IEEE Transactions on VLSI, International Journal of Electronics, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Computer-Aided Design, ACM Transactions on Embedded Computing Systems, and etc.

SELECTED STUDENT AWARD

2015, Boxun Li, Excellent Research Award @ Student Research Forum ASPDAC 2015

2014, Xiaoming Chen, Excellent graduate of Beijing

2014, Xiaoming Chen, Excellent PhD thesis award of Tsinghua University

2013, Song Yao, Gold Medal in ACM Student Research Competition @ ICCAD

2013, Xiaoming Chen, National Scholarship, awarded by Ministry of Education of China

2012, Xiaoming Chen, Young Scholarship Award for Distinguished Doctoral Candidates, awarded by Ministry of Education of China

2012, Yi Shan, IBM PhD Fellowship Award, among 84 around the world

2007- now, 5 students won the Excellent Undergraduate Thesis Award of Tsinghua University

PUBLICATIONS

(*means my supervised or co-supervised student)

JOURNAL PUBLICATIONS:

[J37] Wenqiang Wang*, Jing Yan, Ningyi Xu, **Yu Wang**, Feng-Hsiung Hsu "Real-time High-quality Stereo Vision System in FPGA", in IEEE Trans on Circuits and Systems for Video Technology.

[J36] Hong Zhang*, Xue Feng, Boxun Li*, **Yu Wang**, Kaiyu Cui, Fang Liu, Weibei Dou, and Yidong Huang, "Integrated photonic reservoir computing based on hierarchical time-multiplexing structure", in Optical Express.

[J35] Wulong Liu*, **Yu Wang**, Guoqing Chen, Yuchun Ma, Yuan Xie, Huazhong Yang, "Whitespace-Aware TSV Arrangement in 3-D Clock Tree Synthesis", accepted by IEEE Transaction on VLSI.

[J34] **Yu Wang**, Song Yao*, Shuai Tao*, Xiaoming Chen*, Yuchun Ma, Yiyu Shi, Huazhong Yang, "HS3DPG: Hierarchical Simulation for 3D P/G Network", accepted by IEEE Transaction on VLSI.

[J33] Wujie Wen*, Yaojun Zhang*, Yiran Chen, **Yu Wang**, Yuan Xie, "PS3-RAM: A Fast Portable and Scalable Statistical STT-RAM Reliability/Energy Analysis Method", accepted by IEEE Trans on CAD.

[J32] Wulong Liu*, Yu Wang*, **Yu Wang**, Xue Feng, Yuan Xie, Yidong Huang, Huazhong Yang, "Exploration of Electrical and Novel Optical Chip-to-Chip Interconnects", accepted by IEEE Design & Test.

[J31] Xiaoming Chen*, Ling Ren*, **Yu Wang**, Huazhong Yang, "GPU-Accelerated Sparse LU Factorization for Circuit Simulation with Performance Modeling", IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS), March 2014.

[J30] Yi Shan*, Yuchen Hao*, Wenqiang Wang*, **Yu Wang**, Wayne Luk, Xu Chen, Huazhong Yang, "Hardware Acceleration for an Accurate Stereo Vision System using Mini-Census Adaptive Support

Region",in ACM Trans. on Embedded Computing Systems (TECS'14), vol. 13, no. 4s, April 2014.
[J29] Wulong Liu*, **Yu Wang**, Yuchun Ma, Yuan Xie, Huazhong Yang, "On-Chip Hybrid Power Supply System for Wireless Sensor Nodes", in ACM Journal on Emerging Technologies in Computing Systems (JETC'14), vol. 10, no. 3, April 2014.
[J28] Xiaoming Chen*, **Yu Wang**, Yu Cao, Yuan Xie, Huazhong Yang, "Assessment of Circuit Optimization Techniques under NBTI", in IEEE Design & Test of Computers, Special Issue on Variability and Aging 2013, vol. 30, no. 6, pp. 40-49, Nov. 2013.
[J27] **Yu Wang**, Haixiao Du*, Mingrui Xia, Ling Ren*, Mo Xu*, Teng Xie, Gaolang Gong, Ningyi Xu, Huazhong Yang, Yong He, "A Hybrid CPU-GPU Accelerated Framework for Fast Mapping of High-Resolution Human Brain Connectome", in Public Library of Science (PLOS) ONE 2013, vol. 8, no. 5, May, 2013.
[J26] Xiaoming Chen*, Hong Luo, **Yu Wang**, Yu Cao, Yuan Xie, Yuchun Ma, Huazhong Yang, "Evaluation and Mitigation of Performance Degradation under RTN for Digital Circuits ", IET Circuits, Devices & Systems (IET-CDS), vol.7, no.5, pp.273-282, Sep. 2013.
[J25] Xiaoming Chen*, **Yu Wang**, Huazhong Yang, "NICSLU: An Adaptive Sparse Matrix Solver for Parallel Circuit Simulation", in IEEE Trans. on CAD 2013, vol. 32, no. 2, pp. 261-274, Feb. 2013.
[J24] Weichen Liu*, **Yu Wang**, Xuan Wang, Jiang Xu, Huazhong Yang, "On-Chip Sensor Network for Efficient Management of Power Gating Induced Power/Ground Noise in Multiprocessor System-on-Chip", in IEEE Trans. on Parallel and Distributed Systems 2013, vol. 24, no, 3, pp. 767-777, 2013.
[J23] Yibo Chen*, **Yu Wang**, Yuan Xie, Andres Takach, "Parametric Yield Driven Resource Binding in High-Level Synthesis with Multi-Vth/Vdd Library and Device Sizing", in Journal of Electrical and Computer Engineering 2012, vol. 12, no. 3, Jan. 2012.
[J22] Xiaoming Chen*, **Yu Wang**, Yu Cao, Yuchun Ma, Huazhong Yang, "Variation-Aware Supply Voltage Assignment for Simultaneous Leakage and Aging Optimization", in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 20, no. 11, pp. 2143-2147, Nov. 2012.
[J21] 史圣卿*，陈凯，汪玉，罗嵘. 基于FPGA的稀疏网络关键节点计算的硬件加速方法研究. 电子与信息学报, 2011, vol. 33, no. 10, pp. 2536-2540, Oct. 2010. (in Chinese)
[J20] Xiaoming Chen*, Wei Wu*, **Yu Wang**, Hao Yu, Huazhong Yang, "An EScheduler based Data Dependency Analysis and Task Scheduling for Parallel Circuit Simulation", in IEEE Trans. on Circuits and Systems II, vol. 58, no. 10, pp. 702-706, 2011.
[J19] **Yu Wang**, Hong Luo*, Ku He*, Rong Luo, Huazhong Yang, Yuan Xie, "Temperature-Aware NBTI Modeling and the Impact of Standby Leakage Reduction Techniques on Circuit Performance Degradation", IEEE Trans. Dependable Sec. Comput. Vol. 8, no. 5, pp. 756-769, 2011.
[J18] **Yu Wang**, Xiaoming Chen*, Wenping Wang, Yu Cao, Yuan Xie, Huazhong Yang, "Leakage Power and Circuit Aging Co-Optimization by Gate Replacement Techniques", in IEEE Transaction on VLSI, vol.19, no.4, pp.615-628, April 2011.
[J17] **Yu Wang**, Jiang Xu, Yan Xu*, Weichen Liu, Huazhong Yang, " Power Gating Aware Task Scheduling in MPSoC", IEEE Trans. VLSI Syst. Vol. 19, no. 10, pp. 1801-1812, 2011.
[J16] Kan Wang*, Sheqin Dong, Yuchun Ma, **Yu Wang**, Xianlong Hong, Jason Cong, "Leakage-Aware TSV-Planning with Power-Temperature-Delay Dependence in 3D ICs", IEICE Transactions, vol.94, no.12, pp.2490-2498, Dec. 2011.
[J15] Jing Yan*, Ningyi Xu, Xiongfei Cai, Rui Gao, **Yu Wang**, Rong Luo, Fenghsiung Hsu, "An FPGA-based Accelerator for the Relevance Ranking in Web Search Engines", in ACM Trans on RETS, vol.4, no. 3, pp. 1-25, August 2011.
[J14] Qian Ding*, **Yu Wang** , Hui Wang, Rong Luo, Huazhong Yang, "Soft Error Generation Analysis in Combinational Logic Circuits", in Journal of Semiconductors 2010, vol. 31, no. 9, pp. 095015: 1-6, Sep. 2010.
[J13] Qian Ding*, **Yu Wang**, Hui Wang, Rong Luo, Huazhong Yang, "Output Remapping Technique for Critical Paths Soft-Error Rate Reduction," IET Computers and Digital Techniques, vol. 4, no. 4, pp. 325 - 333, 2010.
[J12] Guangming Yu*, **Yu Wang**, Huazhong Yang, Hui Wang, "Fast-Locking All-Digital Phase-Locked Loop with Digitally Controlled Oscillator Tuning Word Estimating and Presetting", IET Circuits, Devices and Systems, vol. 4, no. 3, pp. 207 - 217, 2010.
[J11] Qian Ding*, **Yu Wang**, Hui Wang, Rong Luo, Huazhong Yang, "SERSim: a Soft Error Rate Simulator and a Case Study for a 32-bit OpenRisc 1200 Microprocessor," International Journal of Electronics, vol. 97, no. 4, pp. 441 - 455, 2010.

[J10] **Yu Wang**, Hong Luo*, Ku He*, Rong Luo, Huazhong Yang, Yuan Xie, "NBTI-aware Dual Vth Assignment for Leakage Reduction and Lifetime Assurance," Chinese Journal of Electronics, vol. 18, no. 2, pp. 225 - 230, 2009.

[J9] **Yu Wang**, Xukai Shen*, Rong Luo, Huazhong Yang, "Leakage power reduction through Dual Vth assignment considering threshold voltage variation", Journal of Circuits, Systems and Computers, vol. 18, no. 7, pp. 1243 - 1261, 2009.

[J8] Hong Luo*, **Yu Wang**, Rong Luo, Huazhong Yang and Yuan Xie," Temperature-aware NBTI Modeling Techniques in Digital Circuits ", IEICE Transactions on Electronics, vol. 92, no. 6, pp. 875 - 886, 2009.

[J7] Michael DeBole*, Ramakrishnan Krishnan*, Varsha Balakrishnan*, Wenping Wang*, Luo Hong*, **Yu Wang**, Yuan Xie , Yu Cao, N. Vijaykrishnan, " A Framework for Estimating NBTI Degradation of Micro-architectural Components", International Journal of Parallel Programming, vol. 37, no. 4, pp. 417 - 431, 2009.

[J6] Yuchun Ma, Xin Li*, **Yu Wang**, Xianlong Hong, "Thermal-Aware Incremental Floorplanning for 3D ICs based on MILP Formulation", IEICE Transactions on Fundamentals of Electronics Communications and Computer Sciences, vol. 92, no. 12, Dec. 2009.

[J5] Bo Zhao*, **Yu Wang**, Huazhong Yang, and Hui Wang, "The NBTI Impact on RF Front End in Wireless Sensor Networks", in Journal of Electronic Science and Technology, ICDT'09, pp. 1-4.

[J4] **Yu Wang**, Ku He*, Rong Luo, Hui Wang, Huazhong Yang, "Two-phase Fine-grain Sleep Transistor Insertion Technique in Leakage Critical Circuits," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 16, no. 9, pp. 1101 -1113, 2008.

[J3] Hong Luo*, **Yu Wang**, Rong Luo, Huazhong Yang, "Software Tools for Analyzing NBTI-induced Digital Circuit Degradation," in Journal of Electronics (China), Volume 26, No. 5, pp. 715-719, 2009.

[J2] **Yu Wang**, Huazhong Yang, Hui Wang, "Signal-path Level Dual-Vt Assignment for Leakage Power Reduction," in Journal of Circuits, System and Computers, 2006, Vol. 15, No. 2, pp:197-216.

[J1] Huazhong Yang, **Yu Wang**, Hai Lin*, Rong Luo, Hui Wang, "Fine-grain Sleep Transistor Insertion for Leakage Reduction," in Chinese Journal of Semiconductors, 2006, Vol.27, No.2, pp:258-265.

CONFERENCE PUBLICATIONS:

2015

[C101] **Yu Wang**, Tianqi Tang, Lixue Xia, Boxun Li, Peng Gu, Hai Li, Yuan Xie, Huazhong Yang, "Energy Efficient RRAM Spiking Neural Network for Real Time Classification", in GLSVLSI 2015. (invited paper)

[C100] Boxun Li*, Lixue Xia*, Peng Gu*, **Yu Wang**, and Huazhong Yang. Merging the interface: Power, area and accuracy co-optimization for RRAM crossbar-based mixed-signal computing system. In DAC, 2015.

[C99] Gushu Li*, Xiaoming Chen*, Guangyu Sun, Hank Hoffmann, Yongpan Liu, **Yu Wang**, and Huazhong Yang. A STT-RAM-based Low-Power Hybrid Register File for GPGPUs. In DAC, 2015

[C98] Xiaoxiao Liu*, Mengjie Mao*, Beiye Liu*, Boxun Li*, Hao Jiang, **Yu Wang**, Mark Barnell, Qing Wu, J. Joshua Yang, Hai Li, Yiran Chen, "Reno: A Highly-efficient Reconfigurable Neuromorphic Computing Accelerator Design", in DAC 2015.

[C97] Xiaolong Xie*, Yun Liang, **Yu Wang**, Guangyu Sun, Tao Wang, "Coordinated Static and Dynamic Cache Bypassing for GPUs", in HPCA 2015.

[C96] Xiaoming Chen*, **Yu Wang**, Huazhong Yang, "A Fast Parallel Sparse Solver for SPICE-based Circuit Simulators", in DATE 2015 (Long, acceptance rate 22%).

[C95] Tianqi Tang*, Lixue Xia*, Boxun Li*, Rong Luo, **Yu Wang**, Yiran Chen, Huangzhong Yang, "Spiking Neural Network with RRAM : Can We Use it for Real-World Application?", in DATE 2015 (Long, acceptance rate 22%) .

[C94] Xinyu Niu*, Wayne Luk and **Yu Wang**, "EURECA: On-Chip Configuration Generation for Effective Dynamic Data Access", FPGA 2015 (Long, acceptance rate 21%).

[C93] Wulong Liu*, Guoqing Chen, **Yu Wang**, Huazhong Yang, "Modeling and Optimization of Low Power Resonant Clock Mesh", in ASPDAC 2015.

[C92] Peng Gu*, Boxun Li*, Tianqi Tang*, Shimeng Yu, Yu Cao, **Yu Wang**, Huazhong Yang, "Technological Exploration of RRAM Crossbar Array For Matrix-Vector Multiplication", in ASPDAC 2015.

[C91] Li-xue Xia*, Rong Luo, Bin Zhao, **Yu Wang**, Huazhong Yang, "An Accurate and Low Cost PM2.5

Estimation Method Based on Artificial Neural Network", in ASPDAC 2015.

2014

[C90] Guohao Dai*, Yi Shan*, Fei Chen, Yu Zhang, **Yu Wang**, Kun Wang and Huazhong Yang, "Online Scheduling for FPGA Computation in the Cloud", in International Conference on Field-Programmable Technology (FPT'14).

[C89] Wenqiang Wang*, Kaiyuan Guo*, Mengyuan Gu*, Yuchun Ma and **Yu Wang**, "A Universal FPGA-based Floating-point Matrix Processor for Mobile Systems", in International Conference on Field-Programmable Technology (FPT'14).

[C88] Tianqi Tang*, Rong Luo, Boxun Li*, Hai Li, **Yu Wang**, Huazhong Yang, "Energy Efficient Spiking Neural Network Design with RRAM Devices", in ISIC 2014. (Invited)

[C87] Fei Chen, Yi Shan*, Yu Zhang, **Yu Wang**, Hubertus Franke, Xiao Tao Chang and Kun Wang, "Enabling FPGAs in the Cloud", Computer Frontiers (CF'14).

[C86] Wulong Liu*, Guoqing Chen, Xue Han*, **Yu Wang**, Yuan Xie, Huazhong Yang, "Design Methodologies for 3D Mixed Signal Integrated Circuits: A Practical 12-bit SAR ADC Design Case", Design Automation Conference (DAC'14), 2014 51st Annual Design Automation Conference, pp.1-6, June 2014.

[C85] Xiaoming Chen*, **Yu Wang**, Yun Liang, Yuan Xie, Huazhong Yang, "Run-Time Technique for Simultaneous Aging and Power Optimization in GPGPUs", Design Automation Conference (DAC'14), pp.168:1-168:6, Jun 1-5, 2014..

[C84] Boxun Li*, Erjin Zhou*, Bo Huang*, Jiayi Duan*, **Yu Wang**, Ningyi Xu, Jiaxing Zhang, Huazhong Yang, "Large Scale Recurrent Neural Network on GPU", in IJCNN 2014.

[C83] Song Yao*, Xiaoming Chen*, **Yu Wang**, Yuchun Ma, Yuan Xie, Huazhong Yang, "Efficient Region-aware P/G TSV planning for 3D ICs.", Quality Electronic Design (ISQED), 2014 15th International Symposium on, pp.171-178, 3-5 March 2014.

[C82] **Yu Wang**, Boxun Li*, Rong Luo, Yiran Chen, Ningyi Xu, Huazhong Yang, "Energy Efficient Neural Networks for Big Data Analytics", Design, Automation and Test in Europe (DATE'14), pp1-2, March 2014.

[C81] Boxun Li*, **Yu Wang**, Yiran Chen, Helen Li, Huazhong Yang, "ICE: INline Calibration for Memristor Crossbar-based Computing Engine", Design, Automation and Test in Europe (DATE'14), pp.184, March 2014.

[C80] Yuliang Sun*, Zilong Wang*, Sitao Huang*, Lanjun Wang, **Yu Wang**, Rong Luo, Huazhong Yang, "Accelerating Frequent Item Counting with FPGA", Field-programmable gate arrays(FPGA'14), 2014 ACM/SIGDA international symposium on, pp.109-112, February 2014.

[C79] Miao Hu*, **Yu Wang**, Qinru Qiu, Yiran Chen, Hai Li, "The Stochastic Modeling of TiO_2 Memristor and Its Usage in Neuromorphic System Design", Design Automation Conference (ASP-DAC), 2014 19th Asia and South Pacific, pp.831-836, Jan. 21-23, 2014.

[C78] Xiaoming Chen*, **Yu Wang**, Yu Cao, Huazhong Yang, "Statistical Analysis of Random Telegraph Noise in Digital Circuits", Design Automation Conference (ASP-DAC), 2014 19th Asia and South Pacific, pp.161-166, Jan. 21-23, 2014. (Best Paper Candidate).

[C77] Boxun Li*, Yuzhi Wang*, **Yu Wang**, Yiran Chen, Huazhong Yang, "Training Itself: Mixed-signal Training Acceleration for Memristor-based Neural Network", Design Automation Conference (ASP-DAC), 2014 19th Asia and South Pacific, pp.361-366, Jan. 21-23, 2014.

2013

[C76] Xiaoming Chen*, Du Su*, **Yu Wang**, Huazhong Yang, "Nonzero Pattern Analysis and Memory Access Optimization in GPU-based Sparse LU Factorization for Circuit Simulation", in Proceedings of the 3rd Workshop on Irregular Applications: Architectures and Algorithms (IA'13, SC'13 workshop), pp.8:1-8:8, Nov. 2013.

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